Contribution ID: **40**   Type: **Poster**

Clock and Timing Distribution in the LHCb Upgraded Detector and Readout System

Tuesday 23 September 2014 16:48 (1 minute)

The LHCb experiment is upgrading part of its detector and the entire readout system towards a full 40 MHz readout system in order to run between five and ten times its initial design luminosity and increase its trigger efficiency. In this paper, the new timing, trigger and control distribution system for such an upgrade is reviewed with particular attention given to the distribution of the clock and timing information across the entire readout system, up to the FE and the on-detector electronics. Different solutions are compared in terms of reliability, jitter, complexity and implementation.

Summary

In the LHCb upgrade, the entire readout architecture will need to be replaced in order to cope with higher sub-detector occupancies, higher rate and higher network load. In particular, the entire LHCb Front-End (FE) and Back-End (BE) electronics will be upgraded to run in a trigger-less fashion, i.e. without the aid of a trigger, thus recording data continuously at the full LHC frequency, for a total data bandwidth of various TB/s. Events selection will be performed in a very flexible and efficient fully software processing farm.

Synchronicity across the whole detector will be maintained by a centralized timing and readout control system (TFC), acting as the TTC distribution system in LHCb, by transmitting a set of commands and information to the whole readout system –and by transmitting a deterministic and controlled clock. In the upgrade scenario, the TFC system is composed of a Readout Supervisor, which centrally generates the commands and it is interfaced to the LHC timing system, and a set of Interface Boards, whose main aim is to act as an active fan-in/fan-out with the rest of the readout system. All the TFC boards are also interfaced to the global LHCb Experiment Control System (ECS) via a PCIe interface bus on a host PC.

While functionally the TFC system will remain very similar to the current system in LHCb, its technological implementation must be done in a different way to cope with a completely new readout architecture based on different technologies. The Front-End electronics will heavily profit from the CERN development of the GBT and GBT-SCA chipset and the Back-End electronics will be based on a PCIe Gen3 readout card hosted on a commercial PC, likely interfaced via InfiniBand to the Data Acquisition network.

In this paper, various solutions and implementation for the distribution of the clock and timing in the upgraded scenario are reviewed. These solutions had been envisaged during the course of the specifications of the system and they are being tested in order to compare their performance in terms of reliability, jitter and complexity within the framework of the upgrade of the LHCb experiment in order to make a final decision on the solution to be used.

Amongst the solutions that will be reviewed are the use of the GBT chipset at the Front-End, the way in which the Front-End electronics shall configure the chipset in order to comply with the specifications and the way in which it shall be driven from the TTC point of view. Moreover, options taken into considerations for the distribution of timing and clock at the Back-End are reviewed as well, comparing synchronization techniques using the CERN-ESE proposition of PON technologies for TTC distribution, using commercial FPGA transceivers (Altera) and the usage of ad-hoc custom solutions. Measurements of jitter and phase control for each solution are presented, together with a brief review of their implementations and requirements to be met.

Author: ALESSIO, Federico (CERN)

Co-authors: HACHON, Frederic (Centre National de la Recherche Scientifique (FR)); CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR)); WYLLIE, Ken (CERN); BARROS MARIN, Manoel (CERN); Mrs BARON, Sophie (CERN)

Presenter: ALESSIO, Federico (CERN)

Session Classification: First Poster Session

Track Classification: Systems

Author: ALESSIO, Federico (CERN)

Co-authors: HACHON, Frederic (Centre National de la Recherche Scientifique (FR)); CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR)); WYLLIE, Ken (CERN); BARROS MARIN, Manoel (CERN); Mrs BARON, Sophie (CERN)

Presenter: ALESSIO, Federico (CERN)

Session Classification: First Poster Session