



A Radiation Hardened TDC with < 10 ps Resolution and Improved Recovery Time from Single Events in 40 nm CMOS

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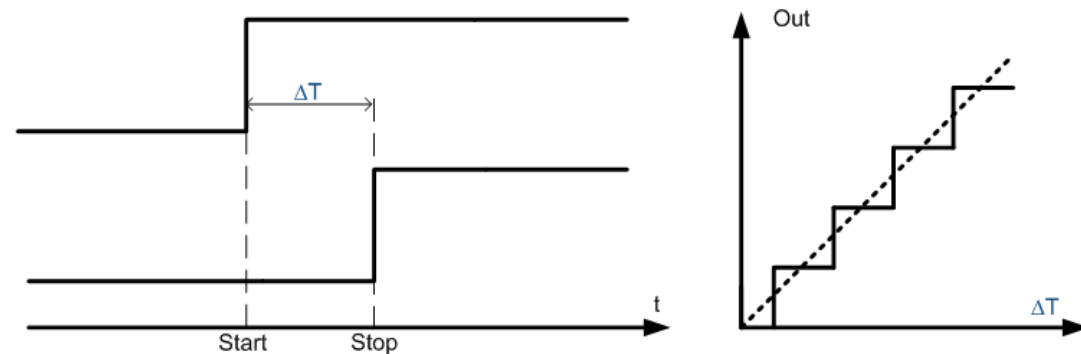
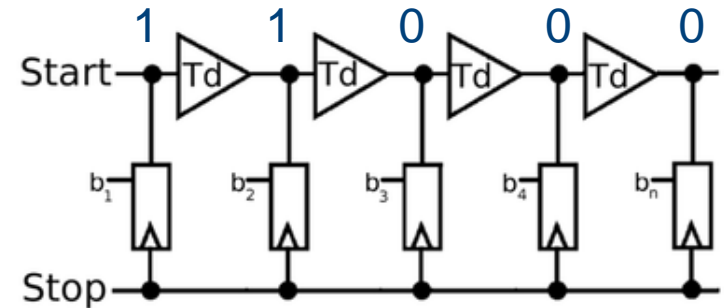
Content

- TDC architecture
- Building blocks
- Measurements
- Conclusion

TDC architecture

High level

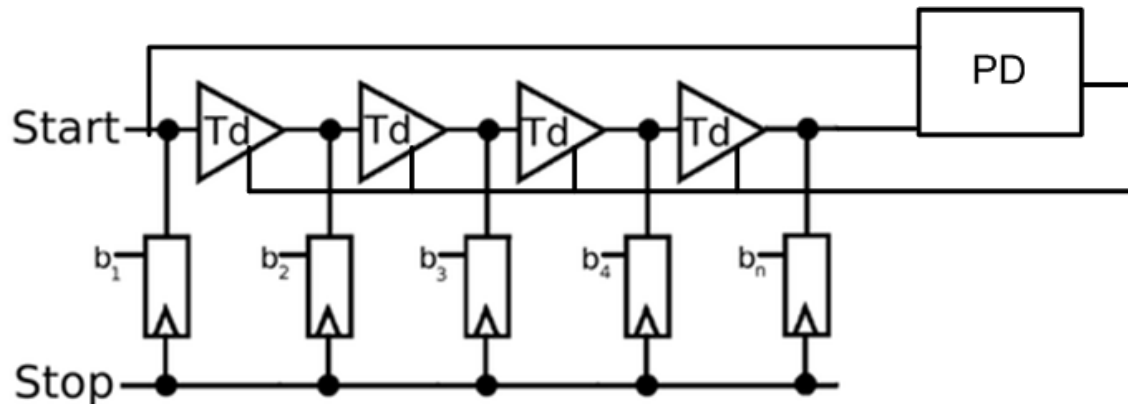
- Flash TDC
 - Time-to-Digital converter
 - $\Delta T \rightarrow$ Digital value
- Single-shot resolution
- Linearity
- Radiation effects
 - TID
 - Delay variation
 - SEE
 - Signal disturbance



TDC architecture

High level

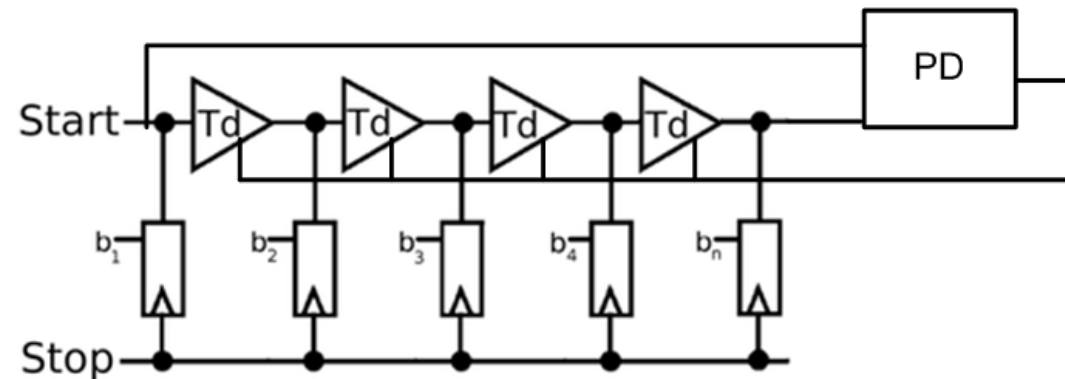
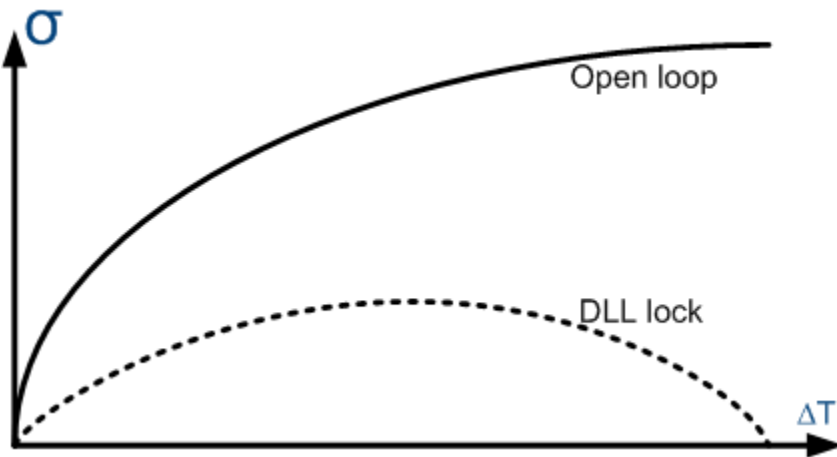
- DLL based TDC
 - Constant resolution
 - $T_d = T_{ref}/N$
 - Corrects PVT
 - Adapts to radiation
 - Interpolation for sub-gate delay resolution



TDC architecture

High level

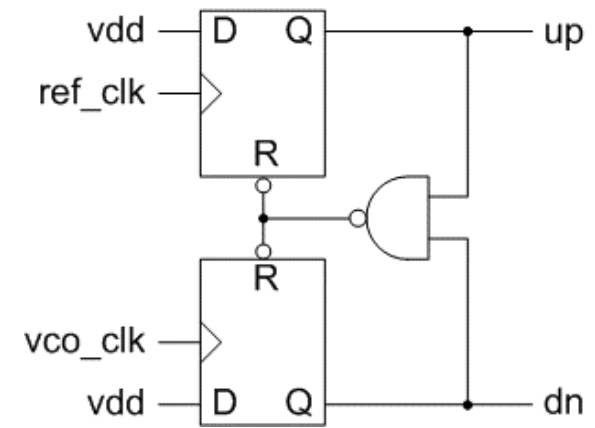
- Lower mismatch
 - Low uncertainty at both PD inputs
 - PD corrects for INL mismatch
- Requires startup time
 - SEE sensitive
 - Resolution unknown during acquisition!



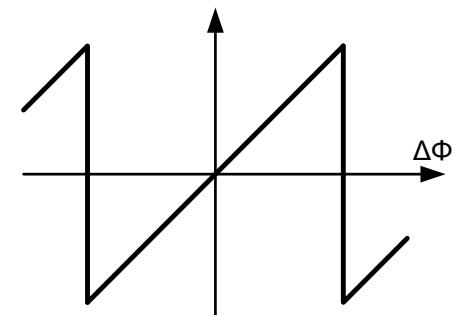
TDC architecture

Phase detector

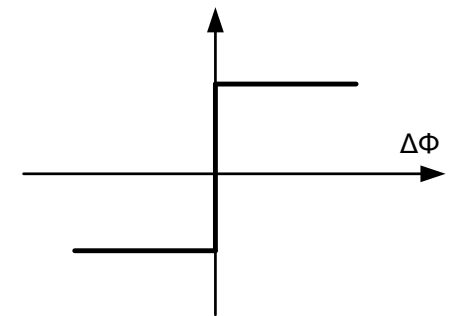
- PFD detector
 - Signal proportional to $\Delta\Phi$
 - Current changes with $\Delta\Phi$
 - Static phase offset
 - Charge-pump offset generates offset
 - False- or harmonic lock in a DLL
- Bang-bang detector (BBPD)
 - “Early” or “Late”
 - Low offset
 - Trade-off speed \leftrightarrow ripple
 - Low ripple = low speed



PFD output

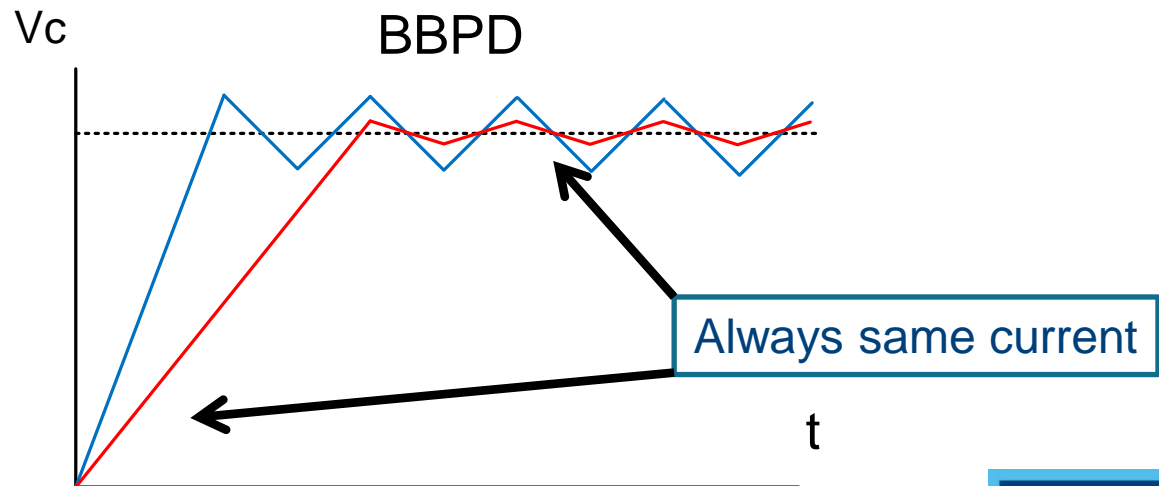
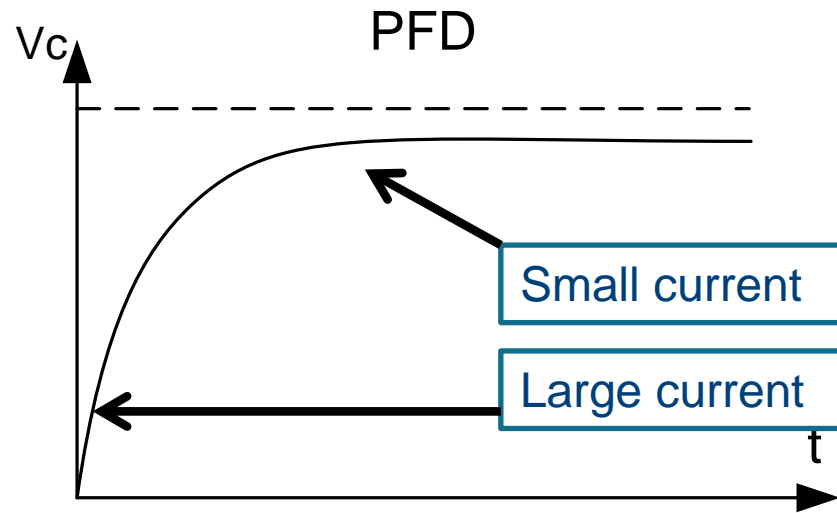


BBPD output



TDC architecture

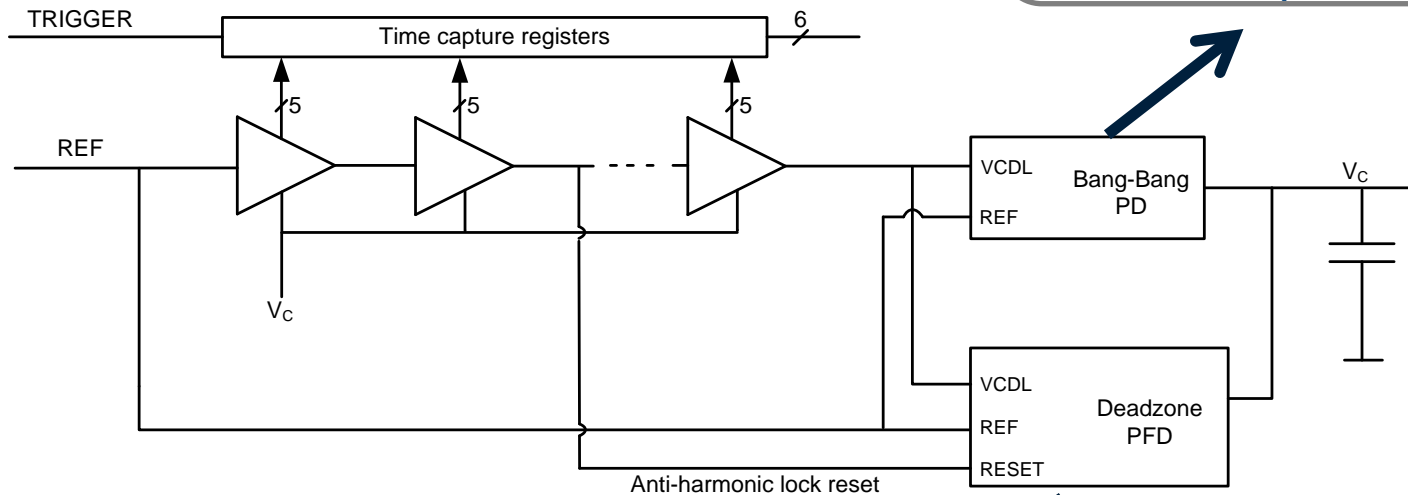
Phase detector



TDC architecture

Phase detector

- Combine BBPD and PFD



Bangbang PD

- Low bandwidth (fine adjustment)
- Low SPO (1.2 ps 3σ) (TID)
- Trade-off: speed vs. ripple (spur)

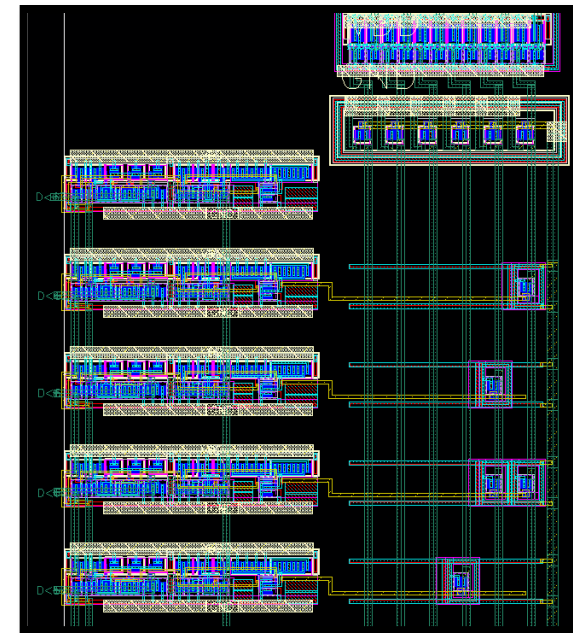
PFD

- Deadzone (20ps)
- High bandwidth
- SEE recovery
- SPO

TDC building blocks

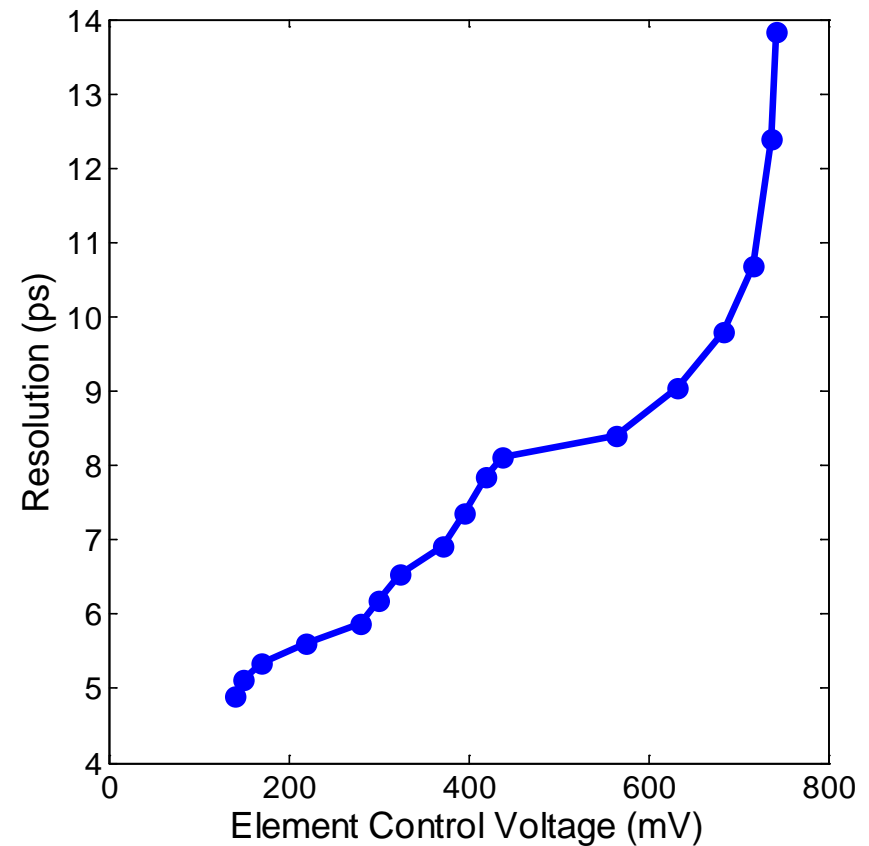
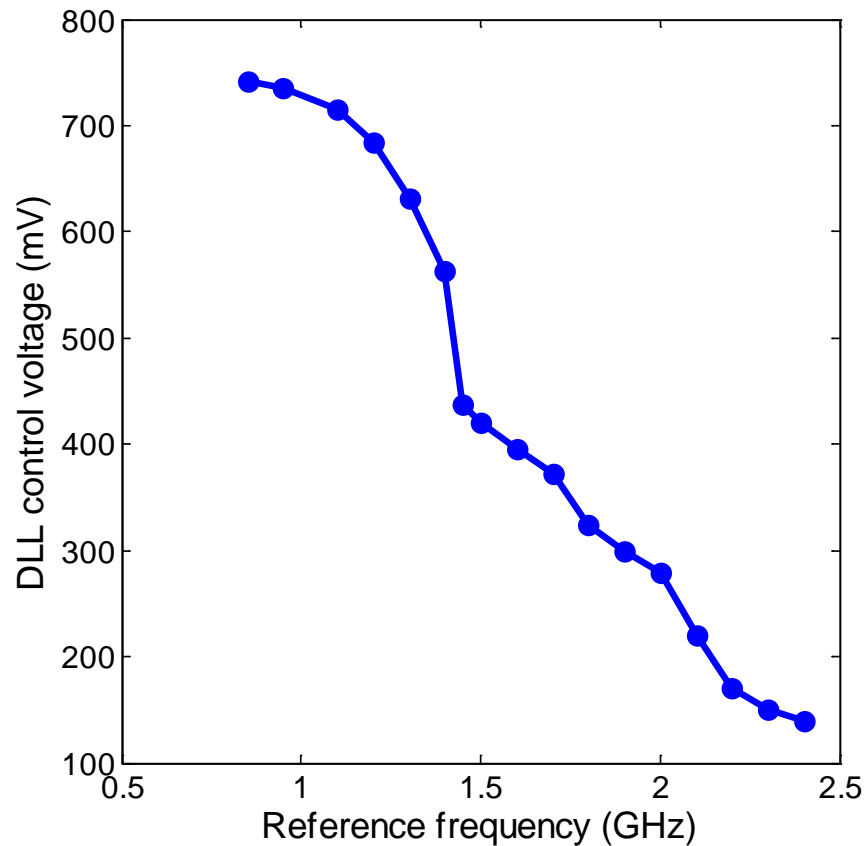
Back-end logic

- Pseudo thermometer code → Binary
 - Bubble correction
 - Searches for '100' event
 - Neglects '101' bubbles
 - Corrects single bubble (extendable)
 - Priority detection
 - If multiple '100' events occur, take first one
 - ROM
 - Hardware ROM controlled by priority detector



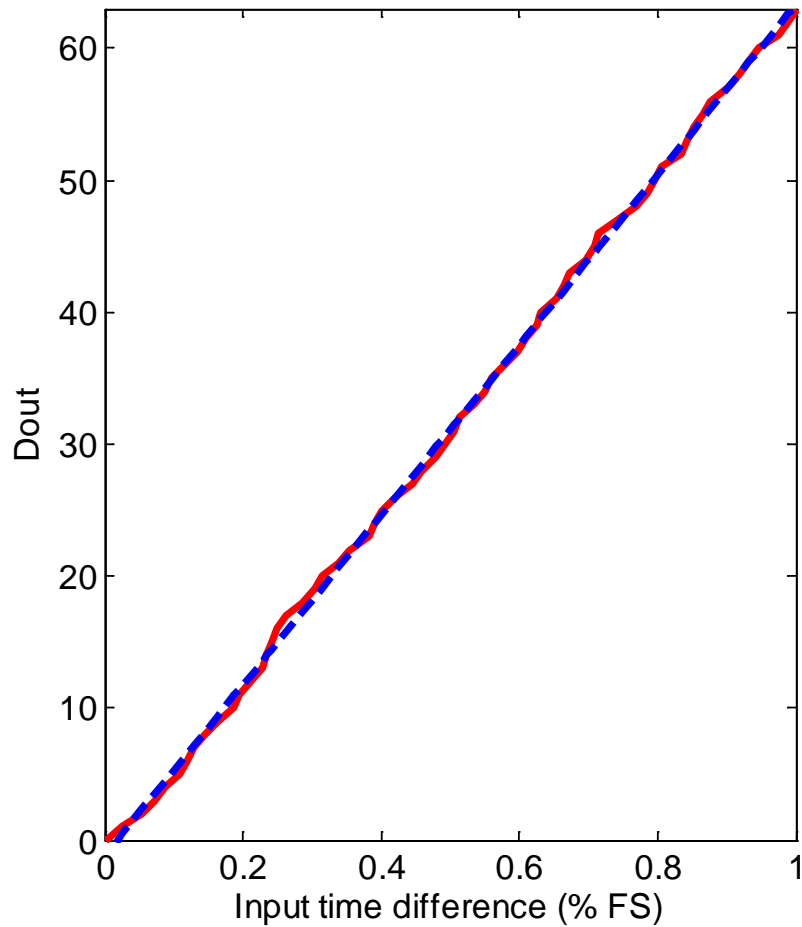
Measurements

- Delay cell resolution (0.9 V nominal V_{dd})

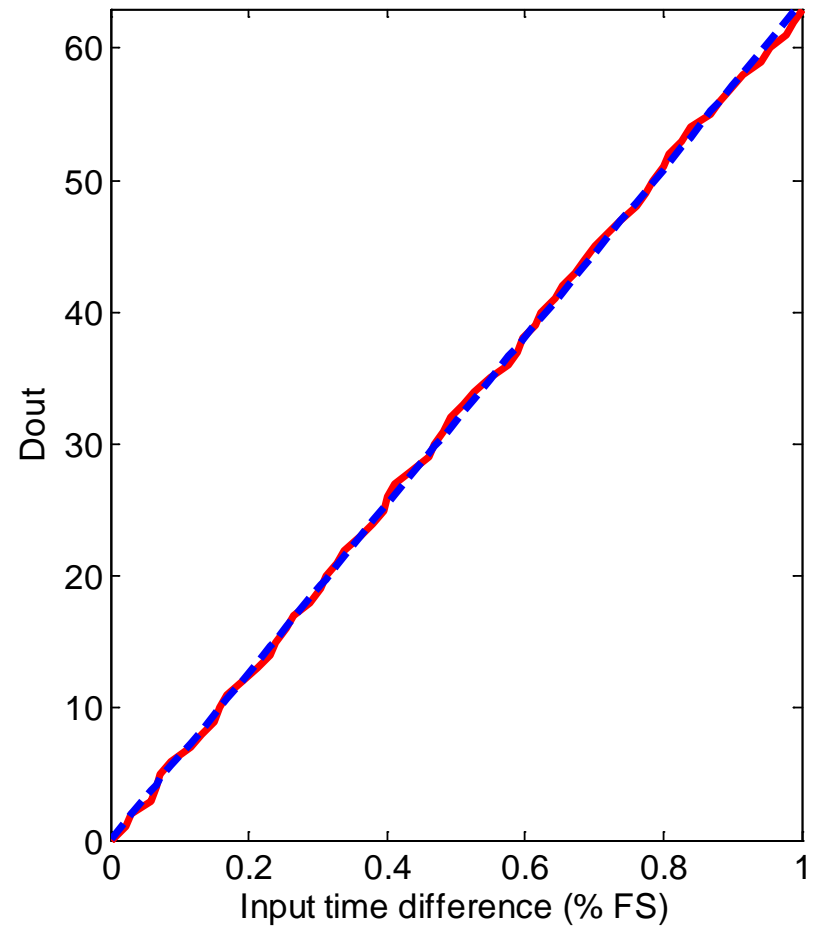


Measurements

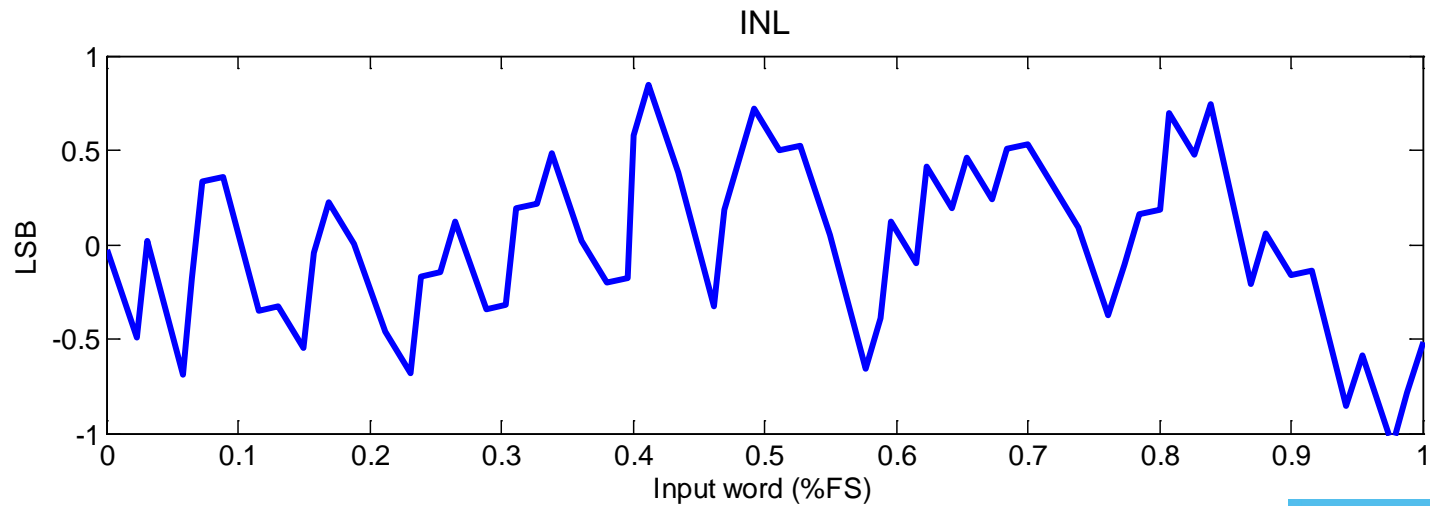
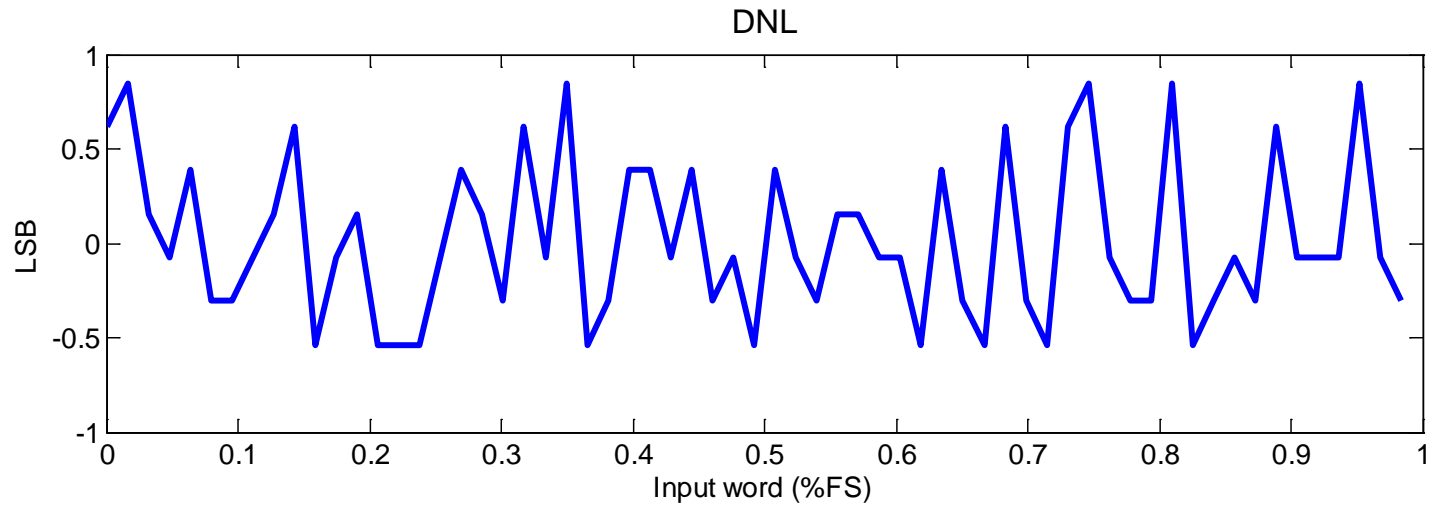
Chip 1 TDC transfer, $f_{\text{ref}} = 1.5\text{GHz}$, $T_{\text{LSB}} = 7.8\text{ps}$



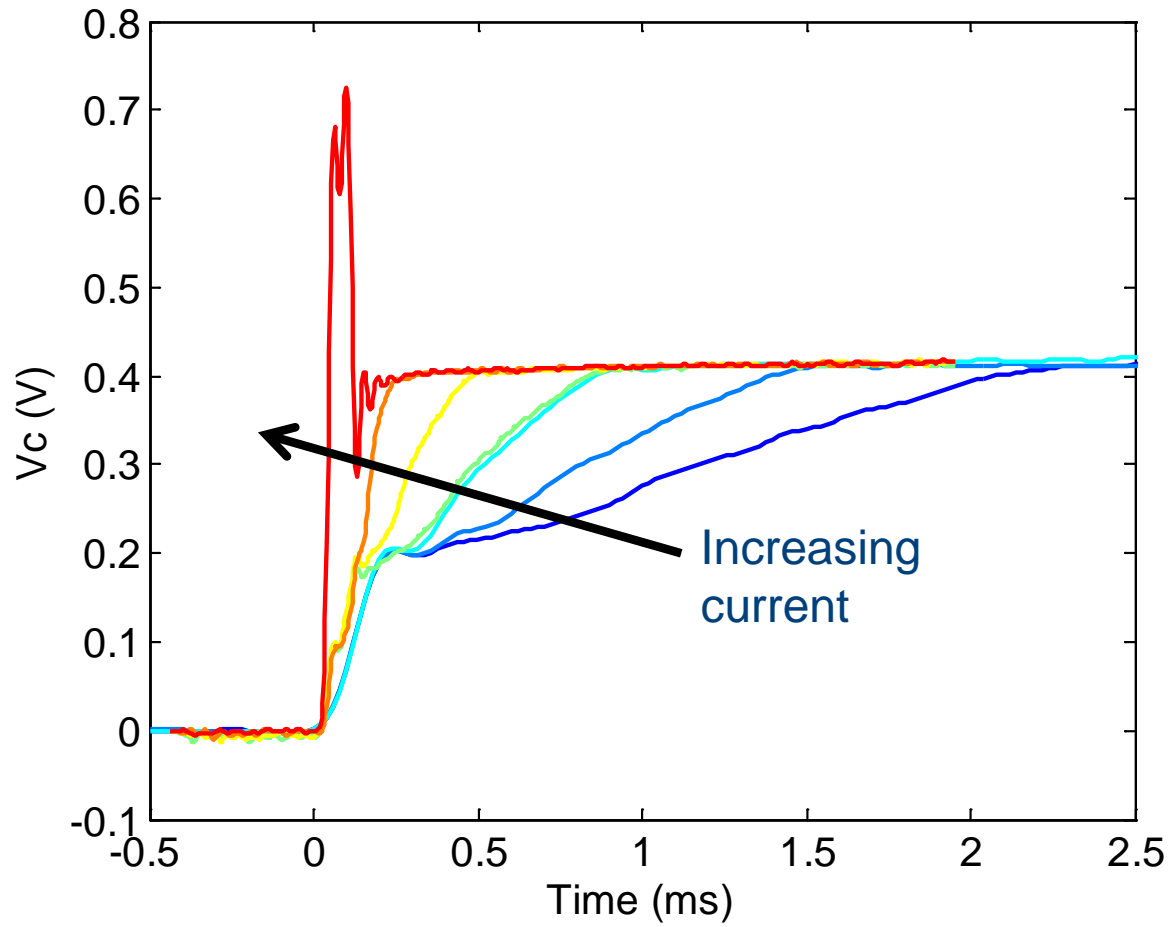
Chip 2 TDC transfer, $f_{\text{ref}} = 1.5\text{GHz}$, $T_{\text{LSB}} = 7.8\text{ps}$



Measurements

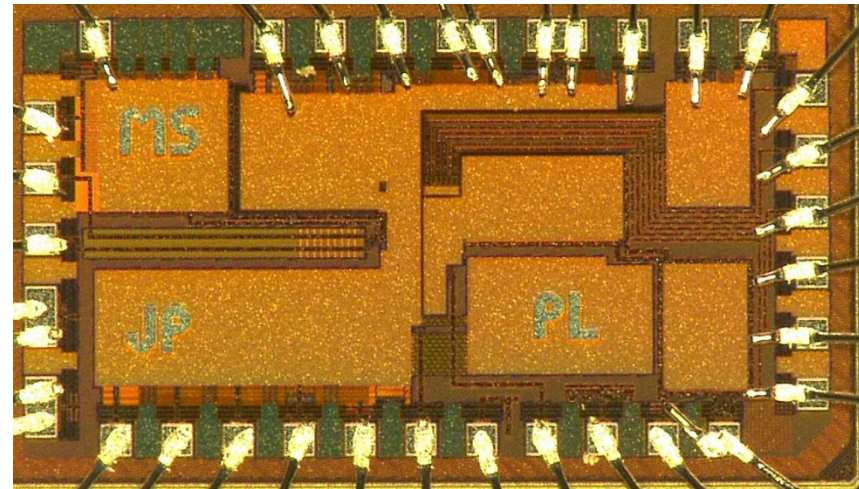


Measurements



Measurements

Core area	156 μm x 256 μm
Resolution (bin)	4.8 ps – 14 ps
Power consumption	4.2 mW – 2.4 mW
Dynamic range	6 bit
Supply voltage	0.9 V – 1.2 V
Sample rate	150 MSa/s
Technology	40nm CMOS



Conclusion

- Single shot TDC fabricated
- 4.8 ps resolution
- Extended startup speed
- SEE recovery improvement
- PFD and BBPD combination