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A Radiation Hardened TDC with < 10 ps Resolution and Improved Recovery Time from Single Events in 40 nm CMOS

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A radiation hardened Time-to-Digital Converter (TDC) has been designed with < 10 ps single-shot resolution using resistive interpolation. The TDC uses a DLL based control loop to calibrate gate delays to a reference clock. The control loop uses a novel low bandwidth Bang-Bang phase detector in combination with a high bandwidth dead-zone PFD for fast recovery after single-event strikes. The Bang-Bang phase detector has internal self-calibration for total dose radiation hardening. Finally an adapted flip-flop is used in the time capture registers that has no data dependent delay to improve overall resolution.

Summary

Future upgrades to HL-LHC detectors such as ATLAS, CMS and LHCb require highly radiation tolerant ASICs with high time resolution in combination with low power. In this work a novel Time-to-Digital Converter (TDC) has been designed for this scope of applications in high energy physics. While advanced sub-micron technologies have improved total dose resistance, single-event tolerance degrades drastically in these nodes. Therefore the TDC has a recovery circuit to improve single event recovery time after a strike has occurred. Nevertheless, total dose radiation effects cannot be neglected for these small time-resolutions. In order to harden the design for total-dose effects and improve overall robustness, a self-calibration technique is proposed to maintain the pre-rad resolution.

In DLL based TDCs, single event strikes can disturb the control loop from the locking point. Each time an event occurs, the loop must recover to this operating point. In a traditional phase-frequency detector (PFD) based loop, high charge-pump currents improve loop recovery time but have the problem of static phase offset (SPO) due to mismatch currents in the charge pump. The offset can only be reduced by reducing the reset time or intrinsically reducing mismatch by using larger devices. Bang-bang phase detectors in combination with a charge pump have no SPO problem due to the charge pump because they operate continuously. A trade-off has to be made between control voltage ripple (low current) and loop speed (high current). To alleviate this trade-off, a combination of a bang-bang phase detector and a PFD with dead-zone is used. The PFD has a high loop speed and is used to recover from a single-event strike. Close to locking range, the PFD enters dead-zone and the bang-bang phase detector takes over the control with a low current charge-pump to achieve low control voltage ripple.

While the PFD improves recovery time of the loop, irradiation can alter the clock-to-data delay of the flip-flop used in the bang-bang phase detector resulting in SPO. A novel self-calibration technique is proposed based on correlated double sampling to completely remove SPO in the bang-bang detector. An adapted flip-flop is used in this detector to reduce hysteresis from the data dependent delay to improve loop performance.

The 17 stage delay-line of the TDC locks on a reference clock of 2 Ghz which is interpolated 5 times to achieve 5.8 ps resolution. The use of a self-calibrated bang-bang phase detector reduces SPO errors below 1.2 ps (worst-case), depending on buffer mismatch. The TDC is designed in 40 nm TSMC CMOS with a core area of 0.0265 mm^2 and core power consumption (excluding IO buffers) of 3.9 mW. First experimental results are expected in july 2014.

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