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Low power Analog Digital Converter for a Silicon Photomultiplier Readout ASIC

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We present an ADC designed in the UMC 0.18um CMOS technology. It will be used in the SiPM analog front-end "KLauS" developed for the analog hadronic calorimeter at ILD. Key parameter in this application is an extremely low power consumption of the front-end electronics. For quantization of the energy depositions, a 10-bit resolution is required. For calibration purposes, a 12-bit quantization is used. A successive approximation register split capacitor array structure is chosen to minimize the DC power consumption. A peak sensing block reduces the sampling rate. Design details and simulation results will be presented.

Summary

The presented ADC will be integrated into the previously developed analog readout front-end for Silicon Photomultipliers "KLauS", which has been developed for the analog hadronic calorimeter (AHCAL) at a future linear collider experiment.
To avoid the necessity for cooling infrastructure in the calorimeter, an extremely low power consumption is required for the front-end ASICs. The upper limit for the power consumption is set to 25uW for a full channel including front-end and ADC. This requirement can be met by using power pulsing schemes with a duty cycle of 1%, in accordance with the bunch train structure foreseen at the ILC.

For the proposed ADC, a successive approximation register (SAR) ADC structure is chosen. By using a capacitive DAC array, the block can have no DC power consumption. Additionally, the digitization rate is minimized by only sampling the pulse height information of events triggered by the analog front-end. Accordingly, the structure promises a low power consumption at the expected channel trigger rates.

A 10-bit resolution is sufficient for the measurement of the scintillation light generated by minimum ionizing particles in the active cells of the detector and can be implemented without additional calibration methods. However, for detector calibration purposes, also high resolution single pixel spectra of the Silicon Photomultipliers have to be recorded. This operation mode requires a quantization resolution of 12 bit, and can be implemented in the ADC by amplification and digitization of the residual error using an additional pipelined SAR ADC block.
Monte-Carlo simulations suggest a differential nonlinearity due to random mismatch of 0.3LSB for 10-bit operation and a DNL of 0.4LSB for ADC digitizing in the high resolution 12-bit mode.
A redundancy error check method is implemented to suppress possible disturbances from digital switching noise by a factor of 8.

In addition, a peak-sensing track&hold block has been designed to be implemented in front of the ADC. The voltage level at the pulse maximum is held and then converted, allowing to reduce the required sampling frequency to the order of MHz. Accordingly, only relatively soft demands have to be put onto the dynamic parameters of the digitization stages.
The simulated error of the peak sensing was found to be less than 1mV for peak amplitudes ranging from 10mv to 1V at a supply voltage of 1.8V.
The total power consumption of the full ADC chain is less than 400uW for an event rate of 1MHz without applying any power pulsing techniques.

The ADC will be submitted in September 2014. We show design details and simulation results of the SAR ADC and the peak sensing block.

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