Thermal Analysis of the proto-VIPRAM2D Chip

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Introduction

In an HEP experiment, tracking the accurate paths of any particles generated by the interaction is the main function of the Silicon Vertex Trigger (SVT). In most triggers, the interaction point is surrounded by a SVT with several circles of detectors. The high-energy particle generated by an HEP experiment goes through all the layers surrounding the center of interaction. When a particle hits the bin in a layer, the time and location information of this event would be recorded by the detector in each layer and transmitted by a data bus to the associative memory for post-processing.

Future HEP experiments searching for rare processes need to address the demanding challenges of fast pattern recognition in triggering as the detector hit density becomes significantly higher. To address the challenges, Fermilab is leading the project on using 3D integration to develop Vertically Integrated Pattern Recognition Associative Memory (VIPRAM) to significantly advance the state of the art.

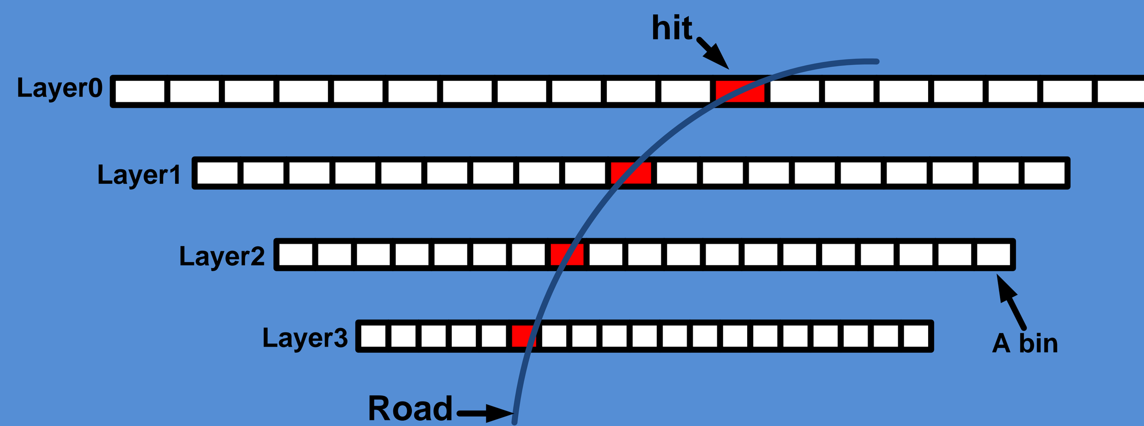

Fig. 1. A road in SVT

VIPRAM

The VIPRAM can detect the road occurring in the trigger by its pattern matching function. It is based on Content-Addressable Memory (CAM) cells. The proto-VIPRAM2D is laid out in a way which can easily be updated to the 3D version in future.

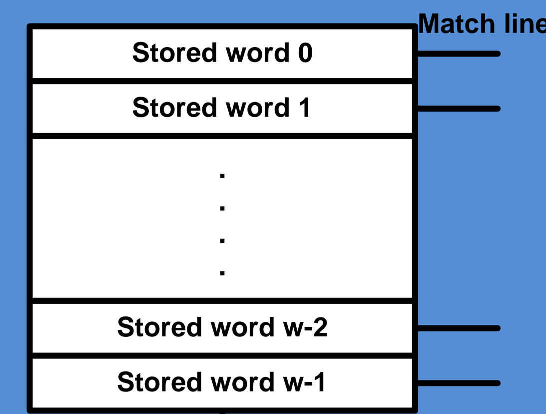

Fig. 2. Simplified structure of CAM system

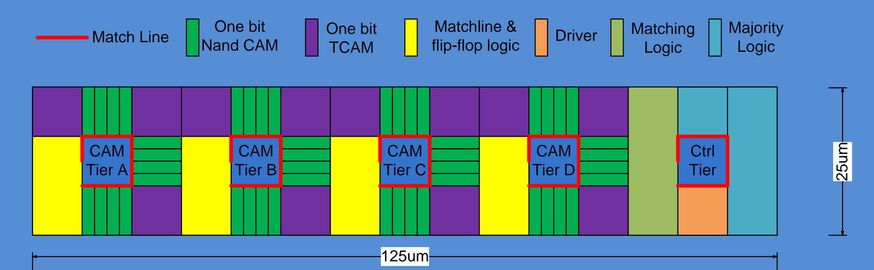

Fig. 4. Layout of one pattern of proto-VIPRAM

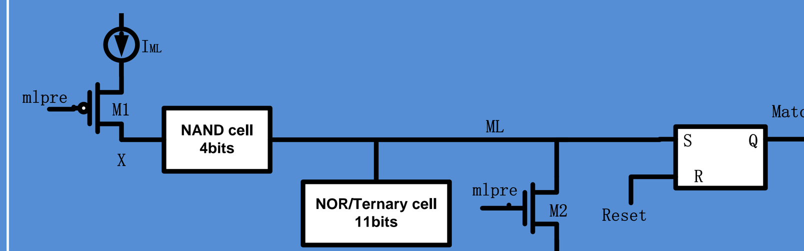

Fig. 3. CAM word schematic

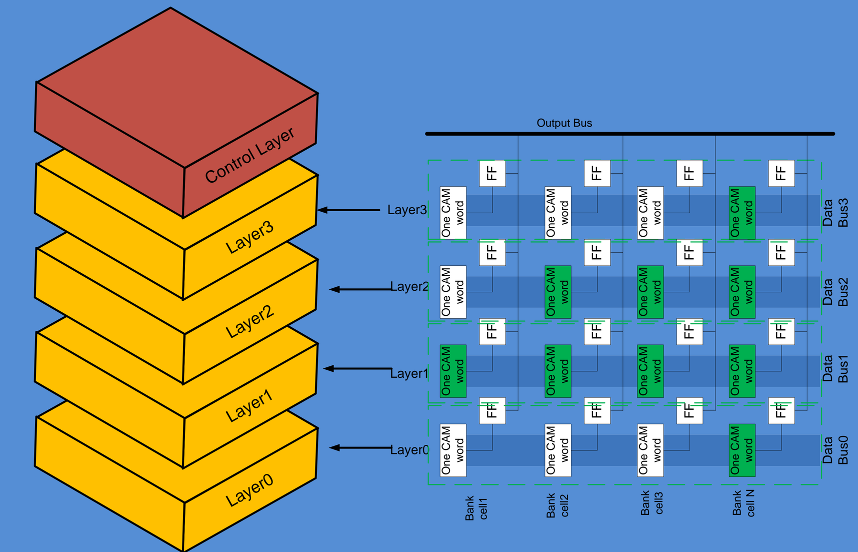

Fig. 5. Architecture of 3D VIPRAM

Thermal Modeling and Simulation

In the proto-VIPRAM, there are 32 patterns in one row and 128 rows for the entire chip, so there are 4096 patterns totally. The size of the CAM core is 4000 μm × 4480 μm. Each CAM cell in VIPRAM has a size of 25 μm × 35 μm and is treated as a single power source. A layered model is built to simulate the thermal effects from package substrate and PCB board.

HotSpot is chosen as the thermal analysis tool for its good trade-off between simulation speed and accuracy, by taking advantage of the regular layout in VIPRAM.

The verification steps are as follows:

Step1: Uploading all stored data into VIPRAM;

Step2: Setting certain CAM cells to be the all-bits matched case;

Step3: At the end of comparing operation (one clock period), resetting all of the match lines.

From the Spice simulation, the minimum clock period for VIPRAM is 7 ns and the corresponding power of CAM and logic cell is 30 μW and 10 μW respectively. The power information and power source location information are given to HotSpot for thermal analysis. The scenarios to activate different amount of power sources at different locations are simulated.

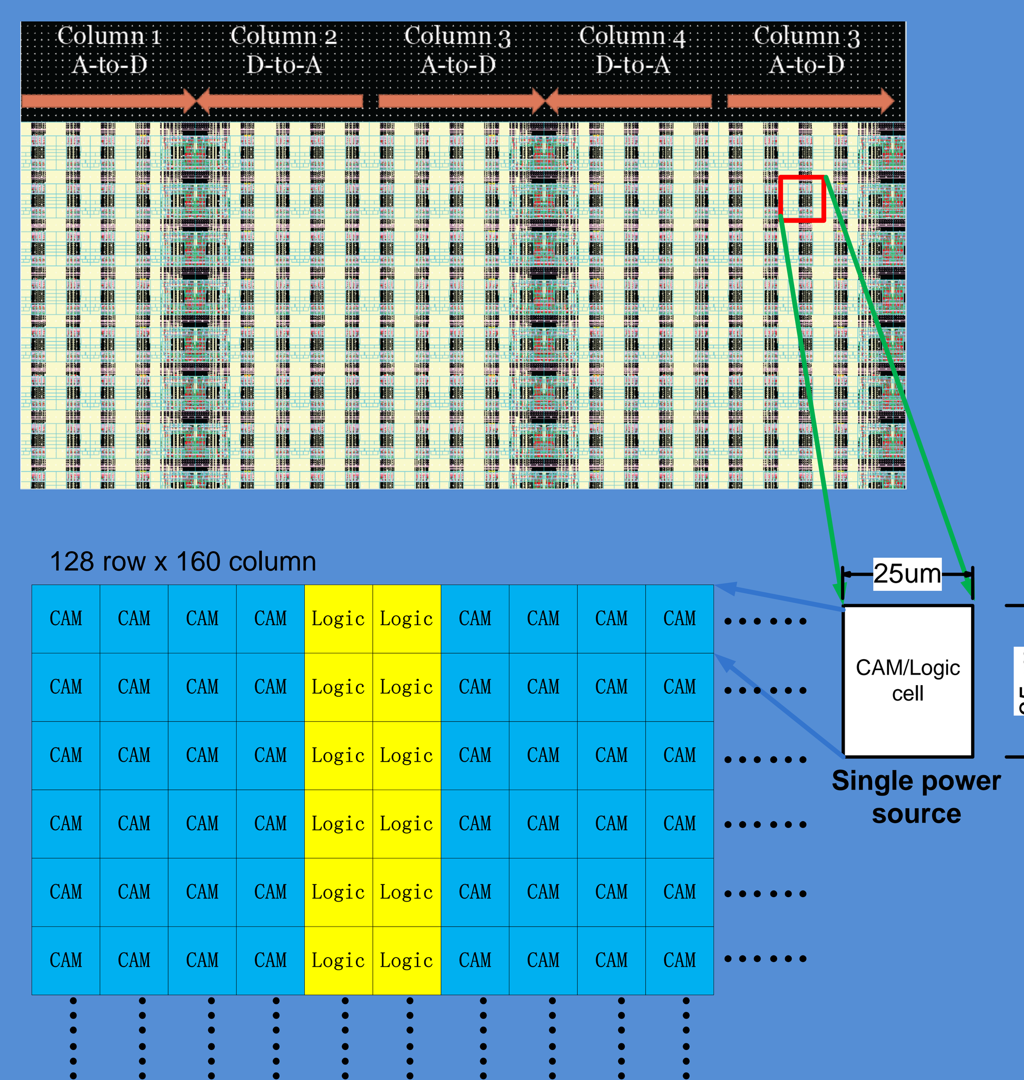

Fig. 6. Block model of power source for proto-VIPRAM

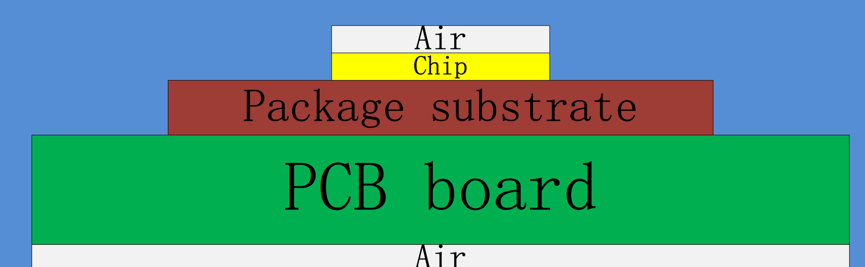

Fig. 7. Layered model of proto-VIPRAM

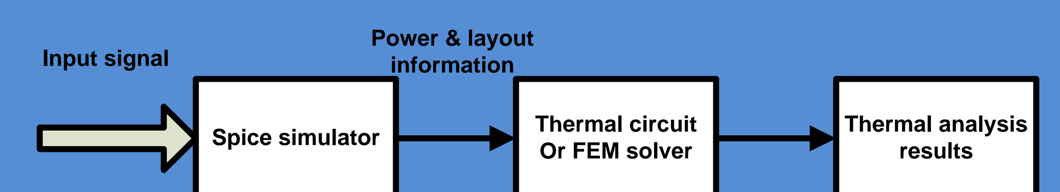

Fig. 8. General thermal simulation flow

Thermal Analysis Results

CAM bank thermal simulation results

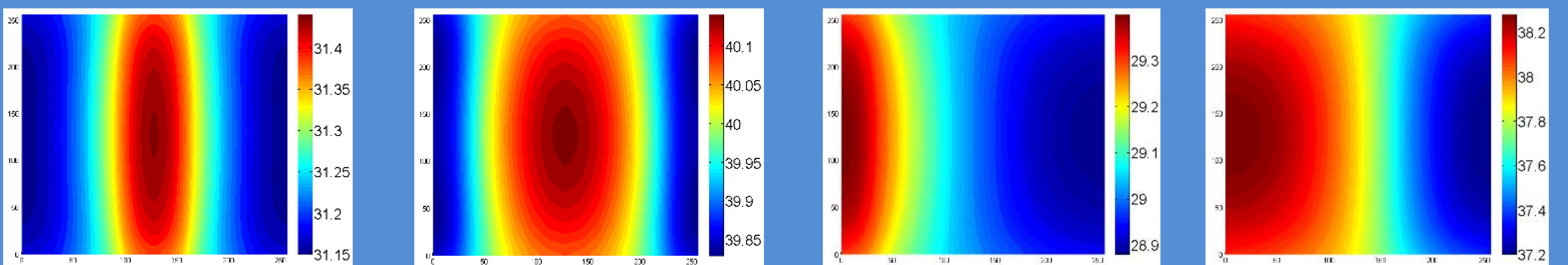

Fig. 9. (a) with 40 columns in the center activated (ΔT = 0.25 ℃) (b) with 120 columns in the center activated (ΔT = 0.25 ℃) (c) with 20 columns on the left activated (ΔT = 0.46 ℃) (d) with 100 columns on the left activated (ΔT = 1 ℃)

Full chip thermal simulation results

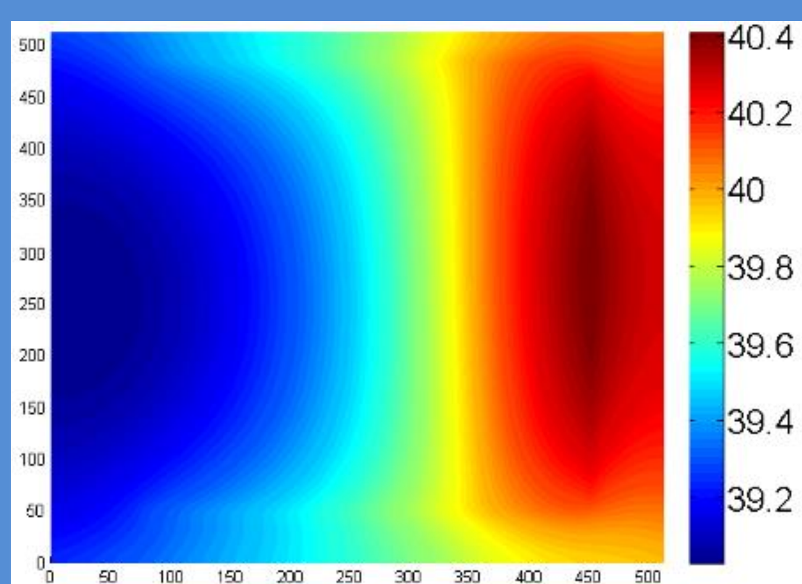

Fig. 10. Full chip simulation results

with 100 columns on the right activated (ΔT = 1.2 ℃)

From the analysis results, the scenarios when CAM cells on the side are activated have larger temperature variations comparing to the cases where same number of CAM cells in the center are activated. The full chip thermal simulation result shows 1.2℃ temperature variation in the proto-VIPRAM chip.

Conclusion

A sub-circuit-block level thermal simulation approach is proposed for the thermal analysis of the proto-VIPRAM chip. The method treats each CAM cell as a unit heat source. This approach significantly reduces the simulation time and computing resources while providing efficient and accurate thermal/temperature simulations in both 2D and 3D IC scenarios.