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Thermal Analysis of the Proto-VIPRAM2D Chip

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Thermal analysis has been essential in designing reliable IC. This becomes even more critical when multiple thin dies are stacked together to form a 3D integration. This paper presents our latest work on thermal modeling, analysis, and simulations on the prototype Vertical Integrated PRAM (proto-VIPRAM2D) chip. We proposed a sub-circuit-block level thermal simulation approach using Fourier heat flow model, where one CAM cell is used as a unit heat source. This approach significantly reduces the simulation time and computing resources while providing efficient and accurate thermal/temperature simulations in both 2D and 3D IC scenarios.

Summary

Future HEP experiments searching for rare processes need to address the demanding challenges of fast pattern recognition in triggering as the detector hit density becomes significantly higher. To address the challenges, Fermilab is leading the project on using 3D integration to develop Vertically Integrated Pattern Recognition Associative Memory (VIPRAM) to significantly advance the state of the art. While 3D offers many advantages in terms of pattern density and processing speed, one major concern is its potential thermal issue when multiple ICs are stacked together with limited heating dissipation path, which may cause chip failure. It is essential to build accurate and efficient thermal analysis model and simulation methods to ensure there are no thermal issues before the ICs are put into 3D.

This paper presents our latest work and results on thermal modeling, analysis, and simulation on proto-VIPRAM2D chip. The proto-VIPRAM2D is a 2D prototype with all building blocks designed to be fully compatible and ready for 3D stacking. It consists of 16,384 Content Addressable Memory (CAM) cells with space reserved for future TSV implementation for vertical integration. (The proto-VIPRAM2D chip design and performance results will be described in another abstract at TWEPP.) The challenges in thermal simulations on a chip with such large number of transistors are the high computation complexity and prohibitively long simulation time if the simulations are performed on a fine scale of transistor level. We propose a sub-circuit-block-level thermal simulation approach using Fourier heat flow model, where one CAM cell instead of a single transistor is used as a unit heat source. This approach significantly reduces the simulation time and computing resources, providing efficient yet accurate thermal/temperature simulations. In our proposed thermal model, the silicon layer consists of 16,386 heat sources (as opposed to or millions of heat sources on a micro-scale device level simulations, or a few heat sources in a more macro-scale level simulations). This strikes a good tradeoff between simulation accuracy and simulation time. In addition, each material layer is modeled including the silicon die, thermal interface layer, heat spread layer, package substrate and PCB test board. Due to low power of each CAM cell and heat spread material in the packaging, simulations predict rather small temperature rise and small variation across the proto-VIPRAM2D chip with various hit rates. To facilitate the thermal measurement of the chip using an infra-red camera in the future, we simulated the temperature distribution without the thermal interfacing material or heat spread. The input patterns that could cause the maximum temperature variation across the chip for measurement have been proposed and verified. Moreover, a preliminary 3D thermal model of VIPRAM consisting of 4 CAM tiers plus one control tier is also developed and simulated. Thermal simulations of such 3D VIPRAM are performed under different scenarios to evaluate the heat/temperature distribution. The proposed modeling and analysis methods for thermal issues can be also used in other chips in the HEP application.

Authors: HOFF, Jim (Fermi National Accelerator Lab. (US)); GUI, Ping (SMU); ZHANG, Tao (SMU); LIU, Tiehui Ted (Fermi National Accelerator Lab. (US)); XIA, Wenbo (SMU)

Presenter: ZHANG, Tao (SMU)

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