A 12GHz Low-Jitter LC-VCO PLL in 130nm CMOS

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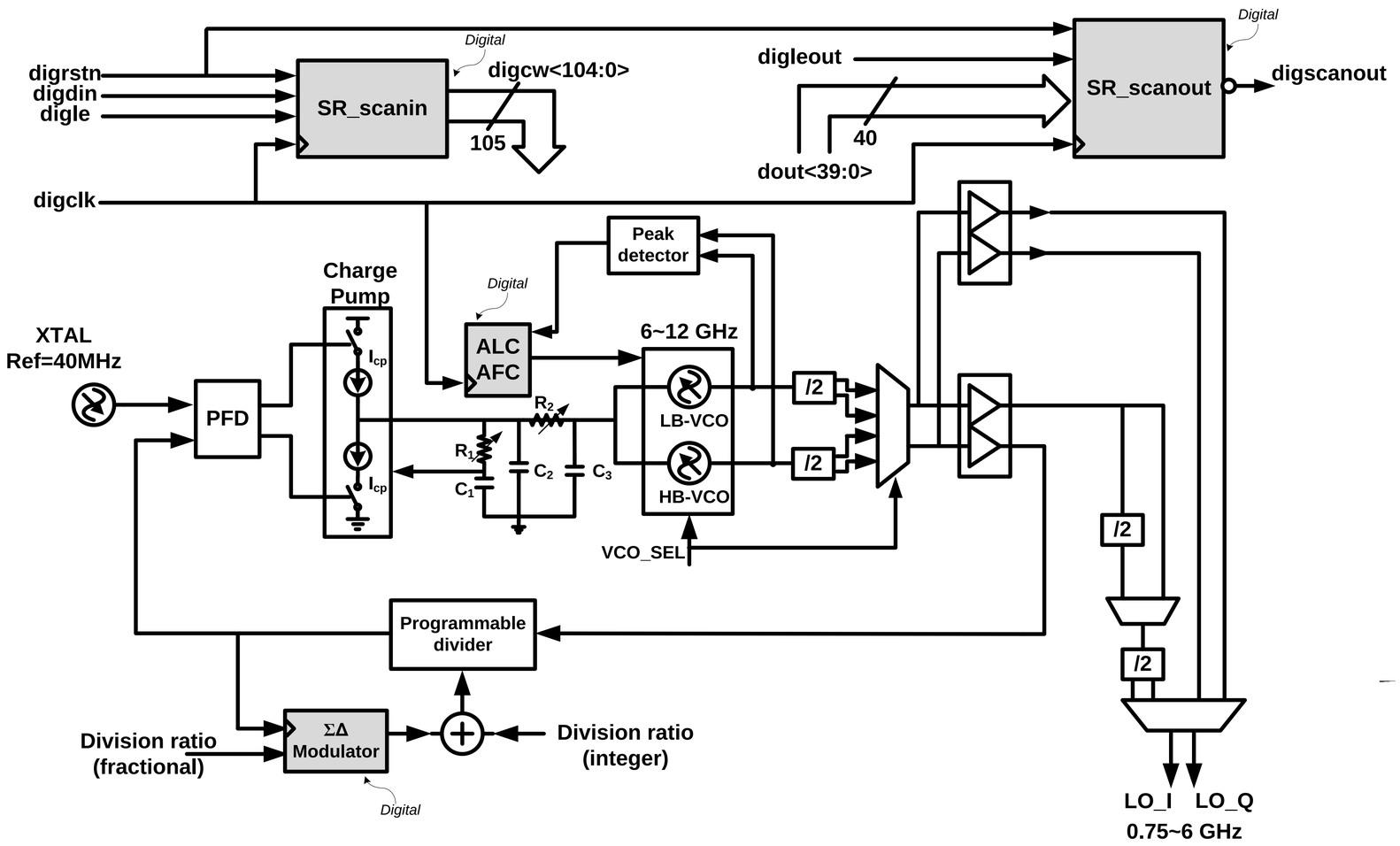
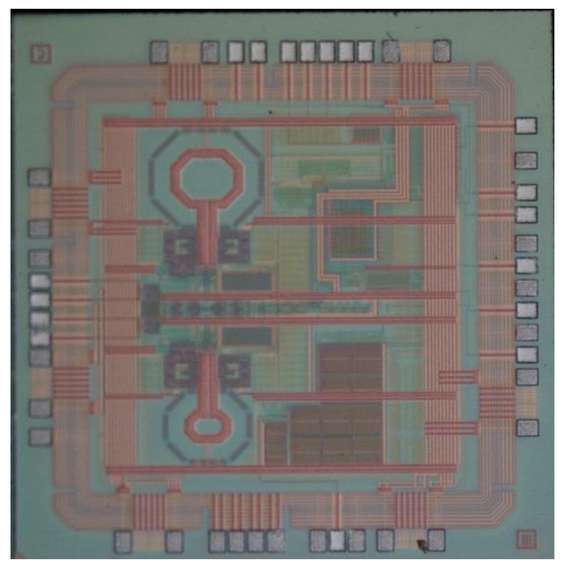
Introduction

- As CMOS technology moves to smaller feature size and lower supply voltage, it becomes increasingly difficult to produce a low-jitter clock source.
- The problem is further compounded since the PLL needs to cover a wide tuning range to compensate the radiation-induced frequency drift.
- This poster presents a low-jitter LC-VCO PLL in 130nm CMOS technology [1] and the SEE testing results
- The PLL covers 6~12GHz tuning range with 370ps RJ_{RMS} performance
- The SEE testing is performed with a neutron beam at Los Alamos National Laboratory and no frequency disturbances are found over the testing period.

Wideband low-jitter LC-PLL



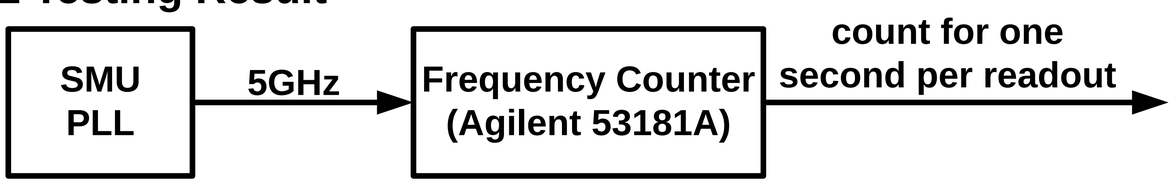
PLL block diagram



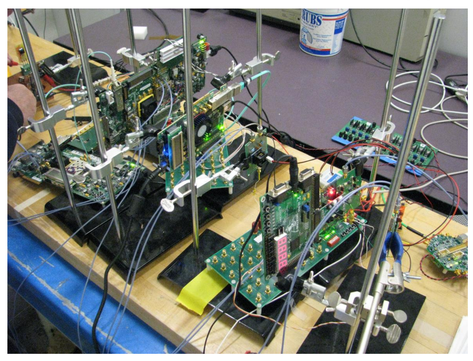
Die photograph

- PLL works in either integer-N or fractional-N mode.
- LC oscillators are chosen because of its low noise performance.
- NMOS negative trans-conductance is adopted due to its lower parasitic for achieving a wide tuning range.
- Two LC-VCO cores covering an octave frequency from 6GHz to 12GHz. The two VCOs have similar topology and capacitor array but different inductances.
- The PLL loop bandwidth can be optimized to tradeoff the in-band and out-band noises.

SEE Testing Result

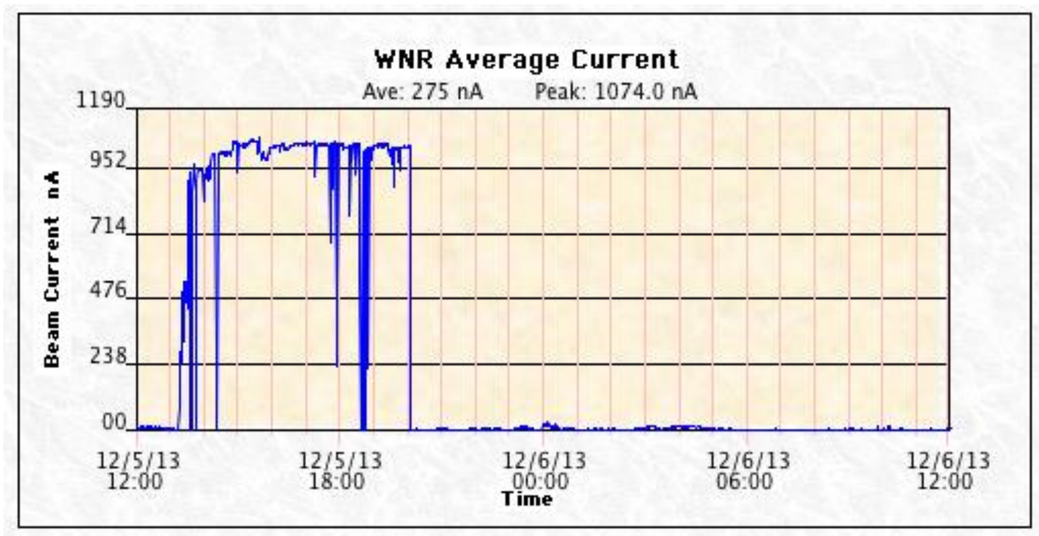


Block diagram of testing setup

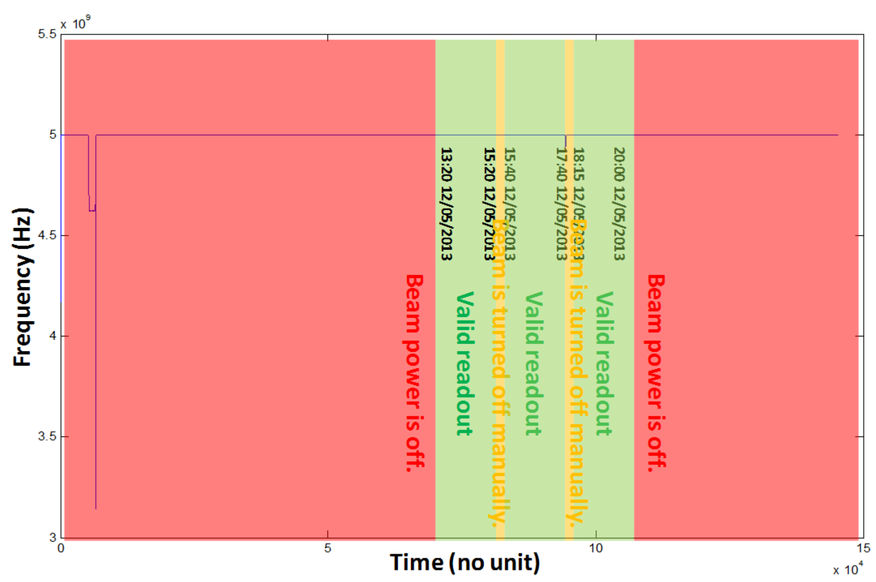


Photograph of PLL board under test

- SEE test in LANL
- Use frequency counter to readout PLL frequency with resolution of 1Hz
- DUT distance is 96.5 inches
- Due to the beam facility problem, the valid testing time is about 7 hours
- During the valid testing time no frequency disturbance is found at the readout of frequency counter



Beam activity during the testing time



No frequency disturbance found during the testing

Summary of the Proposed PLL Performance

	This work
Technology	130nm CMOS
Supply voltage	1.2V
Frequency range	5.6 to 13.4GHz
VCO cores	2
Tuning range per VCO core	47%
Divider ratio	150 to 300
VCO phase noise Δf=1MHz	-122dBc at 6GHz/2 -118dBc at 8GHz/2 -119dBc at10GHz/2 -116dBc at 12GHz/2
Random jitter (RMS)	0.365ps
Measured temperature range	-40°C to 85°C
Power	50.88mW
Area	0.8mm^2

Reference

- [1] Yang You *et al.*, A 12GHz 67% tuning range 0.37ps RJrms PLL with LC-VCO temperature compensation scheme in 0.13μm CMOS, Radio Frequency Integrated Circuits Symposium, 2014 IEEE , pp. 101–104.

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