Contribution ID: **142** Type: **Poster**

A 12GHz Low-Jitter LC-VCO PLL in 130nm CMOS

Wednesday 24 September 2014 17:12 (1 minute)

This paper presents a LC-VCO PLL designed in 0.13μm CMOS technology for multi-data rate serial link applications. The PLL covers a 5.6GHz to 13.4GHz tuning range by using two LC-VCO cores while remaining locked from -40℃ to 85℃. At 25℃, the PLL has a RMS random jitter (RJrms) of 0.37pS at 11.44GHz. The integrated jitter is less than 0.7pS. The PLL consumes 50.88mW of power from a 1.2V supply at 12GHz.

Summary

This paper describes a high-performance LC-VCO PLL that achieves a 5.6GHz to 13.4GHz tuning range and 370fS RMS random jitter in a 130nm CMOS technology supporting high speed serial link designs. As CMOS technology moves to smaller feature size and lower supply voltage, it becomes increasingly difficult to produce a low-jitter clock source. The reduced signal swing increases the sensitivity to both random and switching noises. The problem is further compounded since the PLL needs to cover a wide tuning range to compensate the radiation-induced frequency drift and jitter degradation.

The PLL works in either integer-N or fractional-N mode. The programmable resistors R1 and R2 in the loop filter (LF) along with the programmable charge pump (CP) current ICP provide control over loop bandwidth against different VCO gains (Kvco) and divider ratios (N). LC oscillators are chosen because of its low noise performance. The PLL loop bandwidth can be optimized to tradeoff the in-band and out-band noises. A standalone oscillator cannot simultaneously accomplish both a wide tuning range and satisfactory phase noise, thus the PLL is designed to have two LC-VCO cores covering an octave frequency from 6GHz to 12GHz. The two VCOs have similar topology and capacitor array but different inductances. NMOS negative transconductance is adopted due to its lower parasitic for achieving a wide tuning range. The inductors of the two sub-VCOs are optimized separately for high Q-factor as well as wide tuning range. Each VCO core consists of a single-turn inductor, an 8-bit binary weighted digitally-controlled MIM capacitor array (DCCA), accumulation-mode varactors, and a digitally-controlled automatic leveling control loop (ALC). Since the required negative transconductance varies with the oscillation frequency, the biasing current is made programmable to ensure the oscillator to operate at the edge of the current-limited regime for a maximum voltage swing without excessive waste of power. The DCCA ensures a sufficient overlap ratio between tuning bands in order to tolerate automatic frequency calibration (AFC) errors. The clock distribution network consists of buffers, divider-by-2 and multiplexer blocks to deliver the final clock signals.

The PLL is packaged in a QFN40 package. It has a total of 512 DCCA tuning bands and the measured frequency tuning range is from 5.6GHz to 13.4GHz. The overlap ratio between adjacent tuning bands is larger than 80%. The measured maximum VCO gain (Kvco) is about 550MHz/V. The RMS random jitter (RJrms) is measured to be 365fS at 5.72GHz divide-by-2 output at 25℃ The measured integrated jitter is less than 700fS over the entire tuning range. The PLL consumes 50.88mW from a 1.2V supply voltage at 12GHz at 25℃. SEE testing is performed with a neutron beam at Los Alamos National Laboratory and no frequency disturbances are found over the testing period. TID testing with X-rays is ongoing and results will be presented at the conference.

Authors: Mr HUANG, Deping (University Of Arizona); Prof. CHEN, Jinghong (University Of Houston, Texas); Mr YOU, Yang (Southern Methodist University)

Co-authors: GONG, Datao (Southern Methodist Univeristy); YE, Jingbo (Southern Methodist University, Department of Physics); LIU, Tiankuan (Southern Methodist University)

Presenter: Prof. CHEN, Jinghong (University Of Houston, Texas)

Session Classification: Second Poster Session

Track Classification: ASICs