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VIPRAM Architecture and Its Implementation: from 2D to 3D

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The VIPRAM approach has, from the beginning, attempted to increase pattern density and decrease power density through Vertical Integration. To mitigate issues implicit in adopting an emerging technology, a flexible architecture has been developed that can be implemented in either conventional or Vertically Integrated VLSI. This allows us to bring the system interface to maturity at an early stage while, at the same time, making steady progress towards the final VIPRAM solution. This is particularly important for Level 1 Tracking Trigger applications. The talk will cover the architecture, system interface and implementation that takes the design from 2D to 3D.

Summary

The numerous advantages of an Associative Memory-based track trigger are well established. Its primary limitations lie in pattern density and in readout speed for Level 1 trigger applications. A secondary challenge is to minimize power consumption. Vertical Integration is an emerging technology which offers dramatic improvements in all these areas. The overall objective of the VIPRAM project at this point is to make steady progress towards a final solution. This requires a strategic approach to architecture and layout that permits near term solutions in classical VLSI technology and long term solutions in aggressive Vertical Integration.
The flow of VIPRAM's tasks can be divided into two broad categories: 1) Pattern Recognition Associative Memory (PRAM), and 2) input/output and control (IOC). The former consists of CAM Cells, Majority Logic Cells, and pattern and critical signal distributions. This was the focus of protoVIPRAM2D, a 2D implementation of the 3D-compatible cells necessary for the final design. The details of this successful prototype are discussed in a different abstract. The IOC consists of data input handling, slow control, road match capture, sparsification, and road output. During operation, silicon data is sent to the VIPRAM followed by a unique End-of-Event signal. At the arrival of the End-of-Event, the road match capture logic in the IOC snaps a picture of the state of the PRAM, freeing the PRAM to begin collecting data for the next event, if necessary. The captured road match snap shot is sparsified, placed in a FIFO, serialized and driven off-chip to the track fitting logic.
Design in Vertical Integration is, in a sense, the logical partitioning of functionality into a third dimension. For example, a generic CPU could be partitioned into memory, processor and IO. To make an architecture that can be either 2D or simple 3D or more aggressive 3D, the partitioning must also be adjustable so that its granularity can be changed to fit the desired implementation with the present available technology in a cost effective way. The PRAM structure, intrinsically, is adjustable in the 3rd dimension from the full road level down to the individual CAM level. The IOC, being logically separable from the PRAM, can be implemented on its own tier as well, leaving more space for a high performance system interface.
This talk will cover the new VIPRAM implementation in which a PRAM tier is only partitioned to the road level and the IOC tier is targeted to a Level 1 Track Trigger with the goal to bring the system level interface to maturity. This is fully compatible with our long-term goal of high-density 3D stacking while, at the same time, achieving our near-term need of a functional chip for a CMS Level 1 Tracking Trigger demonstration.

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