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Pulsar II: An FPGA-based Full Mesh ATCA Processor Board

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The Pulsar II is an FPGA-based full mesh ATCA processor board capable of creating a scalable architecture abundant in flexible, high bandwidth interconnections. The resulting full mesh interconnection among FPGAs is a natural fit for spatial and time multiplexed data processing. The design has been motivated by silicon-based tracking trigger needs for the LHC experiments. Near term applications are the ATLAS FTK Data Formatter, which requires spatial data multiplexing, and the CMS Level-1 tracking trigger vertical slice demonstration, which also demands extensive time multiplexing. In this talk we present the board design and performance study results.

Summary

The Pulsar II design has been motivated by silicon-based tracking trigger needs for LHC experiments. In this talk we describe our design and test methodology, board performance results and experience gained in the process.

Our first prototype, called the Pulsar IIa, has been designed around two Kintex-7 FPGAs. These FPGAs include many multi-gigabit serial transceivers (GTX) which are directly connected to the full mesh backplane fabric interface and to fiber transceivers located on a rear transition module (RTM). Each RTM supports I/O bandwidth of up to 400 Gbps bidirectional. Four FMC mezzanine cards are directly connected to the FPGAs over high speed LVDS lines. Mezzanine cards may be used for I/O expansion, system interfaces or for implementing parallel processing engines.

Leveraging the experience we gained through designing, building and testing the Pulsar IIa, we have designed the next generation board, the Pulsar IIb, which is now in the prototype testing phase. The new board design replaces the two Kintex FPGAs with a single Virtex-7 XC7VX690T FPGA. The serial transceiver count has increased to 80 channels, providing a significant bandwidth increase to the RTM, full mesh fabric and mezzanine cards. Much of the design effort has been focused on optimizing the channel performance at 10 Gbps across the backplane, RTM and mezzanine interfaces. The Pulsar IIb board has more than 1 Tbps (bidirectional) interface capability.

The Pulsar IIb has been designed for compatibility with common LHC developments. For example, the FMC mezzanine interface is fully compatible with the CERN TTC FMC card. We are adapting the CMS IPBus interface, which has been developed for uTCA applications, to the Pulsar II and testing with commercial ATCA switches. In addition, the Pulsar IIb is compatible with the LAPP IPMC mezzanine card being developed for Atlas.

The Pulsar IIb will soon be used as Data Formatter in the ATLAS Fast Tracker (FTK), which is a level-2 silicon-based tracking trigger. The Data Formatter system is an application where the full mesh backplane is used to share data among processing nodes. When one considers the many high bandwidth parallel data channels available in the full mesh backplane it also becomes apparent that the Pulsar IIb based architecture can naturally support sophisticated time multiplexed data transfer and processing schemes. An example of one such application is a proposed CMS phase 2 Level-1 tracking trigger vertical slice demonstration in the near future. Each trigger tower processor crate hosts an array of independent track finder engines. In this application the full mesh backplane is used to transfer time multiplexed event data to multiple track processing engines and

the Pulsar-II can host a bank of high-performance associative memory chips, providing a powerful solution to address the CMS detector's tracking trigger challenges for rapid recognition of charged particles. Furthermore, due to the inherent flexibility and scalability of this architecture the Pulsar IIb design may also find applications beyond tracking triggers, within and outside HEP.

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