A Low-Latency and Low-Overhead Encoder ASIC for the Serial Data Transmission in the ATLAS LAr Calorimeter Readout Upgrade

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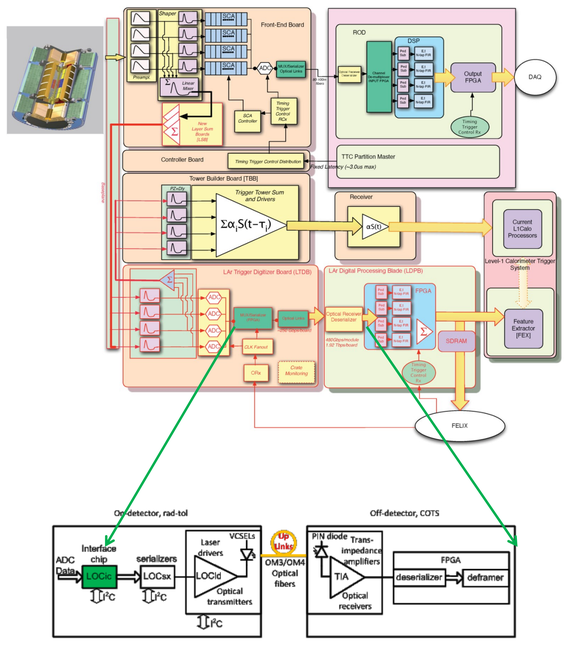
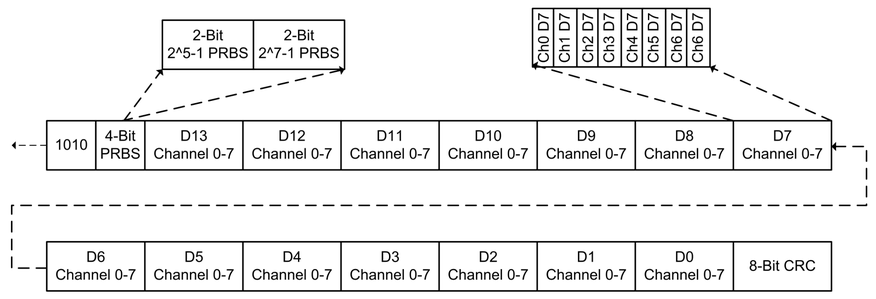
Introduction



- The ATLAS Liquid Argon calorimeter (LAr) Phase-I trigger upgrade calls for a data transmission rate of 204.8 Gbps for each front-end board (LTDB) [1].
- An interface chip, named as LOCic, is needed to encode the ADC data for following serializer.
- An low-latency and low-overhead data frame is proposed and verified.
- Implemented the encoder ASIC based on a commercial 0.25-μm Silicon-on-Sapphire CMOS technology for radiation-tolerance.
- Each encoder ASIC encodes 8 channel ADC at 40 MSPS.
- The latency of encoder is estimated to be less than 7 ns.
- The power consumption of the encoder ASIC is about 100 mW.
- The matched decoder firmware is implemented in an FGPA and used to test the ASIC.
- The current design is for TI ADS 5272 only [2].

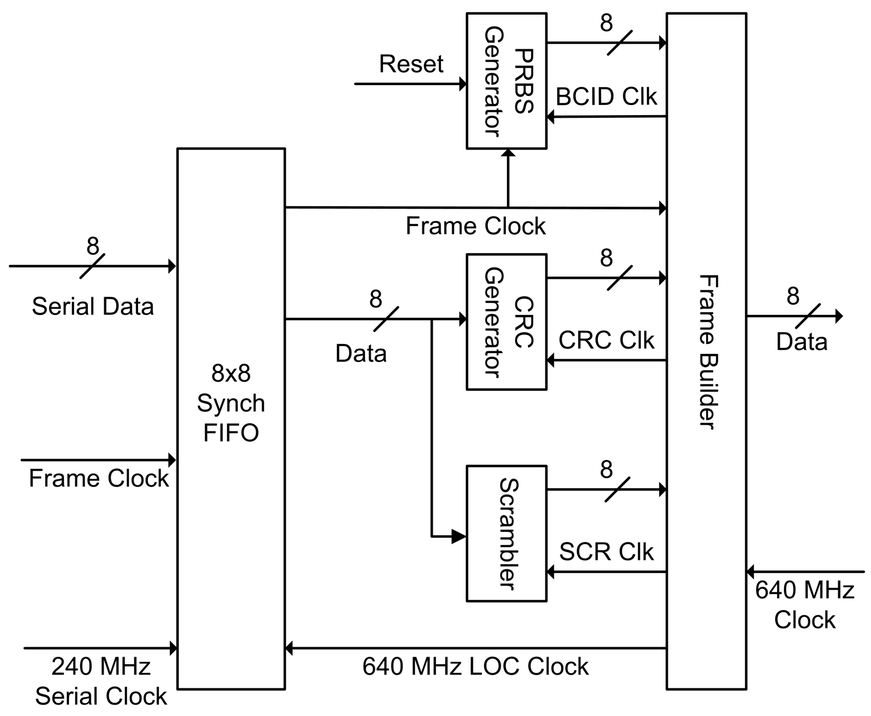
Data Frame Definition



- The frame length is 128 bits, include 112 bits user data, 8 bits frame header and 8 bits CRC code.
- Frame header identifier comprises of “0101” fixed code and 4-bit PRBS code.
- 4-bit PRBS code also carries 12-bit BCID information (period 3564), formed by 2-bit 2^5-1 and 2-bit 2^7-1 PRBS code
- 8-bit CRC code with the polynomial $x^8+x^5+x^3+x^2+x+1$ is attached to detect possible data corruption in the data transmission.
- The ADC data, not including the frame header and CRC code, is scrambled with a scrambler defined by the polynomial $1+x^{39}+x^{58}$ to keep DC-balance in serial data transmission [3].

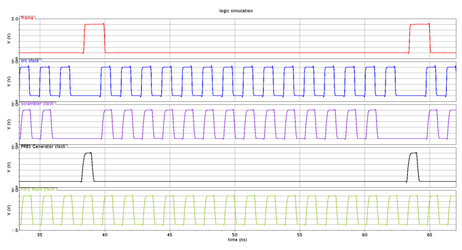
	8B/10B	64B/66B	LOCic
Overhead	25%+framing	3.125%+framing	6.25%
Framing included	No	No	Yes
BCID included	No	No	Yes
Latency of encoder (LHC clock cycle)	2.5	2 (+gearbox)	2
Decoder latency (LHC clock cycle)	4.5	4 (+gearbox)	4
Serial bit # needed to re-sync	30	4224 (min)	136

Encoder ASIC (LOCic) design

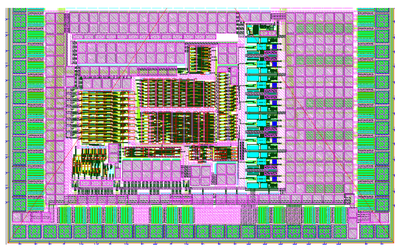


Encoder ASIC (LOCic) diagram

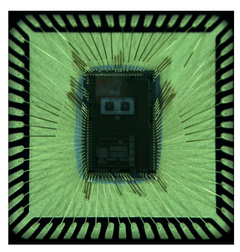
- The main components in the LOCic are driven by a 640 MHz clock. An Integrated Clock Gating (ICG) technique is used to align data and save power.
- A synchronous FIFO is implemented to receive the 8-channel ADC data at 480 MSPS per channel
- A PRBS generator is implemented to generate 4-bit code for each data frame period, 25 ns.
- The scrambler executes 14 times for 16 640-MHZ clock periods to scramble ADC data plus two 8-bit dummy data.
- The CRC generator executes 15 times to calculate 8-bit CRC code for 14-byte user data. A pipeline technique is used to break down the complicated calculation logic to achieve high speed without latency penalty.
- The Frame builder generates gated clocks for all other components and assembles data.



Gated clock signals

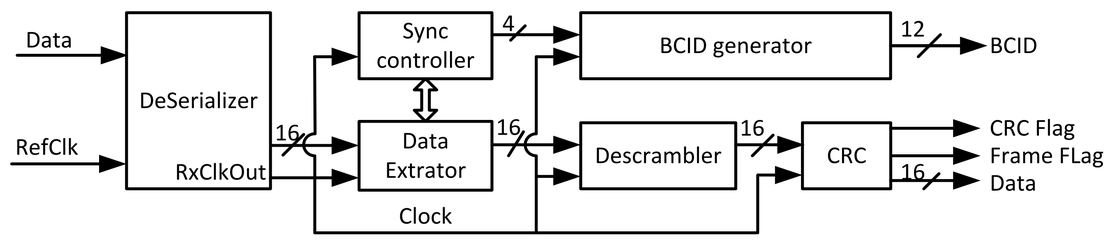


Layout of the ASIC



QFN packaged LOCic

Decoder and Test Firmware

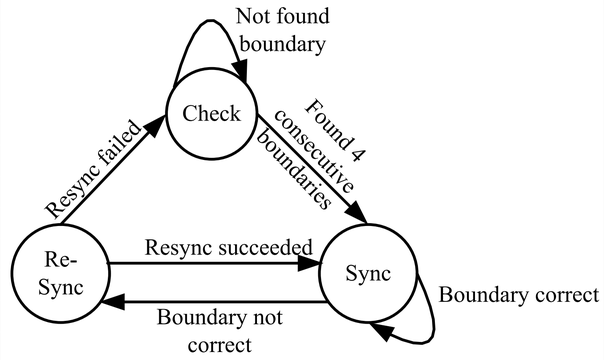


Decoder firmware diagram

- The receiver and test firmware is implemented in Xillix Kintex-7 FPGA
- The whole link system with LOCic has been tested successfully in lab; Irradiation test will follow.
- The deserializer is configured to be 16:1 and all function blocks are operated at 320 MHz.
- A synchronizing controller is designed to seek the frame header and monitor the link status. An elaborate synchronizing logic is implemented to recover the link when it gets lost.
- A corresponding descrambler recovers scrambled ADC data.
- A CRC generator calculates CRC code from descrambled data and verifies the data integrity.
- Full 12-bit BCID information is recovered from the received PRBS code in the frame header.
- Link status are generated for further process.

Function block		Latency (ns)	
		Kintex-7	ASIC + Kintex-7
	FIFO	3.1-6.3	1.6-3.1
TX	Scrambler & CRC gen	3.1	1.6
TX	Frame Builder	3.1	1.6
TX	Serializer	14.4	4.7
TX	Total	23.8-26.9	9.4-10.9
RX	Deserializer	28.5-31.4	
RX	Data Extractor	9.4	
RX	Descrambler	3.1	
RX	CRC Check	3.1	
RX	Total	44.1-47.0	
Total		67.9-73.9	53.5-57.9

Latency of the optical link



The state machine in synchronizing controller

Conclusion

- An encoder ASIC, LOCic, is design and fabricated for the ATLAS LAr Calorimeter front-end readout phase-I upgrade.
- The corresponding decoder has been developed and tested with the fabricated chip.
- The performance of the encoder ASIC achieves the design goal.

Acknowledgments

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References

1. Hucheng Chen, Readout Electronics for the ATLAS LAr Calorimeter at HL-LHC, the Technology and Instrumentation in Particle Physics (TIPP) conference, Chicago, U.S.A, June 9-14, 2011.
2. H. Takai *et al.*, Characterization of COTS ADC radiation properties for ATLAS LAr calorimeter readout upgrade, TWEPP, Perugia Italy, September 23-27, 2013.
3. IEEE802.3 specification (2008), clause 49.

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