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A Low-latency and Low Overhead Encoder ASIC for the Serial Data Transmission in ATLAS LAr Calorimeter Readout Upgrade

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We present the design and test results of a digital encoder ASIC, LOCic, for high-speed serial data transmission in ATLAS LAr calorimeter readout upgrade. This chip implements a low latency and low overhead line code. The user data is scrambled and encoded into a 128-bit data frame including CRC for error detection. The encoder overhead is 12.5%. A 12-bit BCID information is embedded in the frame header. The ASIC is manufactured with a commercial 0.25 μm Silicon-on-Sapphire process and tested to operate at 640 MHz with 7 ns latency.

Summary

The ATLAS LAr calorimeter readout phase-I trigger upgrade calls for a data rate of 204.8 Gbps for each front-end board (LTDB). This data will be transmitted over optical fibers to the back-end. The optical link transmitter side consists of a serializer ASIC (LOCx2) and a custom optical transmitter (MTx). LOCx2 receives data from the upstream ADC, prepares the data and pushes it to MTx which converts it to optical and launches it into a fiber. LOCic is the first function block in LOCx2 that frames and scrambles the parallel data. LOCx2 is being developed with a 0.25 micron Silicon-on-Sapphire CMOS technology which offers a digital library for circuits up to 100 MHz. We developed a method to push the clock of LOCic, a full digital circuit, to 640 MHz.

The front-end ADC is a 12-bit 40 MSPS ADC with a 640 MHz serial output. Each channel ADC outputs 12 bits data plus 2 calibration bits. The custom data frame comprises of 112-bit scrambled ADC data, 8-bit CRC code and 8-bit frame head identifier. The 112-bit user data accommodates 8-channel ADC. The attached 8-bit CRC can detect any 3 continuous bit-flip errors in the data frame. The 8-bit frame header, used to identify the frame boundary, includes 4-bit fixed code "1010"and 4-bit PRBS code. By combining the PRBS code from previous received data frames, the receiver side decoder extracts a 12-bit BCID information. This frame header also provides the capability to quickly re-synchronize the frame boundary if the serial data shift a few bits due to radiation.

The LOCic comprises of a synchronous FIFO, a CRC generator, a scrambler, a PRBS generator and a frame builder to composite the data. To reach the clock frequency of 640 MHz we adopted pipeline technique to simplify the circuit logic executed in each clock period, especially in the CRC generator with a limit of 8 XOR logic units in each step. The whole design is manually laid-out and the clock distribution is carefully aligned in post-layout simulation. LOCic has a latency of about 7 ns.

LOCic is tested at 640 MHz with a power consumption at about 100 mW. The 8-channle ADC data is emulated in a Kintex 7 FPGA evaluation board in the test. The decoder implemented in the FPGA board decodes the data frame built in LOCic. The decoder identifies the data frame boundary correctly and the recovered ADC data passes the CRC code check. The BCID count is also extracted as we expected.

To summarize, we have implemented an encoder ASIC, LOCic, for high-speed serial data transmission in ATLAS LAr calorimeter readout upgrade. The chip meets the design goals in the test. The latency of the encoder is about 7 ns and the overhead is 12.5%. A 12-bit BCID information is transmitted without extra bandwidth cost.

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