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The ToPiX v4 Prototype for the Triggerless Readout of the PANDA Silicon Pixel Detector

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ToPiX v4 is the prototype for the readout of the silicon pixel sensors of the Micro Vertex Detector for the PANDA experiment. ToPiX provides position, time and energy measurement of the incoming particles and is designed for the trigger-less environment foreseen in PANDA. The prototype includes 640 pixels with a size of 100x100 um2, a 160 MHz time stamp distribution circuit to measure both particle arrival time and released energy (via ToT technique) and the full control logic. The ASIC is designed in a 0.13 um CMOS technology with SEU protection techniques for the digital parts.

Summary

PANDA is one of the main experiments at the future FAIR facility under construction near the GSI research center at Darmstadt, Germany. It aims to the study of the antiproton-proton and antiproton-nucleus annihilation reactions.
The Micro Vertex Detector (MVD) is the innermost part of the PANDA apparaturs and consists of both silicon pixel and silicon strip detectors, placed in barrels around the interaction point and in disks in the forward direction. The two innermost barrel layers and the central part of the forward disks will be made of Silicon Pixel Detectors (SPD). Therefore the SPDs will have to cope with the maximum particle density (up to 6.1 MHz/cm^2); the space resolution requirements therefore limits the pixel size to 100 μm x 100 μm. Moreover, the PANDA apparatus will not provide a hardware trigger signal, thus requiring a precise time stamping of the events (1.9 ns r.m.s.) and a high data bandwidth. Deposited energy measurement is also a requirement for the SPD readout electronics.
In order to cope with these challenging requirements, an ASIC-based solution for the readout of the PANDA SPD is under development. The ASIC, named ToPiX, will consist of a matrix of 116x110 cells, thus covering an active area of 1.32 cm^2. The pixel matrix is organized in 55 double columns, each with independent readout logic and local buffering. An end of column control logic provides both data transmission via double data rate serializers and control and configuration informations. The master clock frequency is 160 MHz.

A new reduced scale prototype, named ToPiX v4, has been designed and is currently under test. The prototype is based on a 640 cells pixel matrix, with a layout compatible with the previous prototype version. The operating clock frequency has been increased from 50 to 160 MHz, and a number of modifications have been made in order to increase the linearity for charges below 2 fC, to linearise the

comparator threshold control DAC and to improve the radiation tolerance with respect to both Total Ionizing Dose (TID) and Single Event Upset (SEU) effects.
In particular, a combination of DICE cells, Hamming encoding and TMR redundancy has been implemented in the pixel cell area where space constraints make the redundancy more critical.
TID and SEU tests will be performed in July-August to assess the effectiveness of these improvements.
Differential SLVS I/O links have been used to interface the chip. The ToPiX v4 is designed to be compatible with the GBT transceiver under development at CERN for data and slow control signal transmission.

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