Versatile ASIC for L0 Triggering in Cherenkov Telescopes

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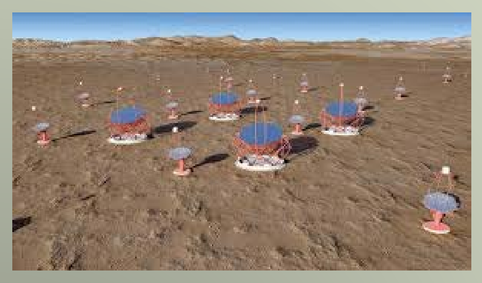
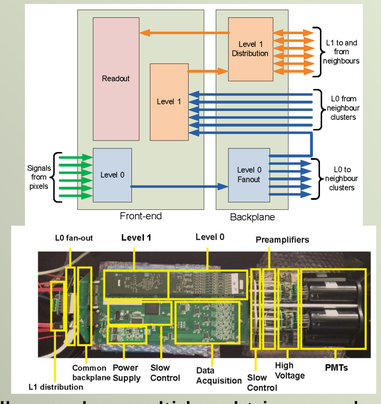
Cherenkov Telescope Array

The future international very high energy gamma ray observatory, the Cherenkov Telescope Array (CTA) [1], will consist of an array of 50-100 dishes of various sizes. Each telescope will have a Kpixel camera with photo-detectors installed in its focal plane and the associated front-end electronics. More than 100K channels in the arrray.

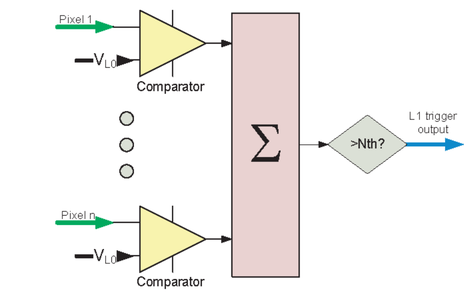




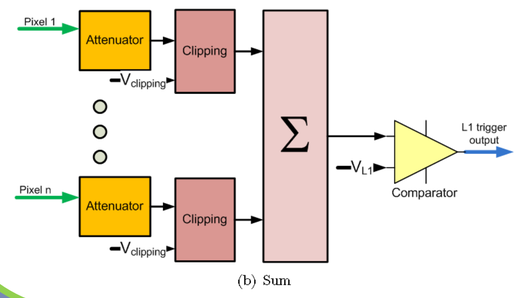
- Arrays of Cherenkov telescopes typically employ multi-level trigger schemes to keep the rate of random triggers from the night sky background low.
- The trigger chain within a telescope may follow a digital, or analogue path.
- In H.E.S.S., Magic and VERITAS, analogue schemes are used
- For CTA several approaches for both options are under investigation.

The analog trigger system

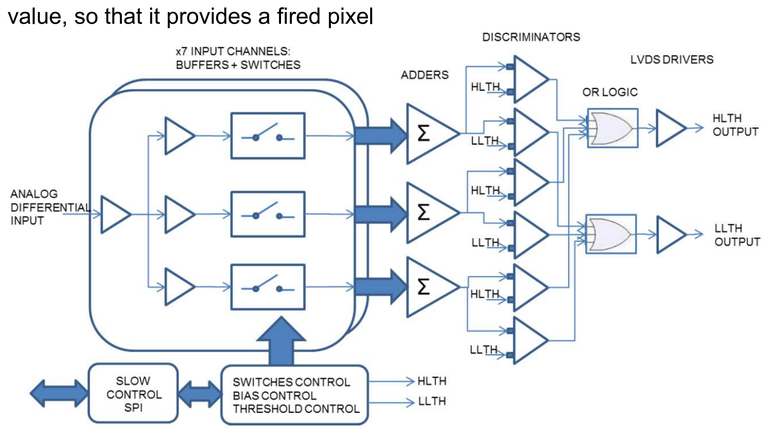
- Level 0 stage processes analog signals of individual pixels in a cluster
- Two concepts proposed
  - Sum trigger: analog clipped sum of the signals of the pixels is raised to the Level 1
  - Majority trigger: signals are compared to a threshold value, so that it provides a fired pixel account to the Level 1 stage



(a) Majority



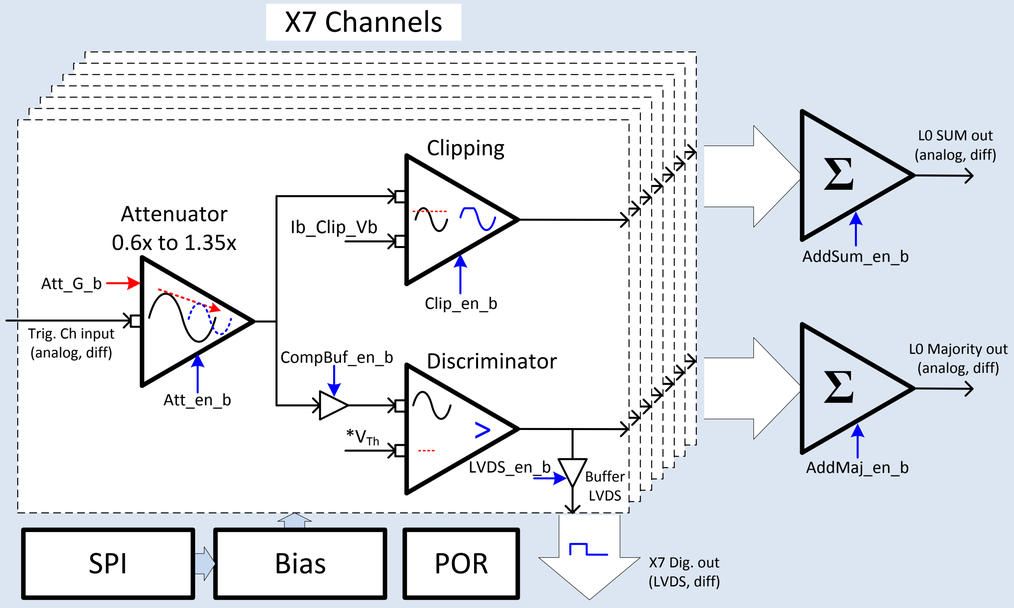
(b) Sum



- At the Level 1, the analog combination of the Level 0 signals (both in the Majority and Sum modes) for all possible compact regions of a geometrical size given within the hardware limits is examined.
- This combination roughly consists of the analog addition of the Level 0 signals for different geometrical patterns.
- The Level 1 stage takes the decision to trigger the camera if the output of the combination in any part of the camera exceeds a given threshold.

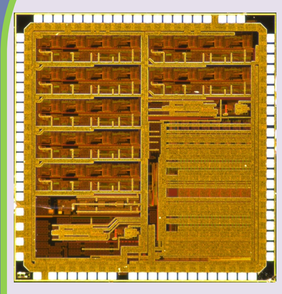
ASIC for Level 0 trigger

- The two different Level-0 approaches have been included in the L0 ASIC: the Majority trigger and the Sum trigger concept.
- Each differential input goes through an attenuator circuit (programmable in the slow control interface) to the two level-0 trigger approaches in order to compensate for photosensor non-uniformity.
- The Majority trigger concept compares the signal from each pixel to a voltage threshold by using a discriminator circuit [2]
  - Each differential pair output of the discriminator is available as a LVDS output.
  - All the discriminator outputs are also internally added and are also available in an analog differential output.
- The Sum trigger clips the signals exceeding a given value in order to limit the influence of after pulses from the photo sensors.
  - Then, adds the signal from all pixels in the cluster and sends the resulting signal to the Level-1 decision subsystem by an analog differential output.

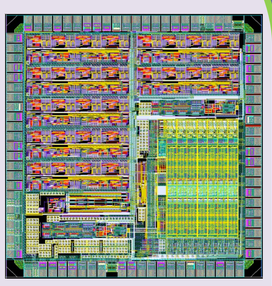


* Vth ➔ Configured by a 10 bits DAC (DacCode)

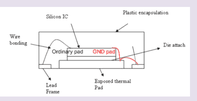
Technology



- Austriamicrosystems BiCMOS SiGe 0.35 µm technology
  - Compatibility with other CTA-Spain chips [3], [4]
- About 12 mm^2
- 7 Channels
- Majority & Sum trigger approach
- 7 LVDS digitized outputs
- SPI Slow Control Interface
- 30 samples packaged

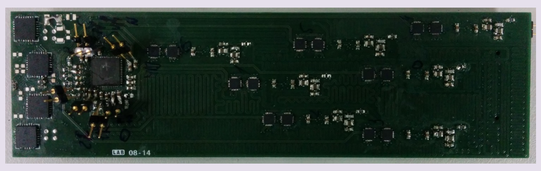


- Three different simultaneous operation modes
  - Sum trigger
  - Majority trigger
  - Discriminator outputs (7 outputs)
- Each subsystem of each channel can be set in “power down mode”
- High speed design
  - Bandwidth of sum trigger exceeds 500 MHz
  - Bandwidth of each building block exceeds 700 MHz
- Based on a combination of open and closed loop design
  - Open loop differential with linearity compensation
  - Closed loop adder with 50 Ω line driver [3]
- Power consumption < 90 mW/ch
  - With all trigger modes set to active
    - QFN 56 package (8x8 mm):
      - < 1mm bond wires
    - Downbonds to package cavity
      - < 0.5 mm wires
    - Multiple ground and power supplies

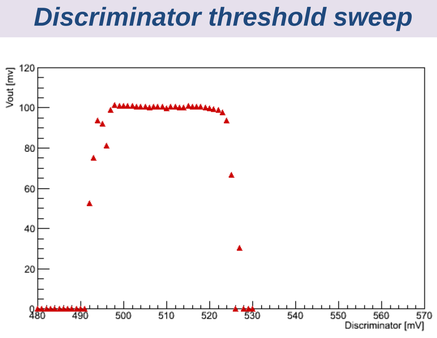


Test results

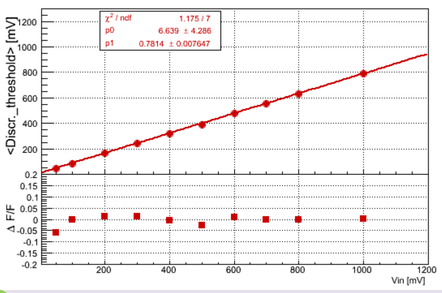
L0 mezzanine



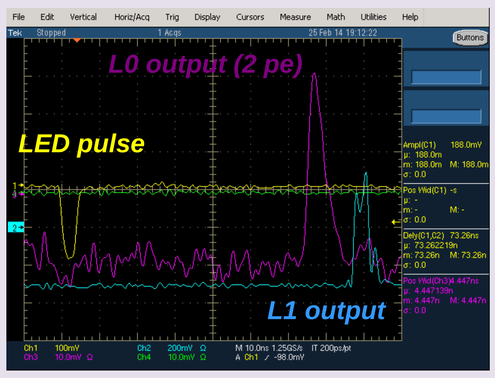
Discriminator threshold sweep



Discriminator linearity

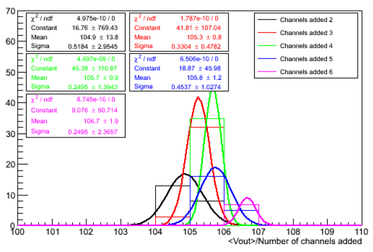


Dragon FE [5] with L0 & L1 ASICs

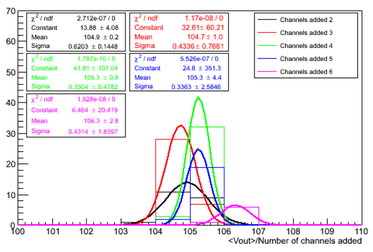


Majority trigger adder

Vin = 50 mV

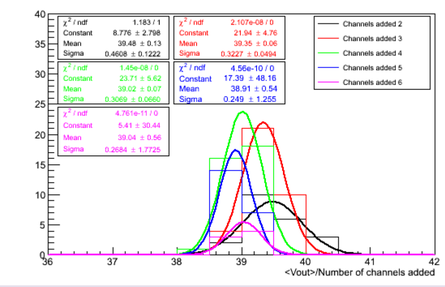


Vin = 500 mV

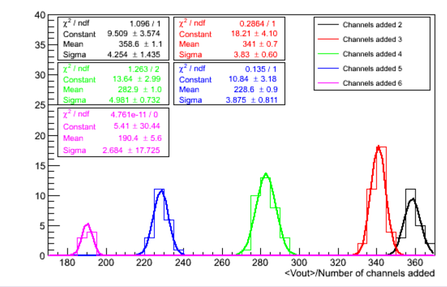


Adder

Vin = 50 mV

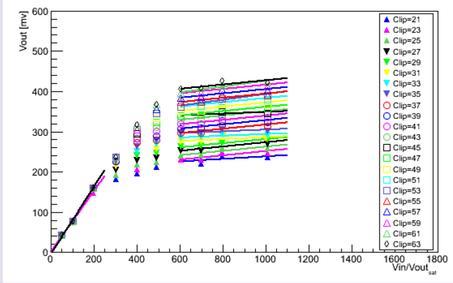


Vin = 500 mV

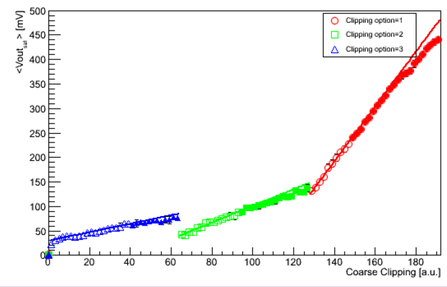


Sum trigger

Clipping transfer function



Clipping tuning range



References

[1] The CTA Consortium, “*Design Concepts for the Cherenkov Telescope Array*”, August 2010, http://arxiv.org/abs/1008.3703

[2] F. Guilloux, E. Delagnes “SCOTT: A time and amplitude digitizer ASIC for PMT signal processing”, NIM A, vol.725, 2013, Pages 175-178, http://dx.doi.org/10.1016/j.nima.2012.11.164.

[3] A. Sanuy, D. Gascón et al. "Wideband (500 MHz) 16 Bit Dynamic Range Current Mode Input Stage for Photodetector Readout", 2011 IEEE, NSS, Valencia, 2011

[4] L. Freixas et alt. “Analogue Sum ASIC for L1 Trigger Decision in Cherenkov Telescopes Cameras”, TWEPP 2014, Aix en Provence, 2014.

[5] H. Kubo et alt. “Development of the Photomultiplier-Tube Readout System for the CTA Large Size Telescope”, ICRC, Rio de Janeiro, 2013.

Acknowledgment

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