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# Versatile ASIC for L0 Triggering in Cherenkov Telescopes

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A versatile and reconfigurable ASIC implementing multiple concepts of low level trigger (L0) for Cherenkov telescopes is presented. Two different Level-0 approaches have been included in the L0 ASIC: the Majority trigger (sum of discriminated inputs) and the Sum trigger concept (analog clipped sum of inputs). Up to 7 input signals can be processed following one or both of the previous trigger concepts. Each differential pair output of the discriminator is also available as a LVDS output. Differential circuitry using local feedback allows high speed (500 MHz) to be achieved while maintaining good linearity in a 1 Vpp range.

## Summary

Arrays of Cherenkov telescopes typically employ multi-level trigger schemes to keep the rate of random triggers from the night sky background low. The trigger chain within a telescope may follow a digital, or analogue path. In H.E.S.S., Magic and VERITAS, analogue schemes are used, but for CTA several approaches for both options are under investigation.

The analog trigger concept is implemented in three stages. In the first one, the so-called Level 0 stage processes analog signals of individual pixels in a cluster. For this processing, two systems have been prototyped with COTS components in order to test either the Sum or Majority trigger concepts. In the former, the analog clipped sum of the signals of the pixels is raised to the second stage, the so-called Level 1, where the camera trigger decision is taken. In the latter, the signals are compared to a threshold value, so that it provides a fired pixel account to the Level 1 stage. At the Level 1, the analog combination of the Level 0 signals (both in the Majority and Sum modes) for all possible compact regions of a geometrical size given within the hardware limits is examined. This combination roughly consists of the analog addition of the Level 0 signals for different geometrical patterns. The Level 1 stage takes the decision to trigger the camera.

In this work we describe the ASIC implementation of the Level-0. The two different Level-0 approaches have been included in the L0 ASIC: the Majority trigger and the Sum trigger concept. All the approaches have been designed by using full differential circuits to minimize crosstalk and common mode noise. Each differential input goes through an attenuator circuit (programmable in the slow control interface) to the two level-0 trigger approaches in order to compensate photosensor non-uniformity. The Majority trigger concept compares the signal from each pixel to a voltage threshold (also programmable in the Slow Control (SC)) by using a discriminator circuit. Each differential pair output of the discriminator is available as a LVDS output. All the discriminator outputs are also internally added and are also available in an analog differential output. The Sum trigger concept clips the signals exceeding a given value (also programmable in the SC), in order to limit the influence of after pulses from the photo sensors. Then, adds the signal from all pixels in the cluster and sends the resulting signal to the Level-1 decision subsystem by an analog differential output.

All the analog L0 functionalities are implemented on a single ASIC. Different system and channels can be set in standby mode to minimize power consumption. Hence, it is a highly configurable and flexible system. Simulation and test results will be presented.Differential circuitry using local feedback allows high speed (500 MHz) to be achieved while maintaining good linearity in a 1 Vpp range. The ASIC is implemented in a 0.35 um SiGe BiCMOS technology.

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