PACIFIC: A 128 ch ASIC for Scintillating Fiber Tracking in LHCb Upgrade

H. Chanal, A. Comerma, J. Mauricio, D. Gascon*, X. Han, J. Mazorra, F. Yengui, N. Pillet, R. Vandaele

on behalf of the LHCb SciFi group

** SiUB & ICC. Universitat de Barcelona*

TWEPP – Aix en Provence – September 23th 2014

UNIVERSITAT DE BARCELONA

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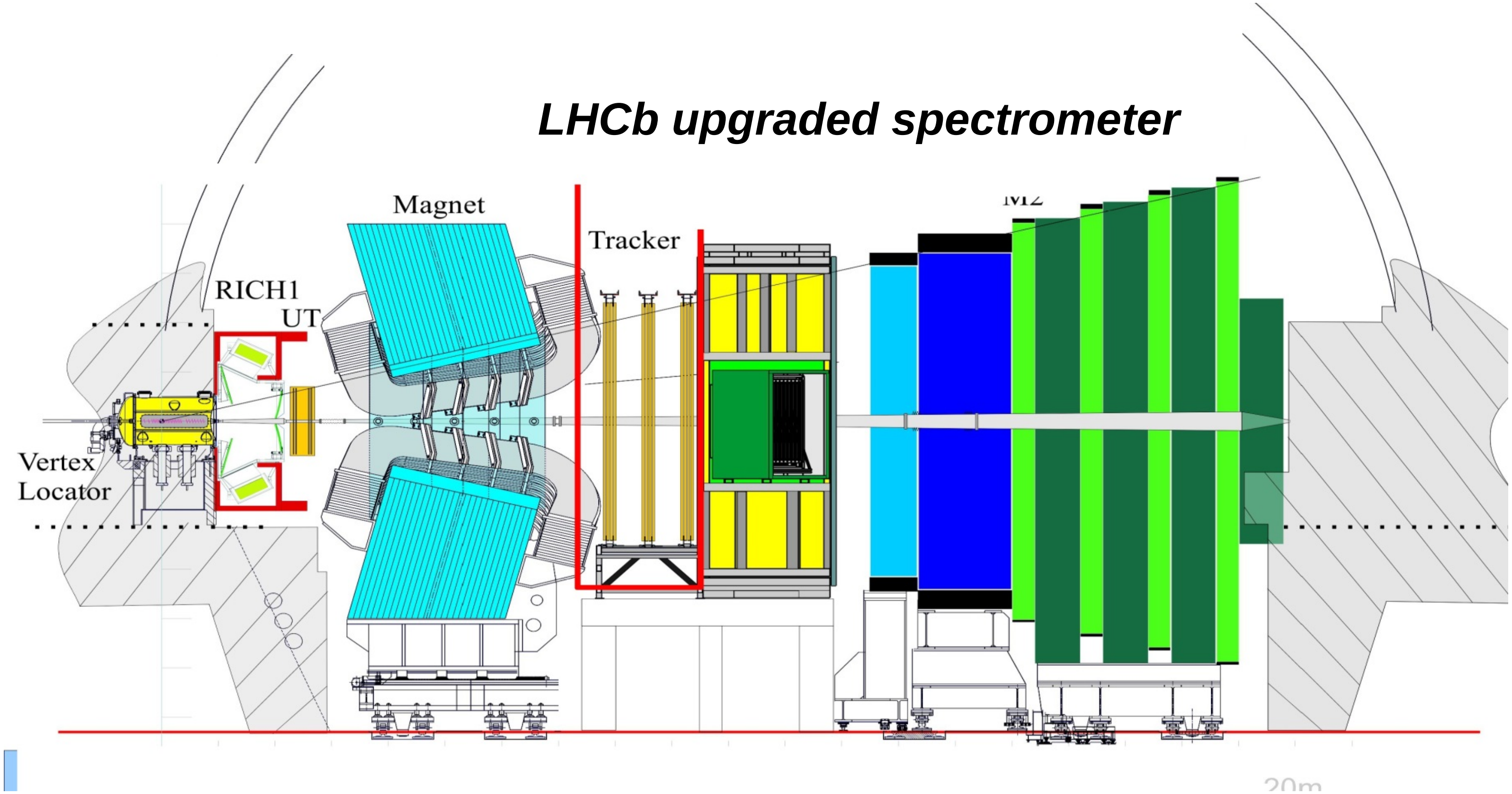
1. ***SciFi Detector***
2. SciFi Electronics
3. PACIFIC ASIC
4. Input stage
5. Shaping
6. Digitization
7. Test Results
8. Outlook

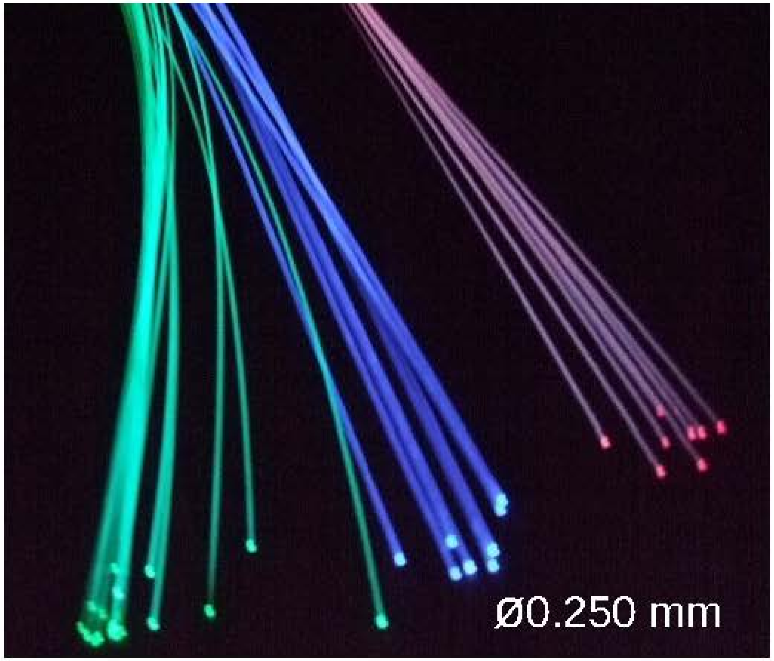
I. SciFi Detector: LHCb upgrade

- Almost every physics measurement in LHCb is limited by statistical uncertainties, not systematic: increase luminosity !
- Replace 1 MHz hardware trigger → 40MHz software trigger, all front- end electronics to 40 MHz
- 10 times smaller uncertainties after 10 years



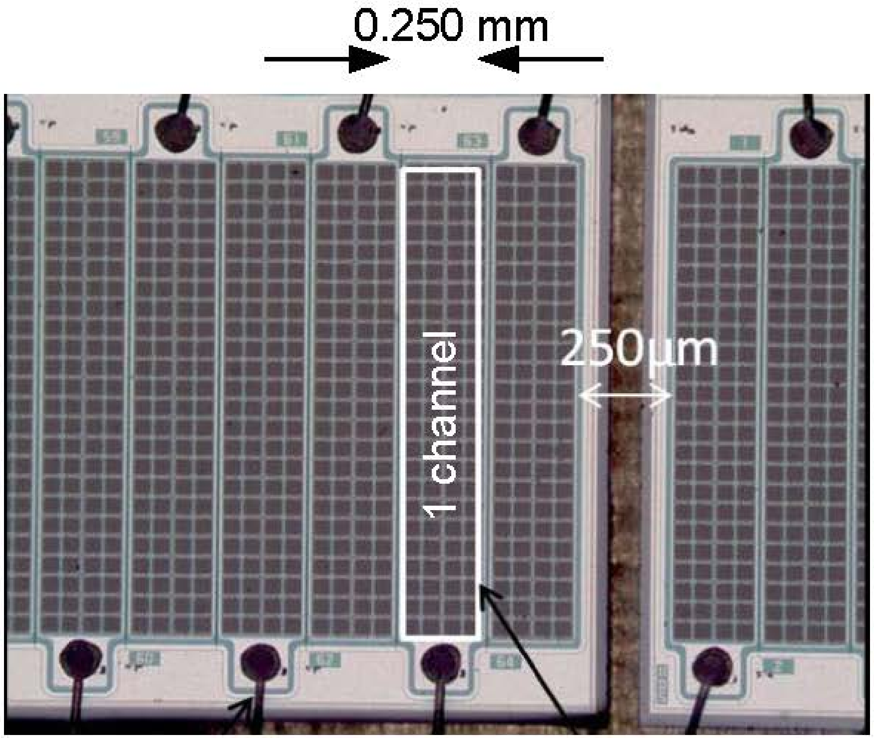
I. SciFi Detector

The SciFi tracker



Scintillating fibres

-fast decay time (2.8ns)
-good light yield and attenuation length



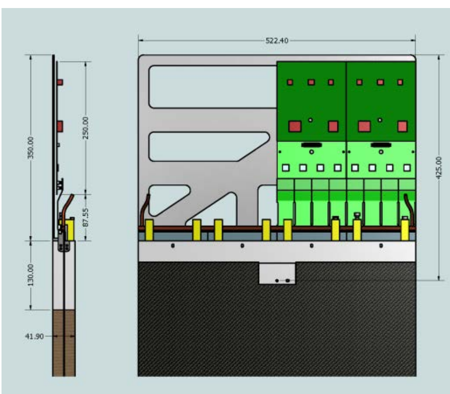
An array of pixelated silicon photomultipliers

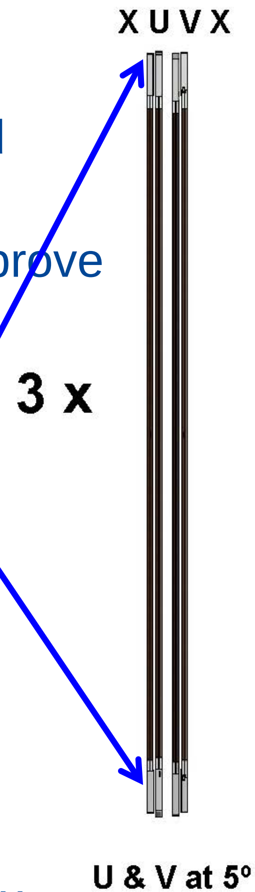
-fast signals
-high photon detection efficiency (40+%)
-compact channel size

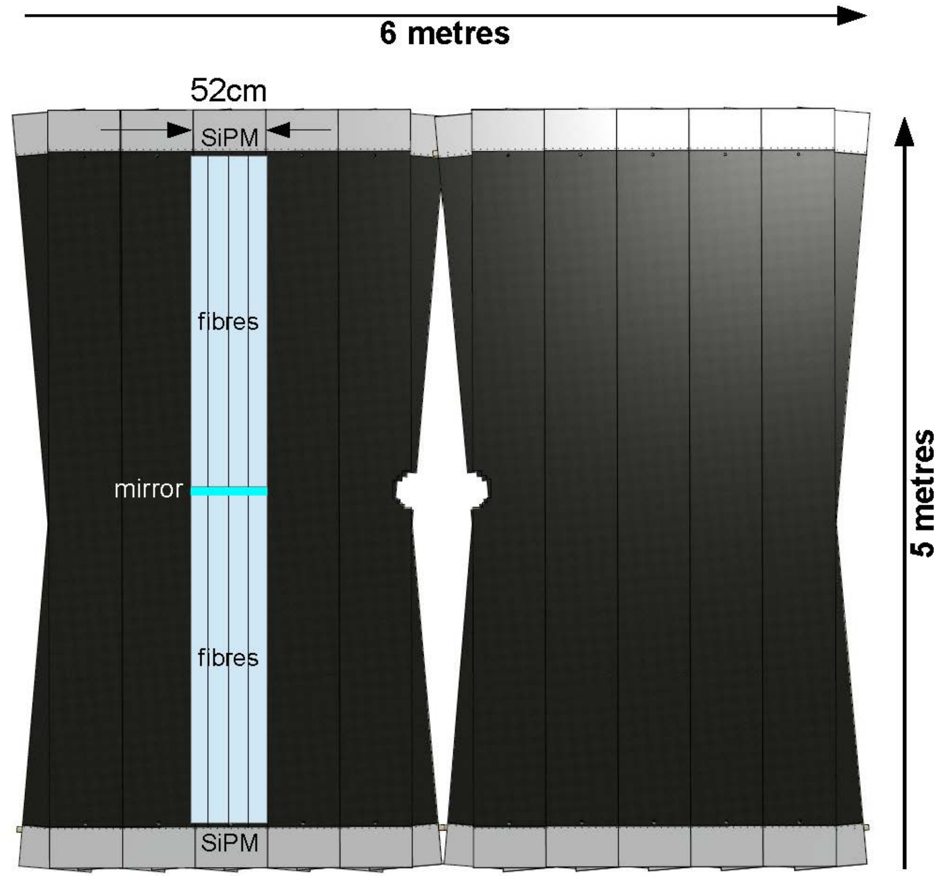
I. SciFi Detector

The SciFi tracker

- 3 stations x 4 detector planes
- 12 modules per plane
- 16 SiPMs per module
- Fibers read out at top and bottom
- Mirror in the middle to improve light yield (radiation)







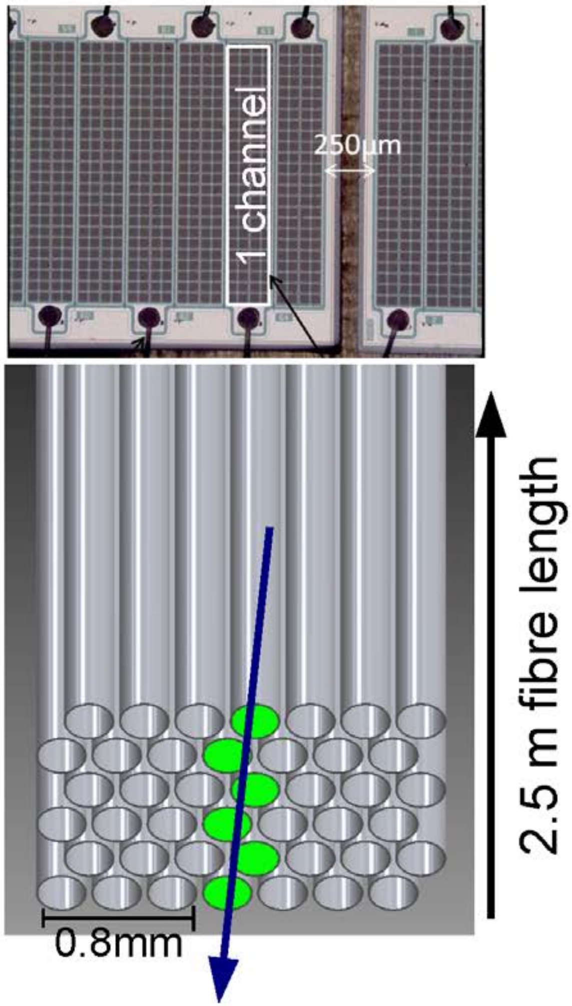
- SiPM, FE electronics and services in a ReadOut Box
- 560k channels
  - 4352 SiPM

I. SciFi Detector

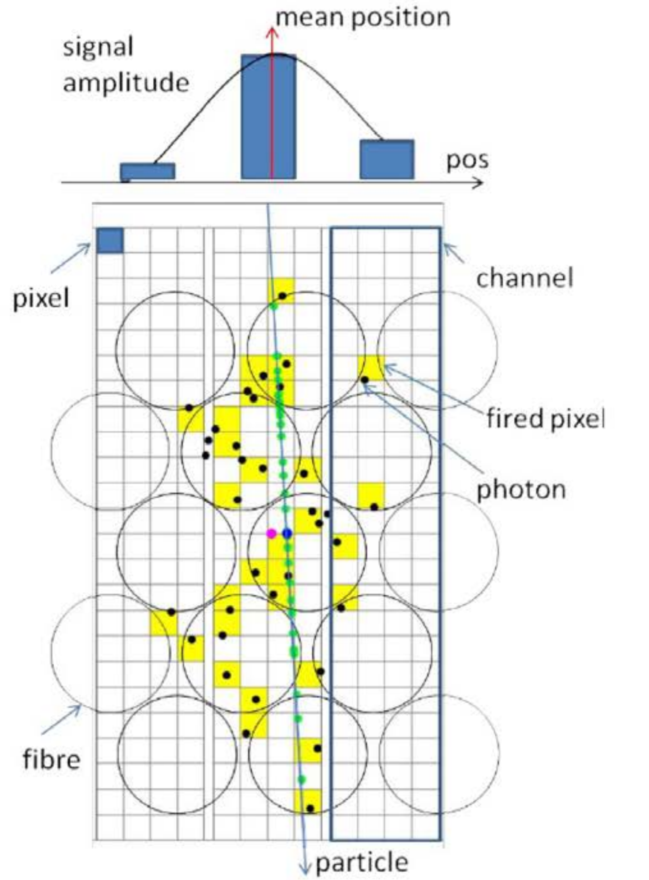
The SciFi tracker: basic principle

SiPM array

Scintillating Fibres (0.250mm diameter)



Signal cluster



Typically one observe 15-20 photoelectrons for 5 layers of fibre

I. SciFi Detector

II. SciFi Electronics

III. PACIFIC ASIC

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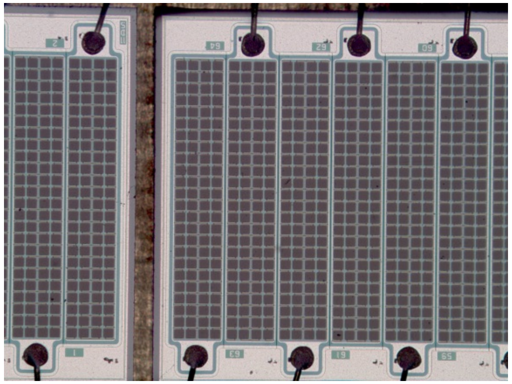
VII. Test Results

VIII. Outlook

II. SciFi Electronics: SiPMs

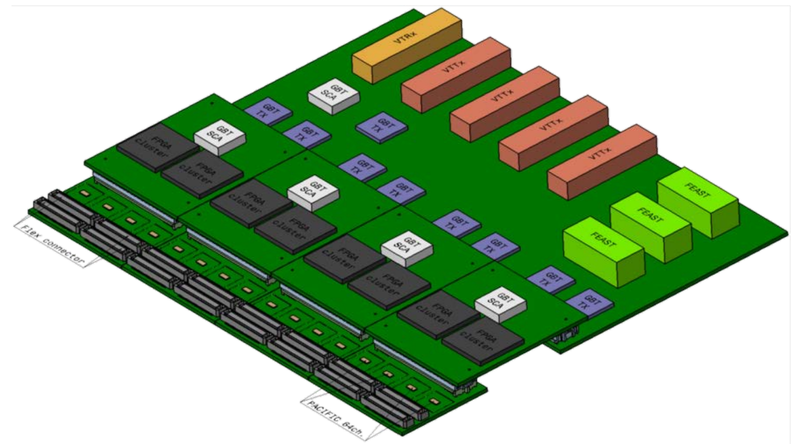
- Demanding SiPM requirements
- High PDE
- Low x-talk
- Support the radiation environment
- Small temperature dependence
- Small dead regions
- Thin entrance window!
- Right now only two producers can provide suitable SiPMs
  - Hamamatsu
  - Ketek
- Long capton interconnection
  - Transmission line model

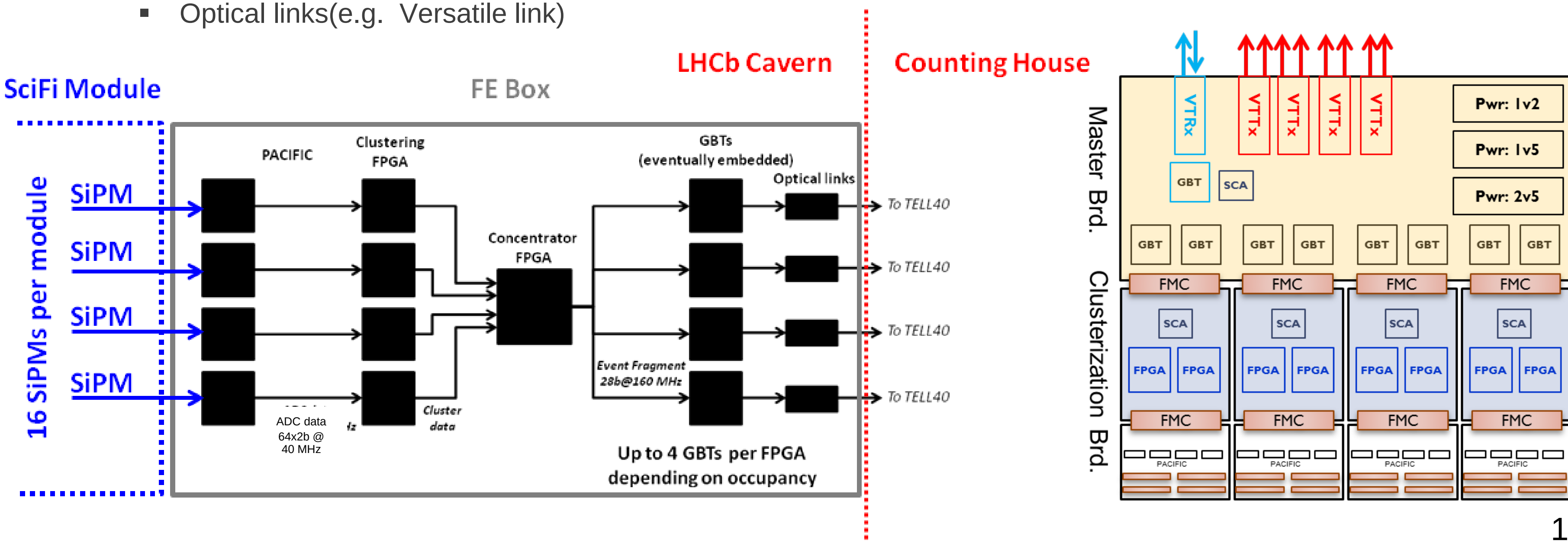


SiPM Flex Cable

II. SciFi Electronics: Read Out Box

- FE Box consists of 3 boards
  - Analog board
    - Pacific chip (one or two)
    - Connectors to SiPMs and FPGA
  - Clusterization board
    - Microsemi FPGA(s) and eventually GBT(s)
    - Connectors to PACIFIC and Master
  - Master board
    - Concentrator FPGA under discussion
    - Master GBT
    - SCA
    - Power
    - Optical links(e.g. Versatile link)

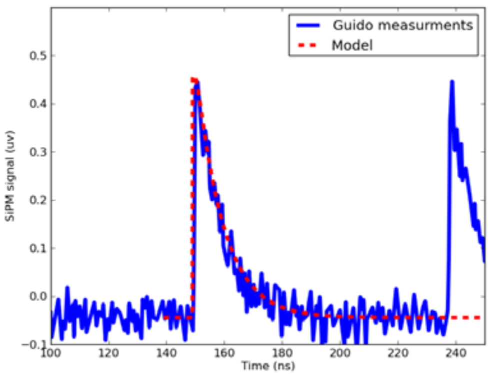


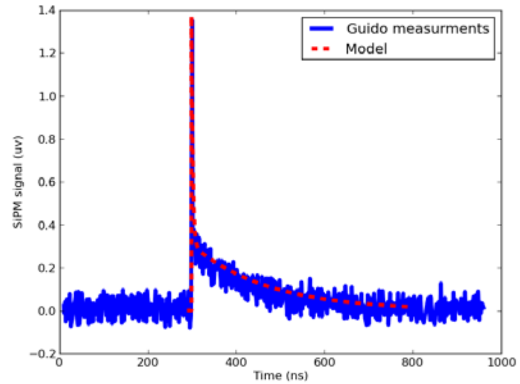


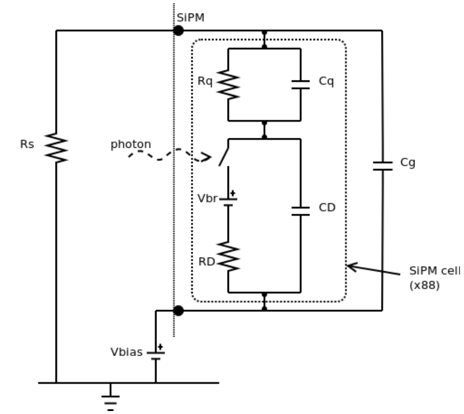
II. SciFi Electronics: the signal

- Two providers and different prototypes: ***signal shape not fully defined***

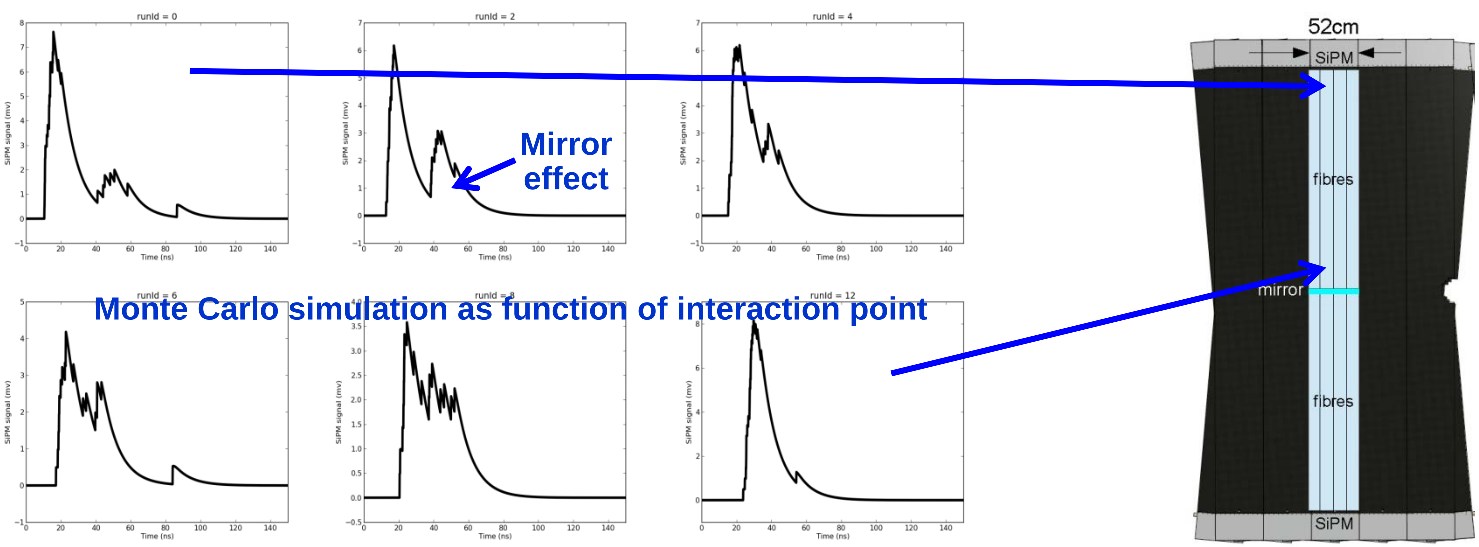
Single cell signal (measurement versus simulation)







- Low photo-statistics: ***signal dominated by large statistical fluctuations***
  - Radiation damage will worsen the problem
- ***Signal shape depends on the interaction point***



I. SciFi Detector

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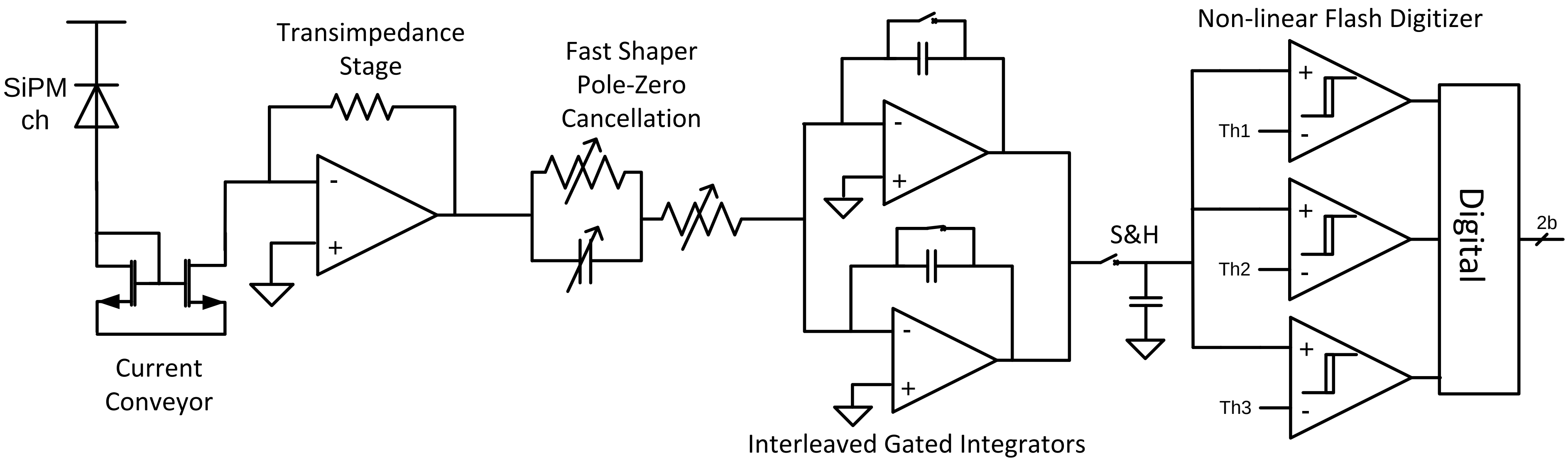
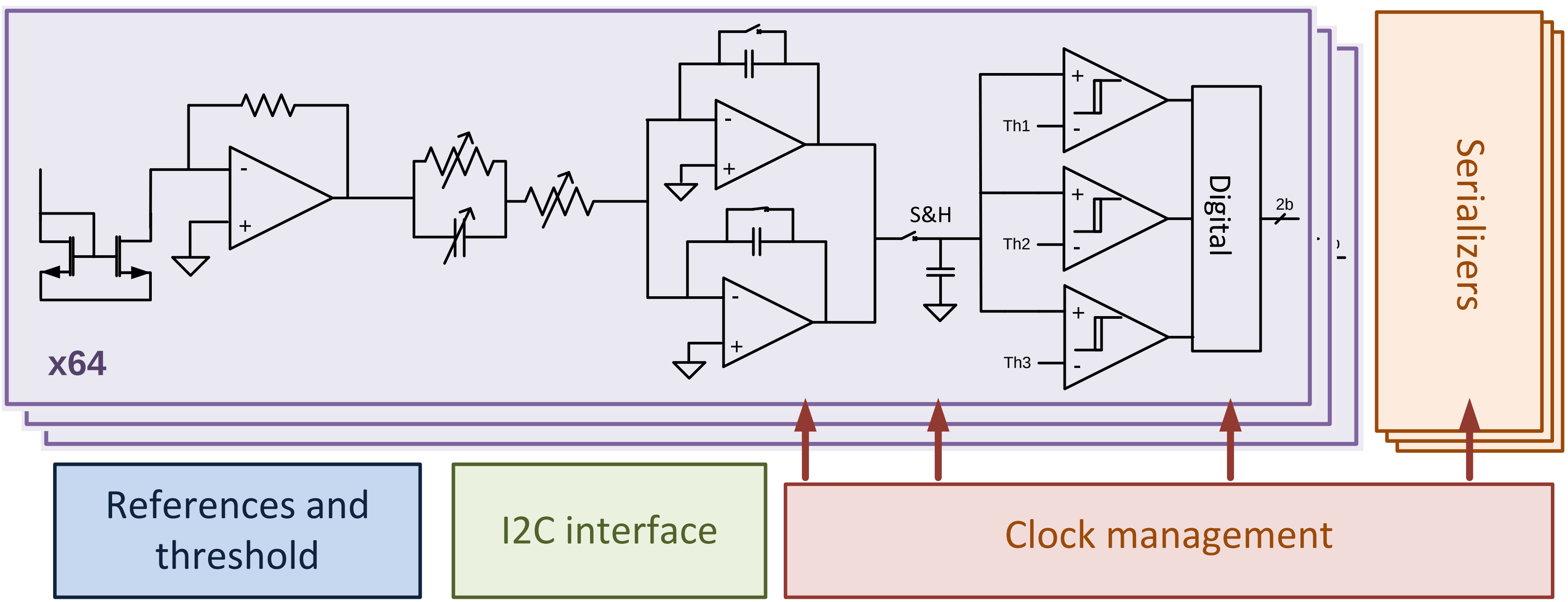
III. PACIFIC ASIC: ***Analog Signal Processing***



- Current conveyor with very low impedance input (≈ 30Ω)
  - Adjustable gain / dynamic range
  - Input voltage adjustment
- Fast tunable shaper
  - Pole-zero cancellation to cancel slow SIPM time constant
  - A FWHM of 5 ns is achieved for single-cell signal
- Dual interleaved 25ns gated integrator
  - Almost no dead time
  - Average photo-statistical fluctuations
  - Maximize charge collection (25 ns integration)
- 2 bits 40MS/s flash non-linear ADC
- Power consumption < 8mW/channel @ 1.2 V

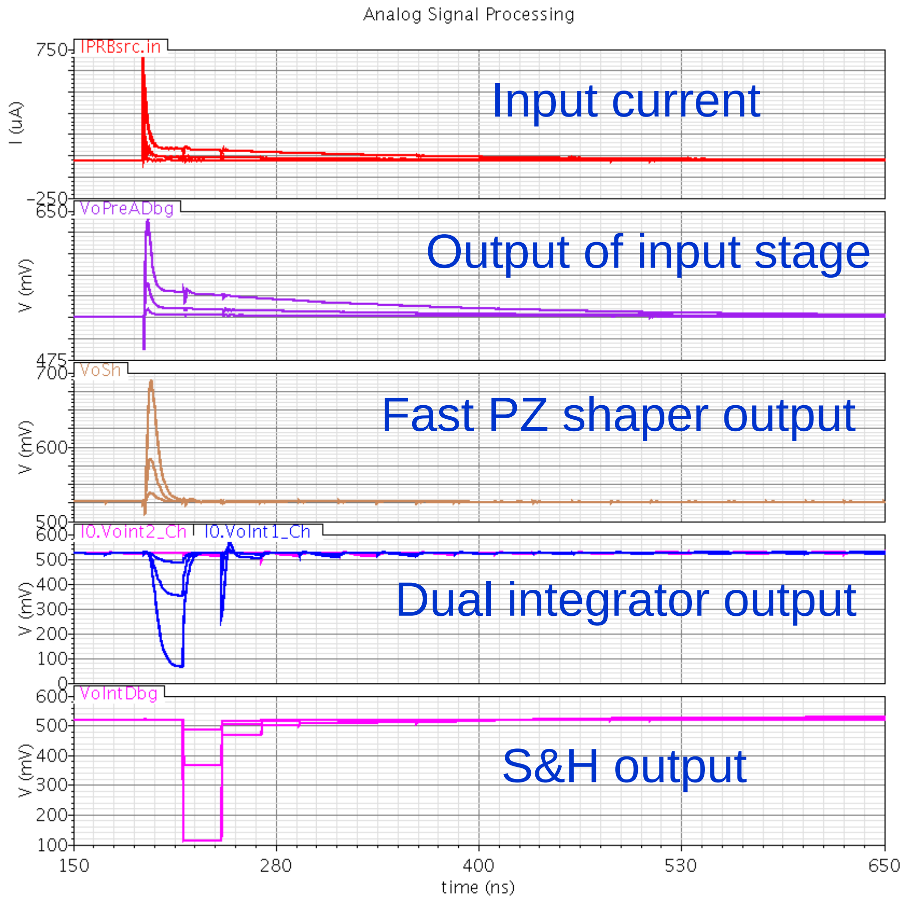
III. PACIFIC ASIC

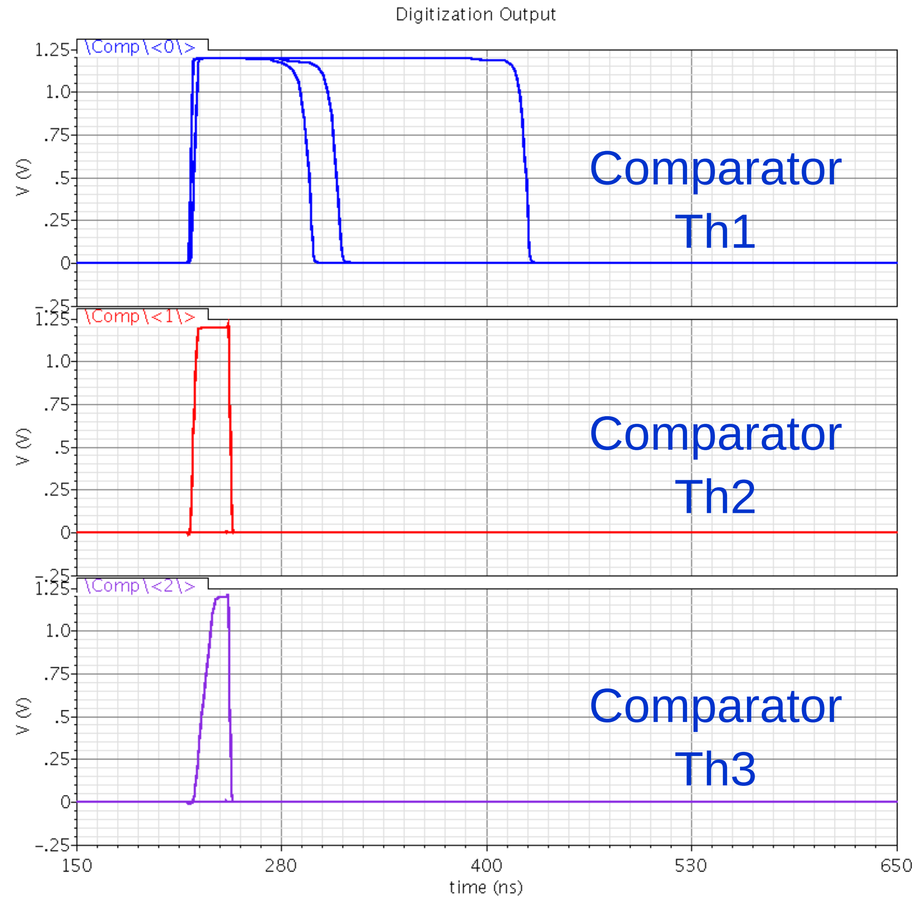


- 130 nm CMOS technology
  - PACIFIC1 (1 Ch) and PACIFIC2 (8 Ch) in IBM
  - PACIFIC3 will be in TSMC, with 64 Ch
- Serialization at 160 MHz
  - Single ended versus differential output to clustering FPGAs
- Bandgap references and I2C interface based on CERN design

III. PACIFIC ASIC

- Analog signal processing simulation
  - Signal: 1, 5 and 15 cells
  - Threshold 1 is set to detect single cell (higher value in data taking)





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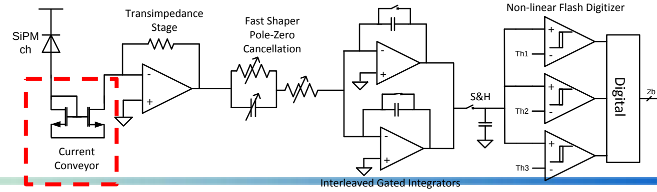
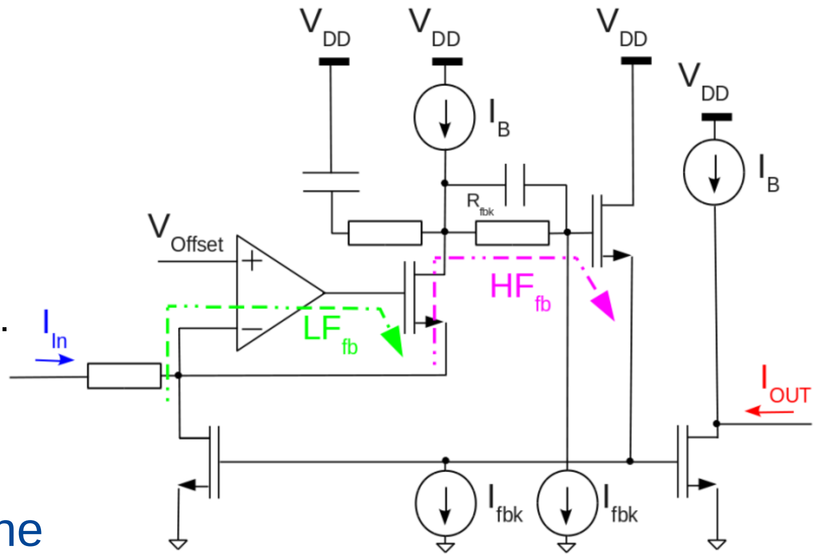
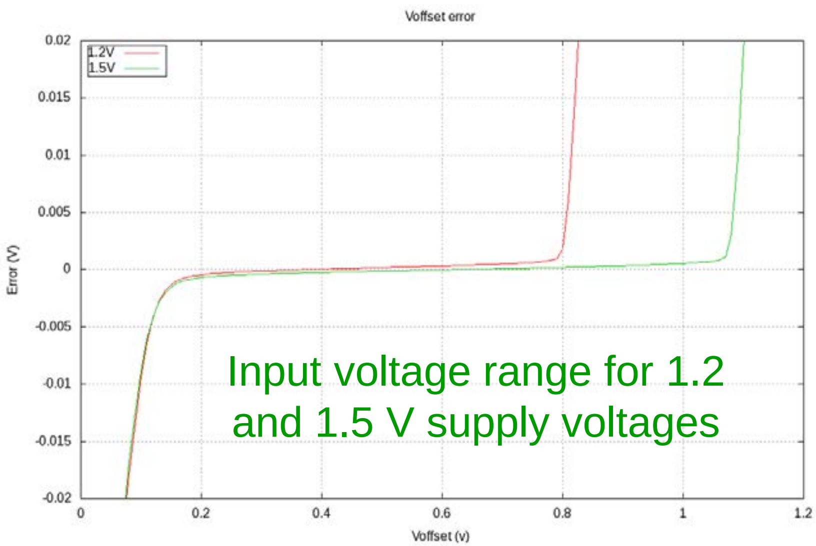
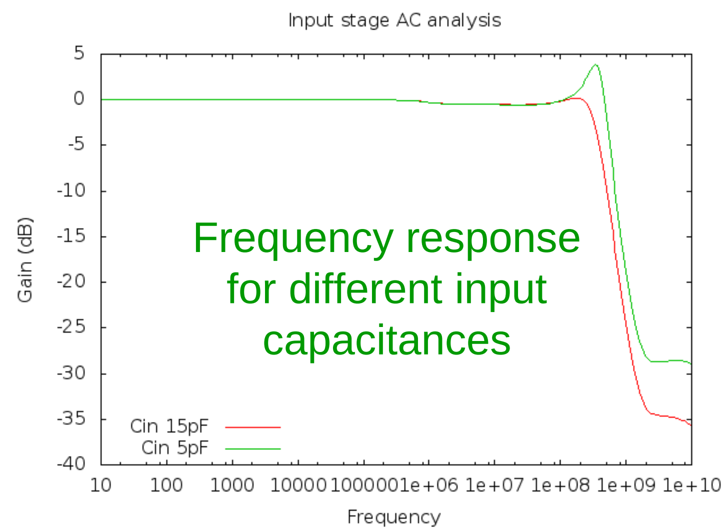
IV. Input stage



- Low voltage current mode preamplifier with the current flowing from the SiPM anode to the circuit:
  - High bandwidth (> 250MHz).
  - Low power (< 1mW, maximum of 8mW/channel including all ASIC).
  - Low input impedance (30Ω < Zin < 40Ω).
  - DC voltage controllable at input node (≈ 0.5V range).
  - Good single cell resolution for calibration.
- The HF feedback path that keeps this input impedance constant (@ signal BW).
- The LF feedback controls the dc voltage of the input node by virtual short circuit with LF OTA.







IV. Input stage

- The HF feedback path that keeps this input impedance constant (@ signal BW).
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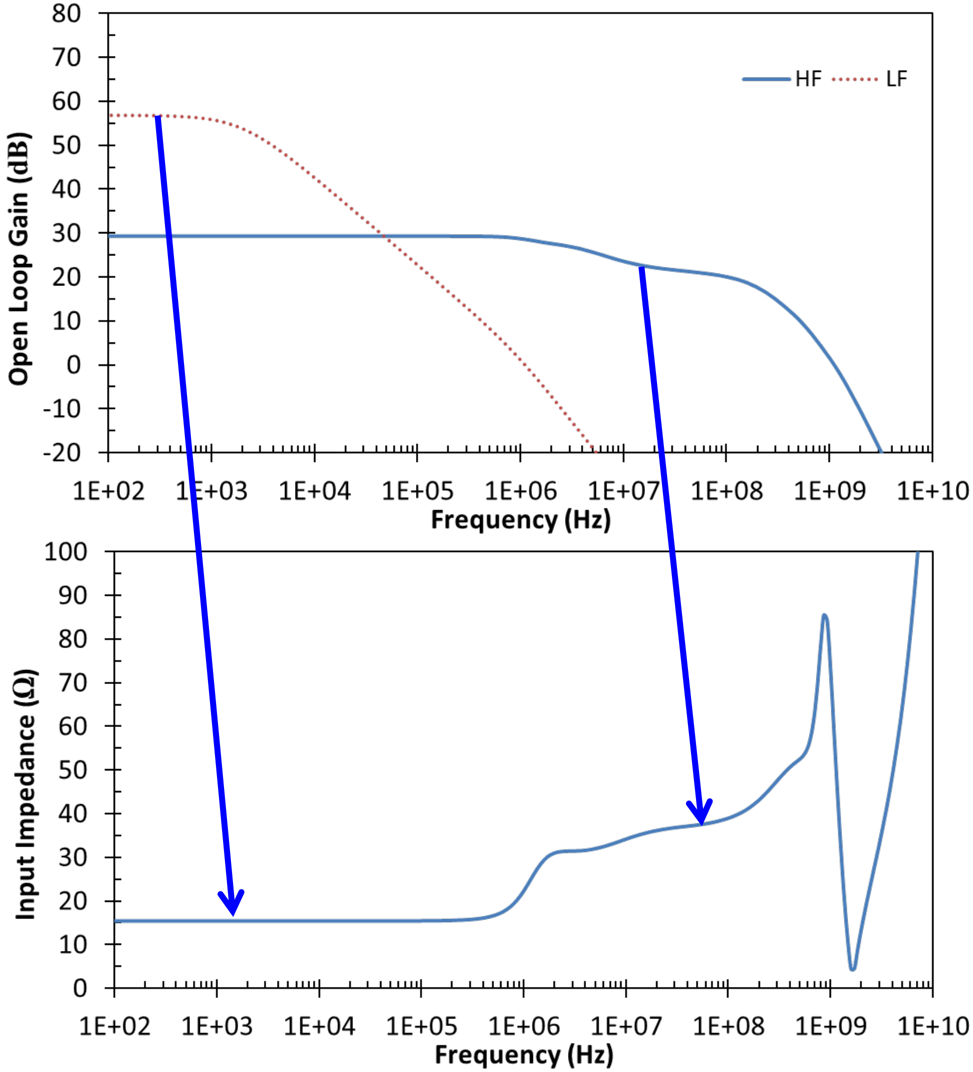
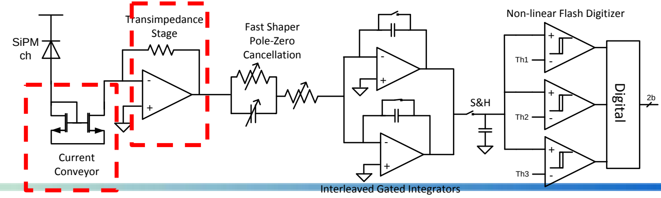


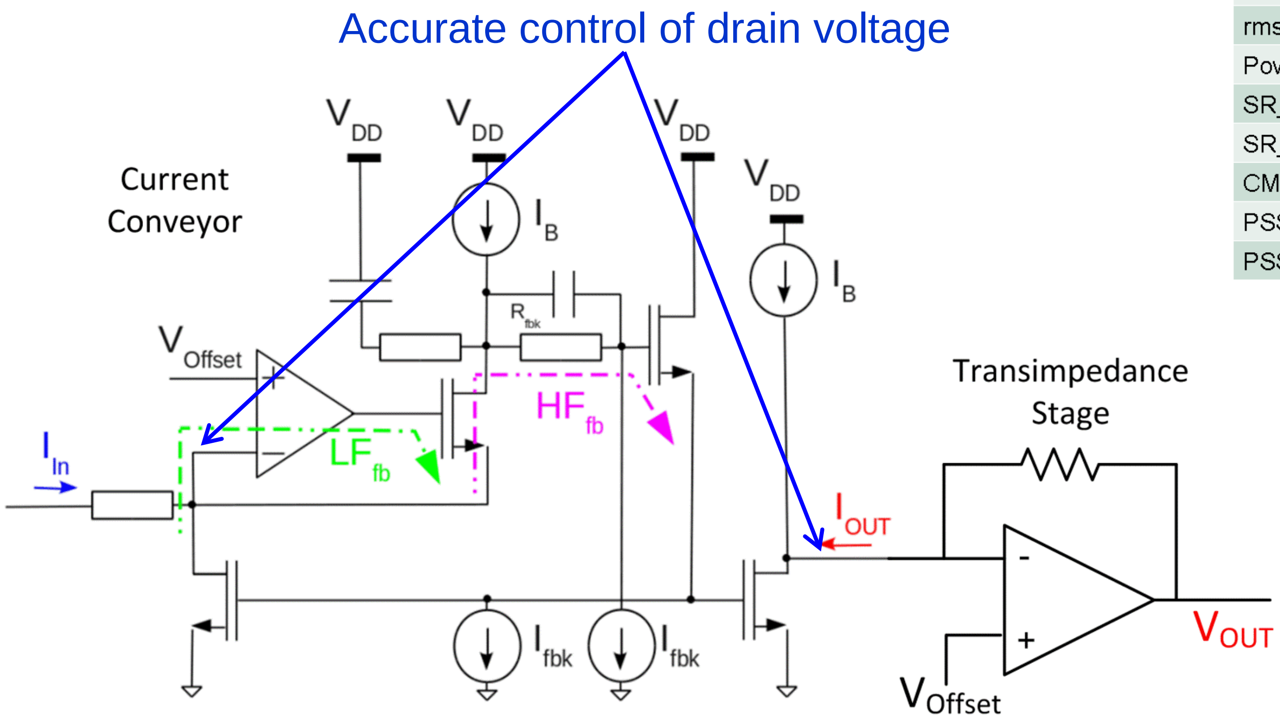
IV. Input stage



- SiPM current signal is converted to a voltage signal for further processing
- Closed loop transimpedance stage for:
  1. Current to voltage conversion
  2. Control of conveyor output voltage: linearity !
- A high speed OTA is required
  - GBW > 250 MHz with 80 º phase margin
  - Low power (700 uA, < 1 mW)
    - Class AB operation to cope with 5mA peak currents

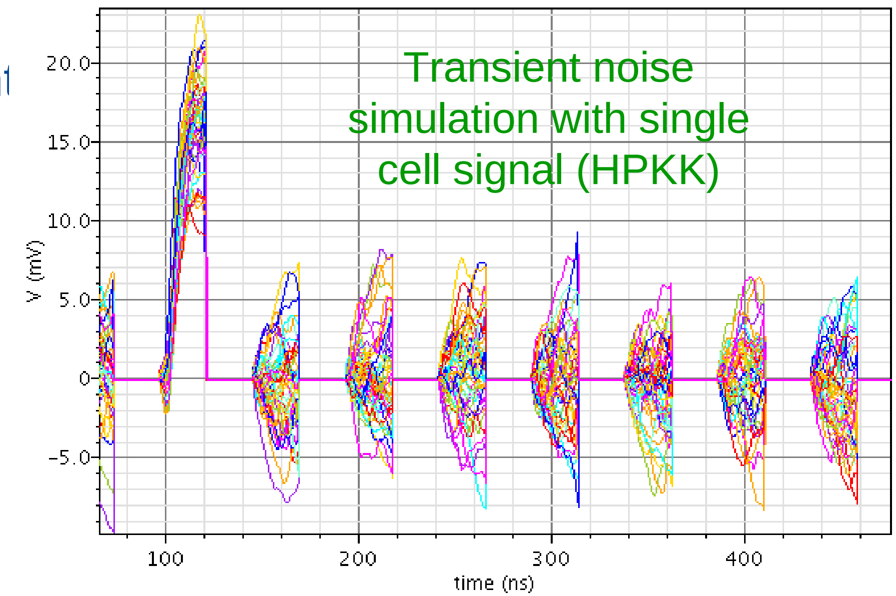
High speed OTA parameters

Parameter	Tech A	Tech B
Gain open Loop	54,38 dB	61,95 dB
Gain Margin > 9	8,67 dB	10,18 dB
Phase Margin > 65	86,78 deg	84,57 dB
Unity Gain Freq.	304,5 MHz	306,3 MHz
Bandwidth	463,7k	209,5k
GBW	243,5M	262,7MHz
rmsNoise	184,7u	146,6u
Power DC (Vin=0.5)	771,2u	750,3u
SR_rise	99,77k	99,89k
SR_fall	-99,82k	-99,94k
CMRR	75,37 dB	79,72 dB
PSSR_m	71,45 dB	85,87 dB
PSSR_p	33,29 dB	41,64 dB

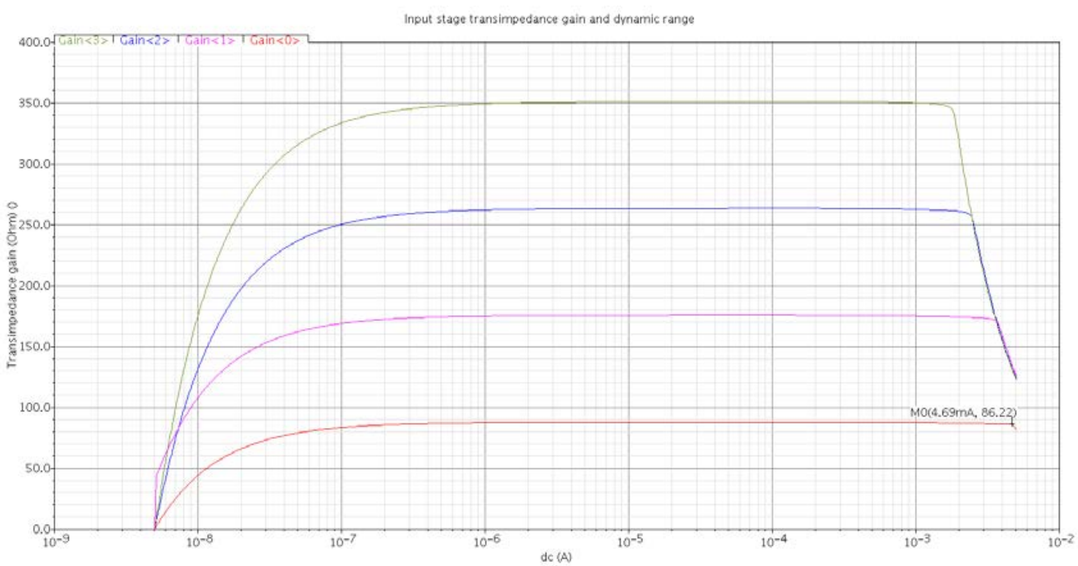


IV. Input stage

- To deal with different SiPM and different operating conditions the gain of the current conveyor is tunable by a factor 4
  - Gain of current mirror is changed
- Maximum range (about 5 mA) is achieved smallest gain
- Higher gain is intended for single cell calibration (“single photoelectron”)
  - Good resolution: SNR > 5 after gated integrator



Transient noise simulation with single cell signal (HPKK)



Linearity and dynamic range for different current mirror gains

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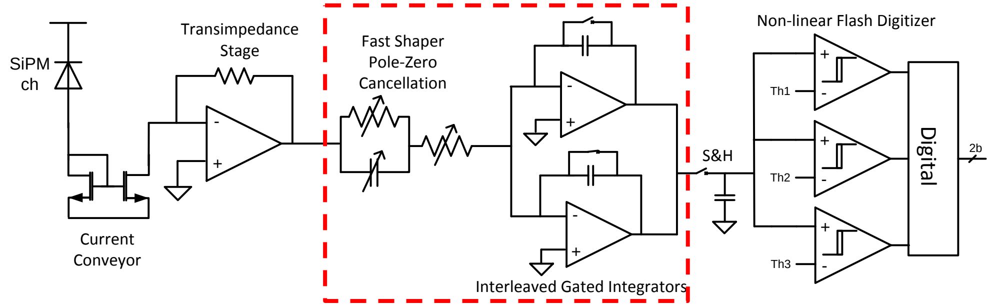
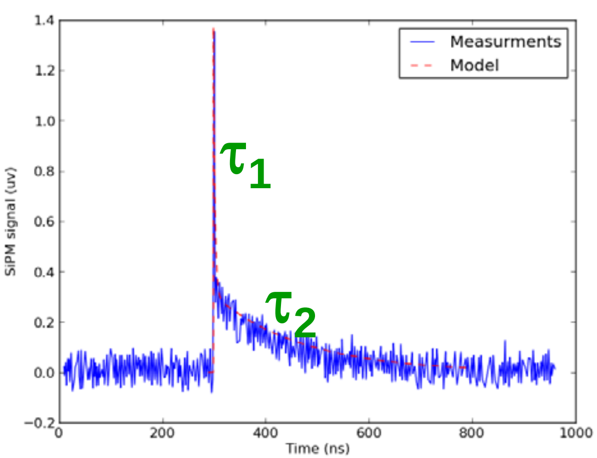
V. Shaping

- Two steps:
  - Pole zero cancellation for slow SiPM time constant supression
  - Gated integration for optimal light collection and average statistical fluctuations



- Pole-zero cancellation is a well known technique
  - For instance ion-tail cancellation in gaseous detectors
  - Main goal is to cancel slower SiPM time constant (τ_2)

Ketek



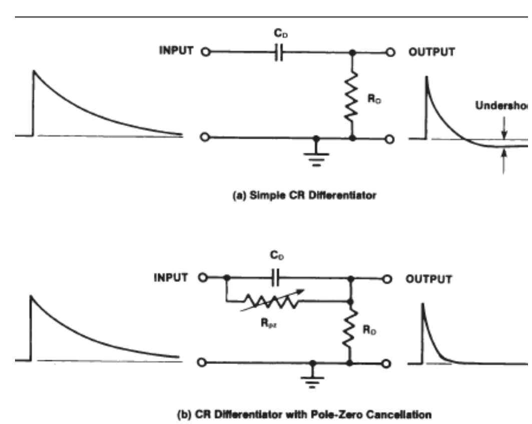
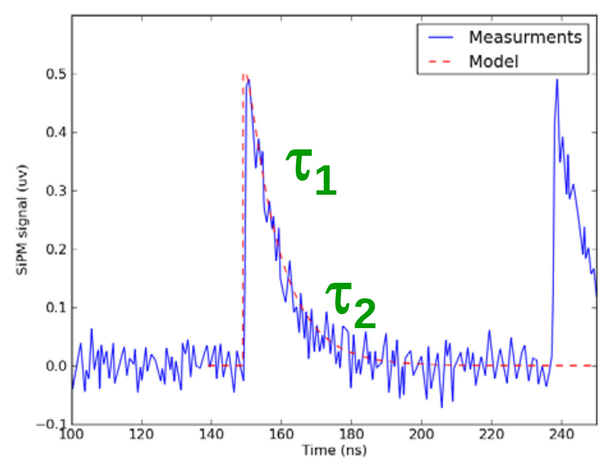


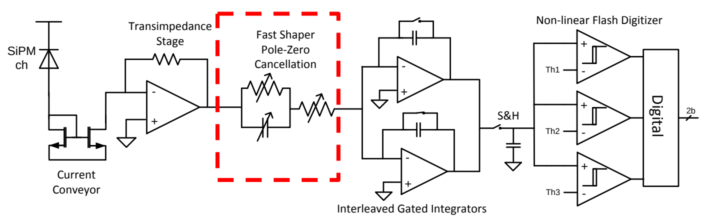
Fig. 12. The Benefit of Pole-Zero Cancellation.

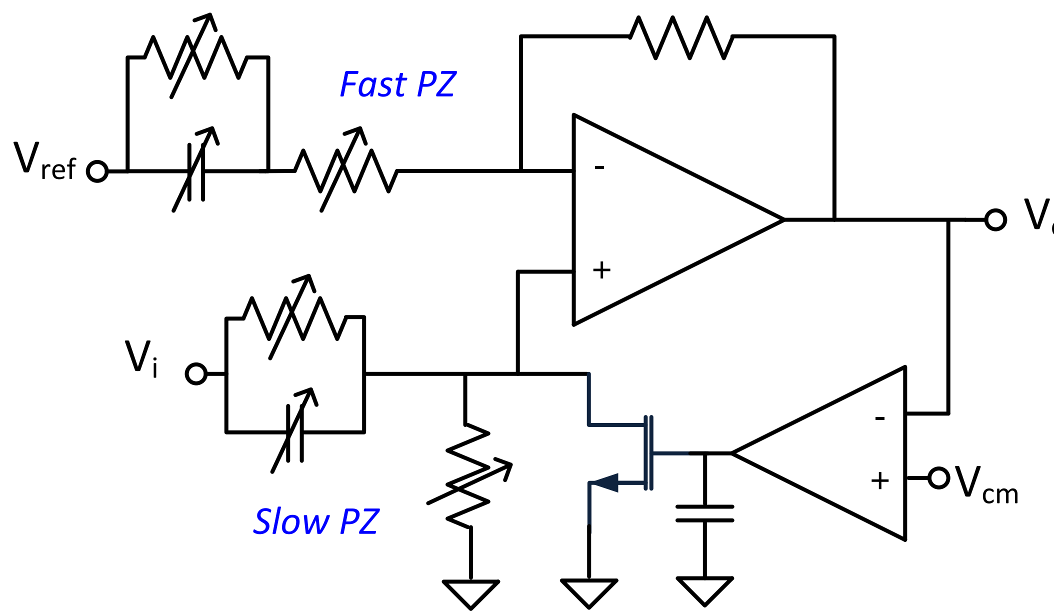
Hamamatsu



V. Shaping

- Double pole-zero cancellation.
  - First time constant cancels the slowest time constant of SiPM response, the one associated to internal SiPM capacitances and quenching resistor.
  - The second one cancels the fastest one, related to parasitic interconnect capacitance and input impedance of the preamplifier.
- Closed loop shaper based on the same OTA used for the transimpedance amplifier of the input stage.
- The poles and zeroes are tunable, and they have been calculated to be able to operate with very different time constants of Ketek and Hamamatsu SiPMs
- A DC feedback loop is used to control the quiescent output voltage
  - Critical as next stage is a gated integrator



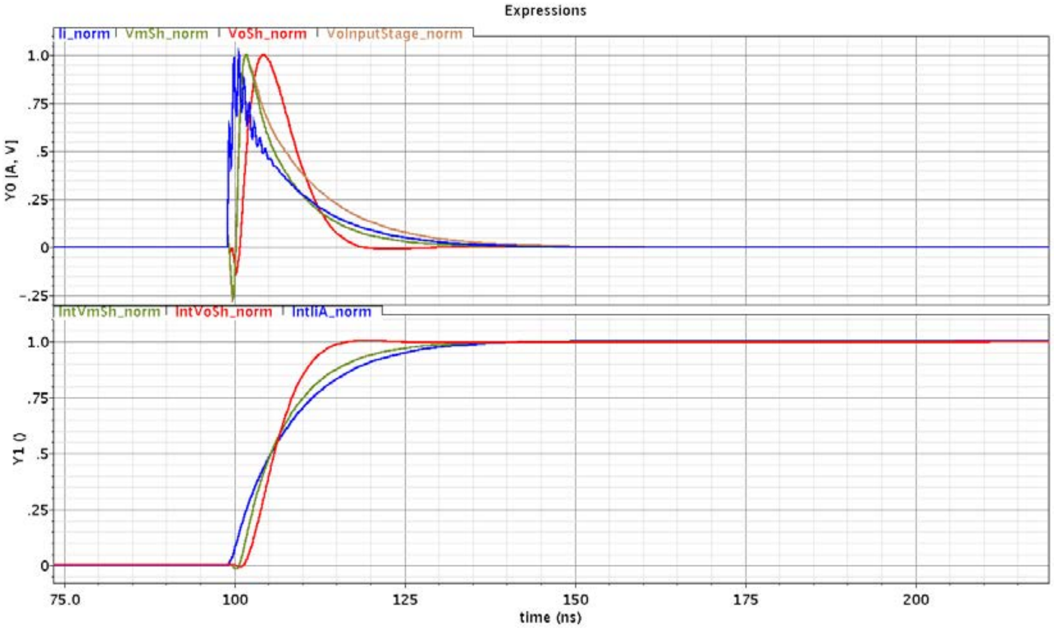


V. Shaping

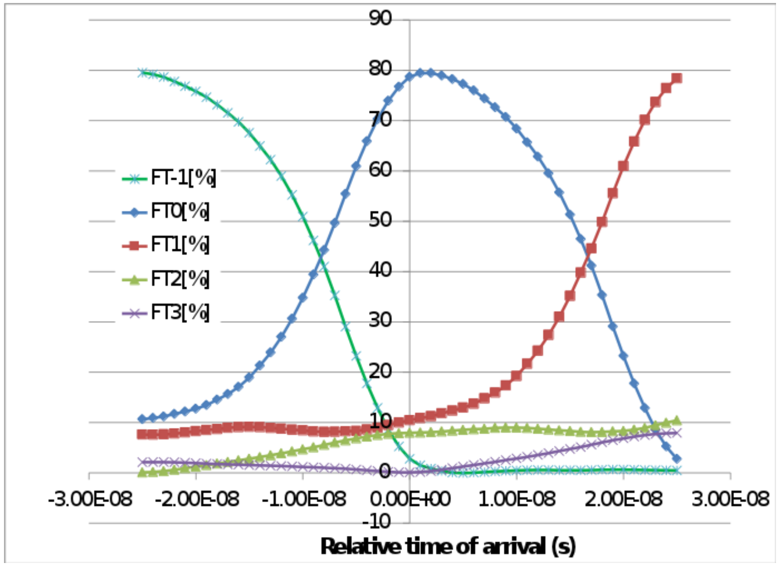
- Double pole-zero cancellation adapted for both SiPM pulse shapes
  - Normalized input current ("Ii_norm")
  - Input stage output ("VoInputStage_norm")
  - First pole zero cancellation output ("VmSh_norm")
  - Final shaper output ("VoSh_norm")
  - The integral of these signals is also shown.
- Final integral rise time is faster than 10 ns even if time constants are very different (particularly τ_2)

Hamamatsu

Transient simulation



Simulated output of gasted integrator (5 BX)



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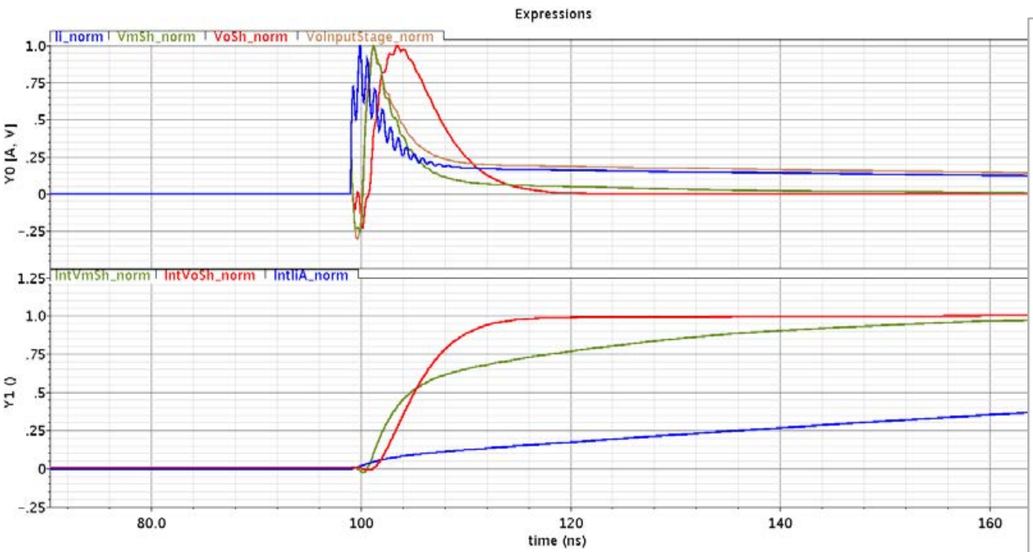

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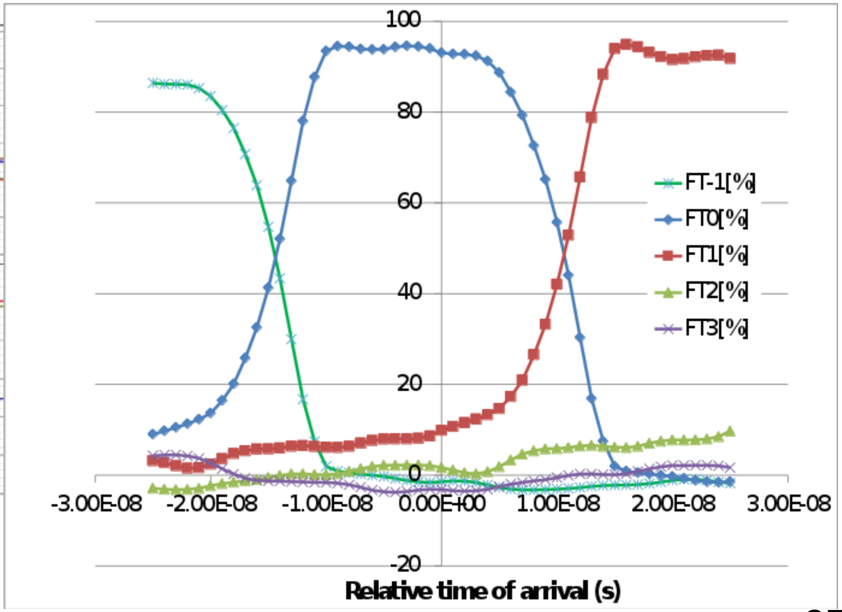
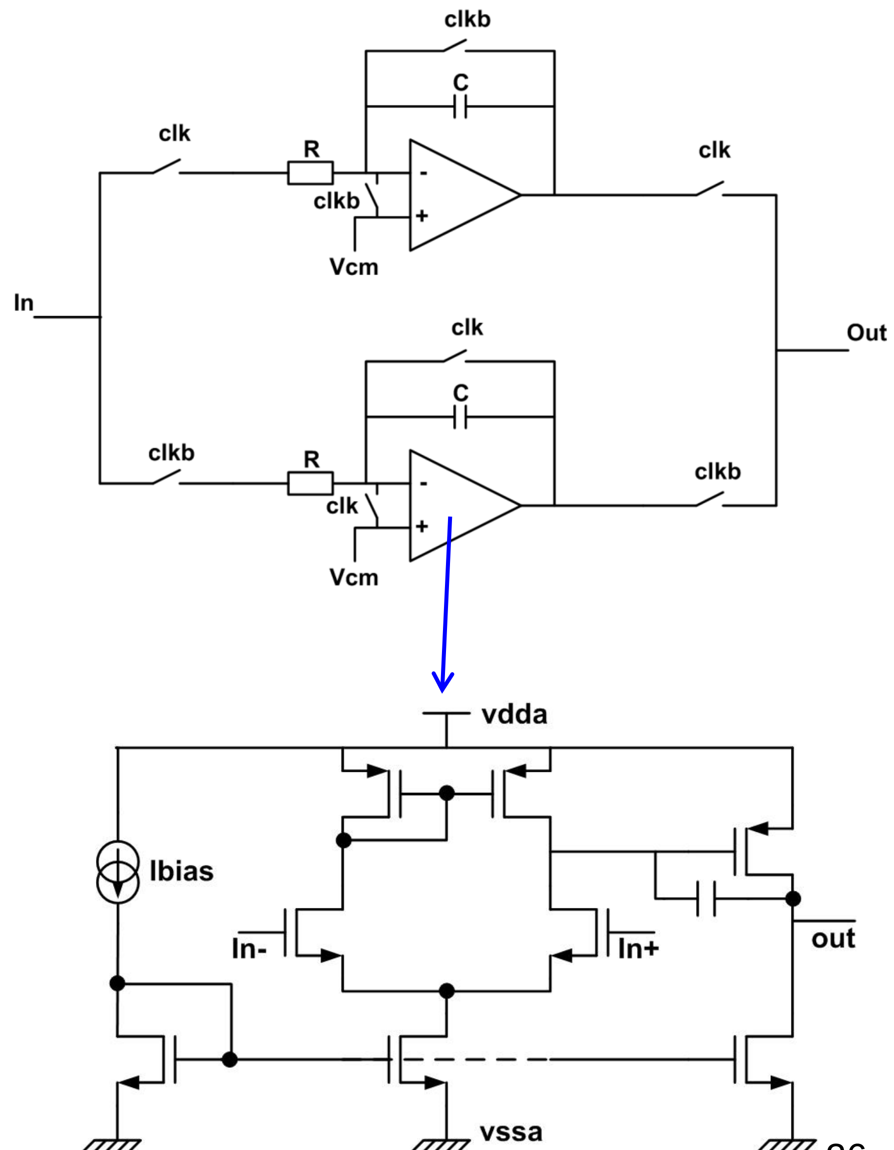
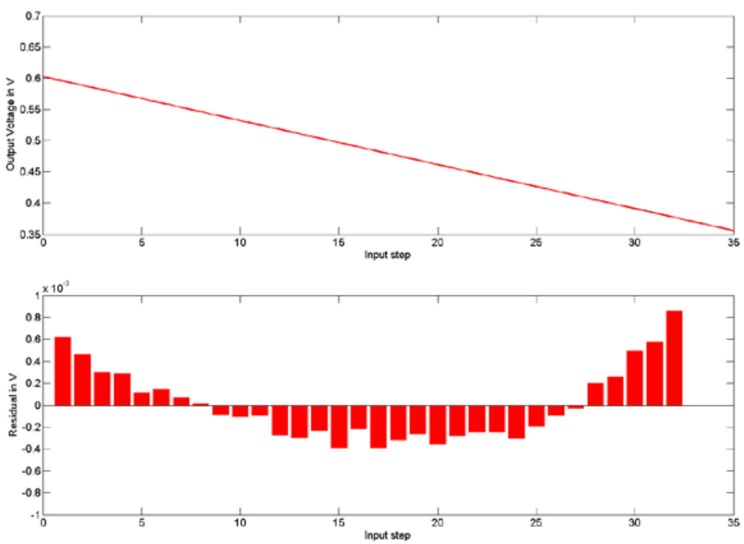


V. Shaping

- Classic integration architecture
- To avoid any dead time during the acquisition, it has been decided to interleave two gated integrator
- Digitization must be synchronized with gated integrator
- A classic Miller OTA is used for the integrator
  - 200 MHz GBW with 58º phase margin
  - 300 uA supply current



Integrator linearity



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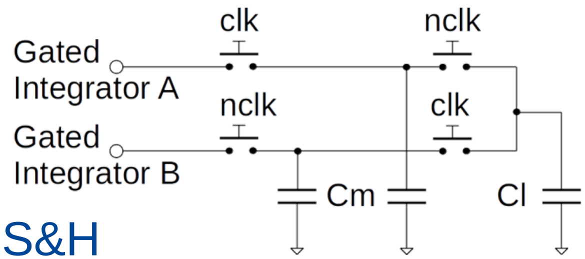
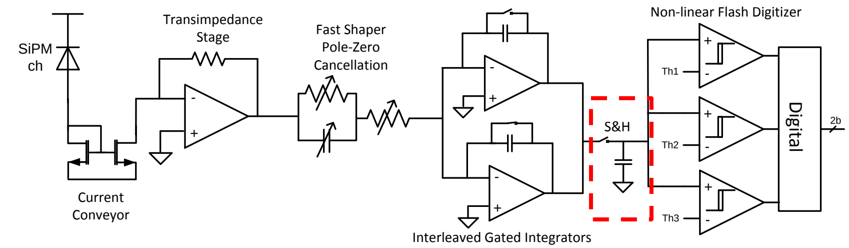
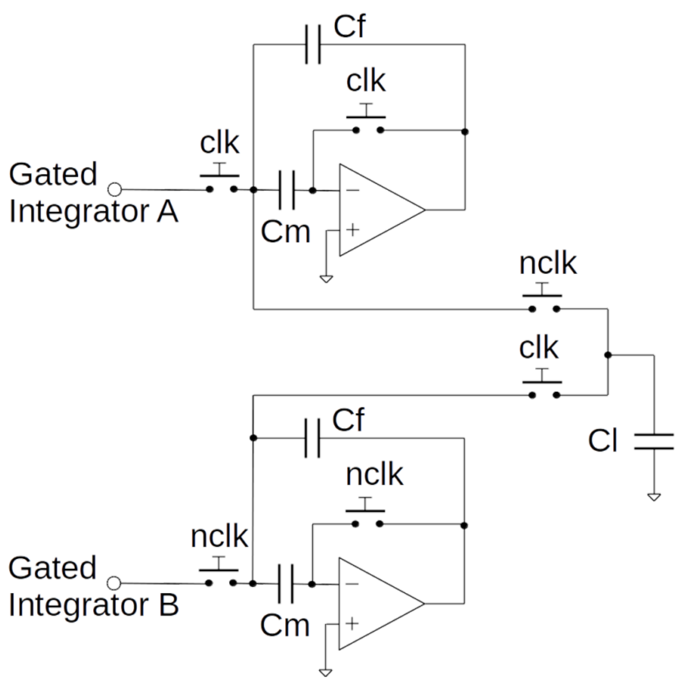
VI. Digitization

- A sample and hold circuit is required to store analog value at the end of integration period
- For first PACIFIC versions it was a simple capacitor & switch designs
  - Sampling errors
  - Charge sharing
  - Load depending



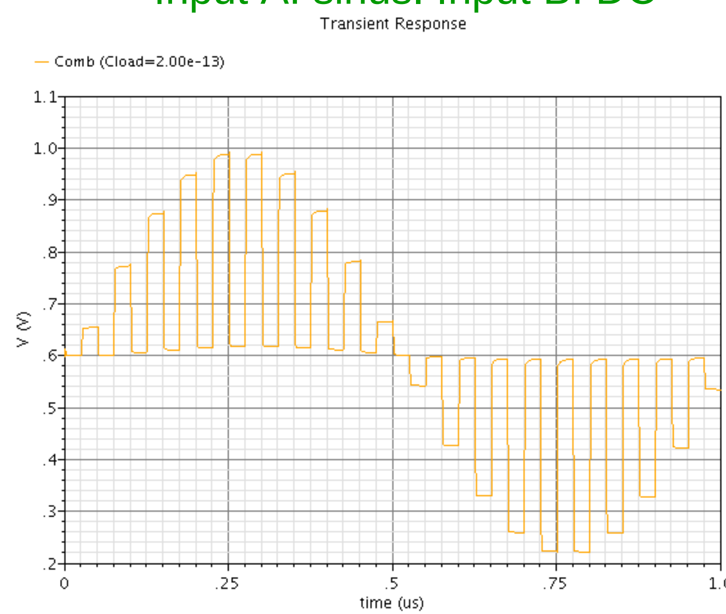


- Evolution to a Miller S&H

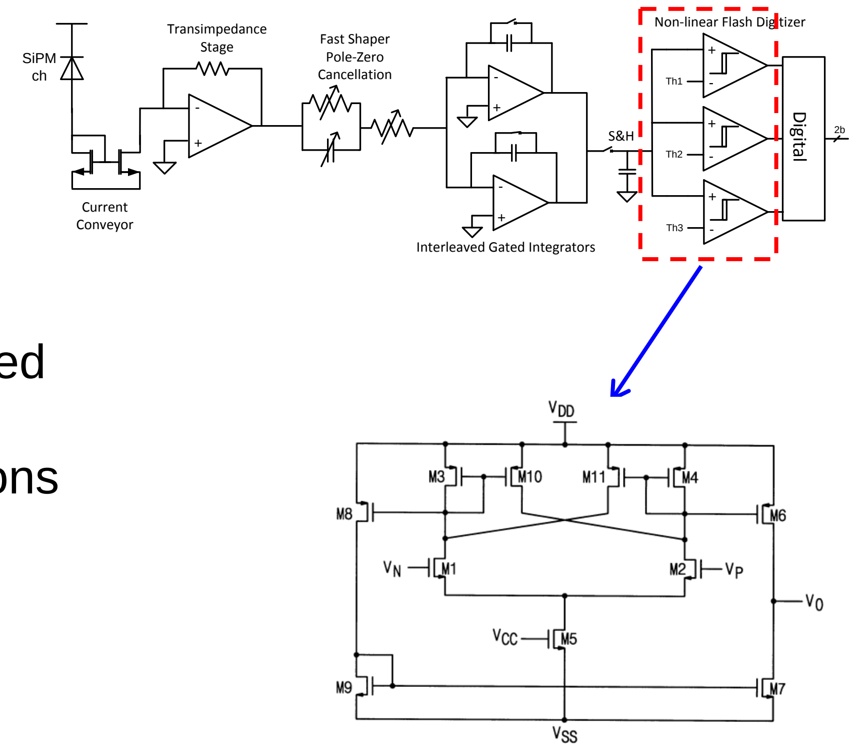


Miller S&H simulation

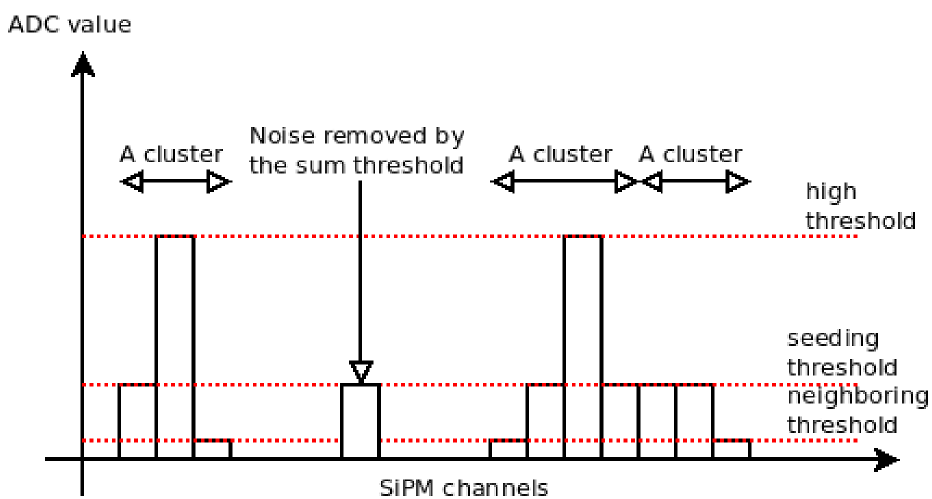
Input A: sinus. Input B: DC



VI. Digitization



- Simple barycenter computation with 3 thresholds:
  - Seed threshold: Candidate for a cluster
  - Neighbour threshold: With a seed, included in a Cluster
  - High threshold: Cluster, no others conditions
  - Cluster sum threshold: Confirm a cluster



- Comparator with hystheresis
  - About 10 mV
- 45 uW power consumption
  - 135 uW per channel
- Range: 20mV to 850mV

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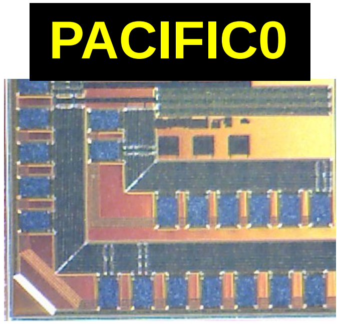
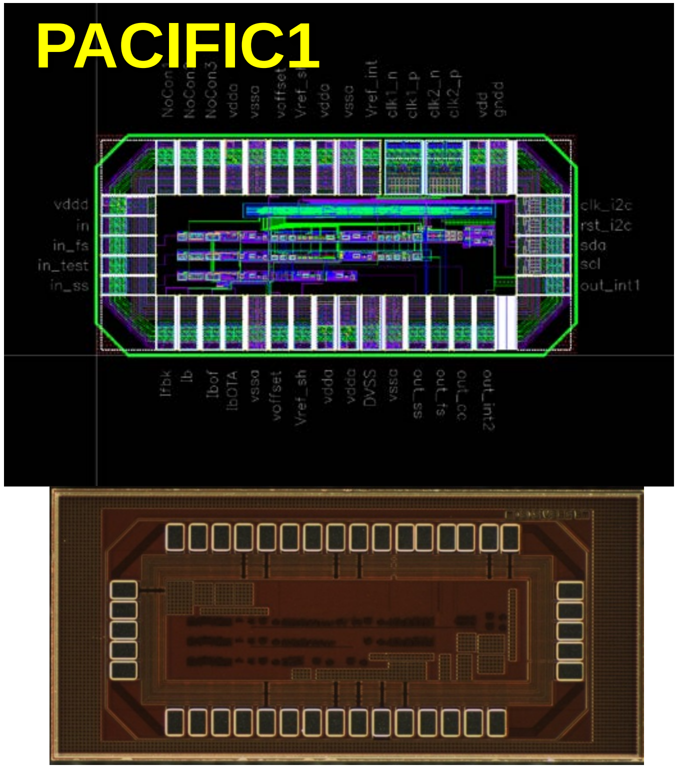
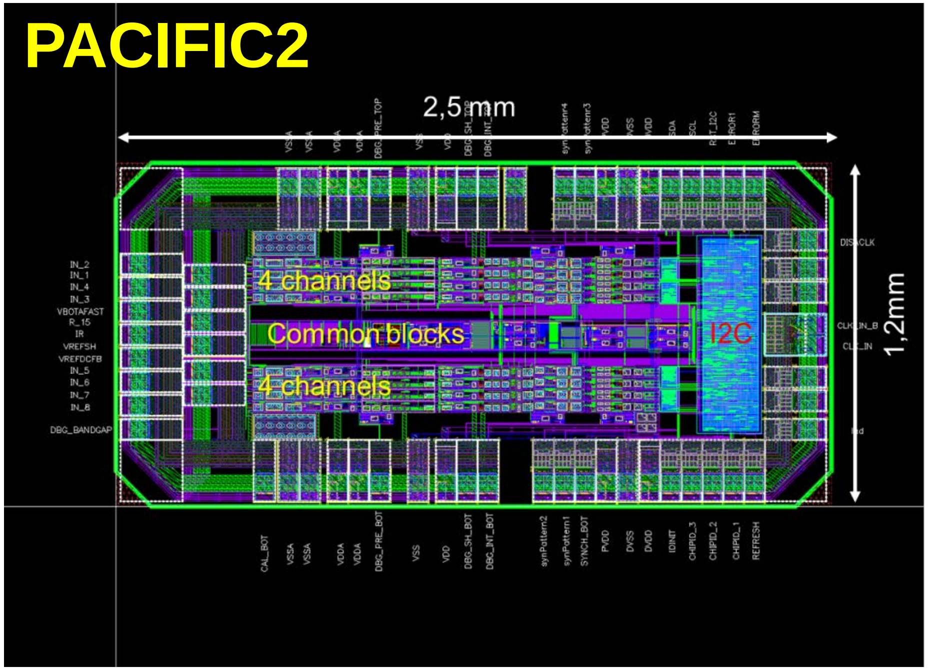
VII. Test results

- Several submissions using IBM technology:
  - PACIFIC0 (May 2013): Current conveyor
    - First version, fixed gain
  - PACIFIC1 (November 2013) : Full analog front end
  - PACIFIC2 (May 2014) 8 channels prototype with digitization.
    - PACIFIC2 has a design problem in the digital I/O ring
    - A second version has been submitted in August.
- Next prototype in TSMC (PACIFIC3):
  - 64 channels with digitization

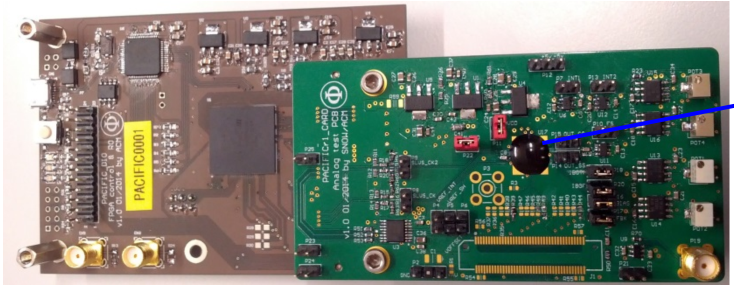


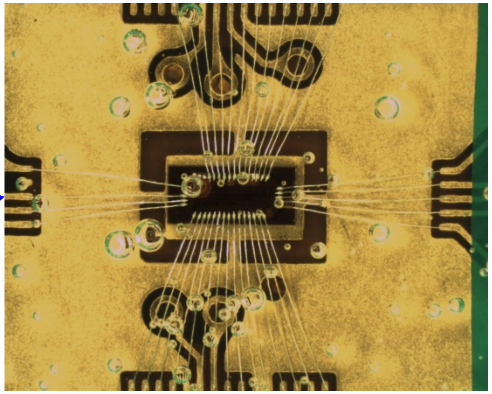




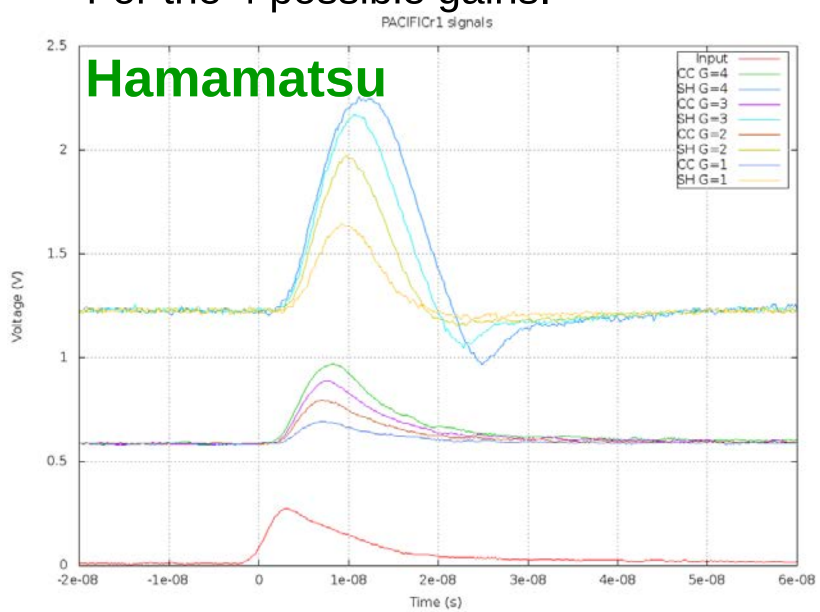
VII. Test results: PACIFIC1

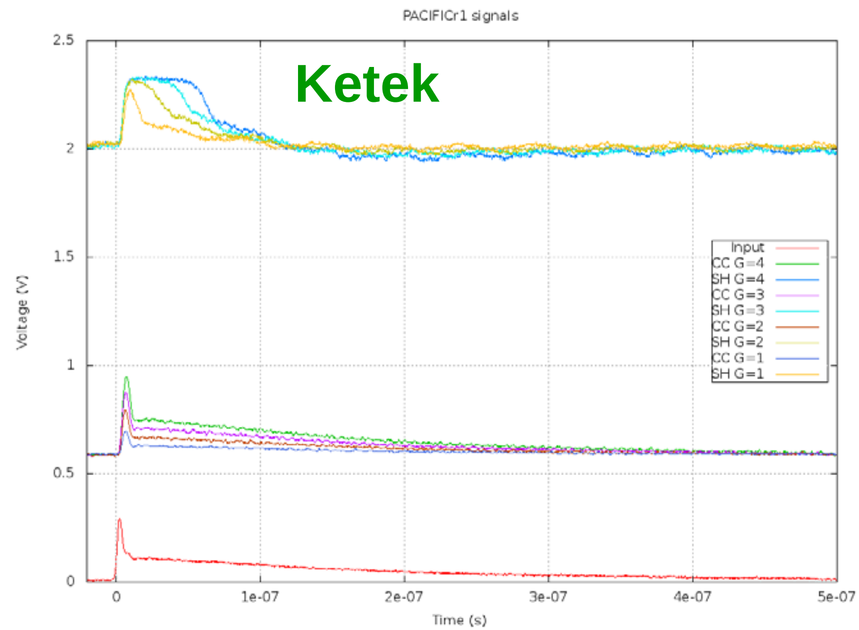
- Test set-up based on 2 PCBs
  - References, I2C, integrator clocks, etc





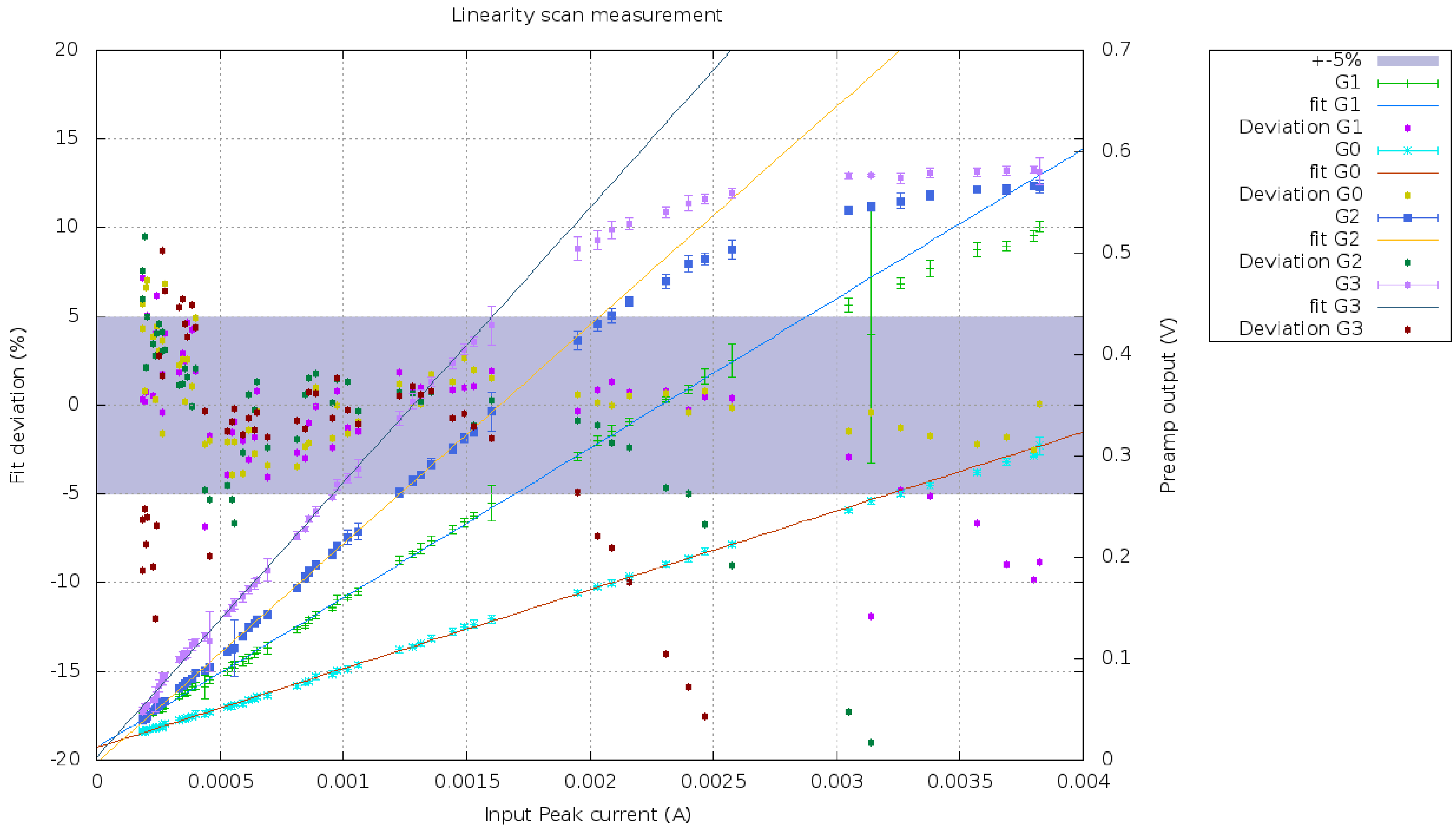
- Gain control and parameters tuned for default shapes:
  - Plotted CC (Current Conveyour output) and SH (Shaper Output)
  - For the 4 possible gains.





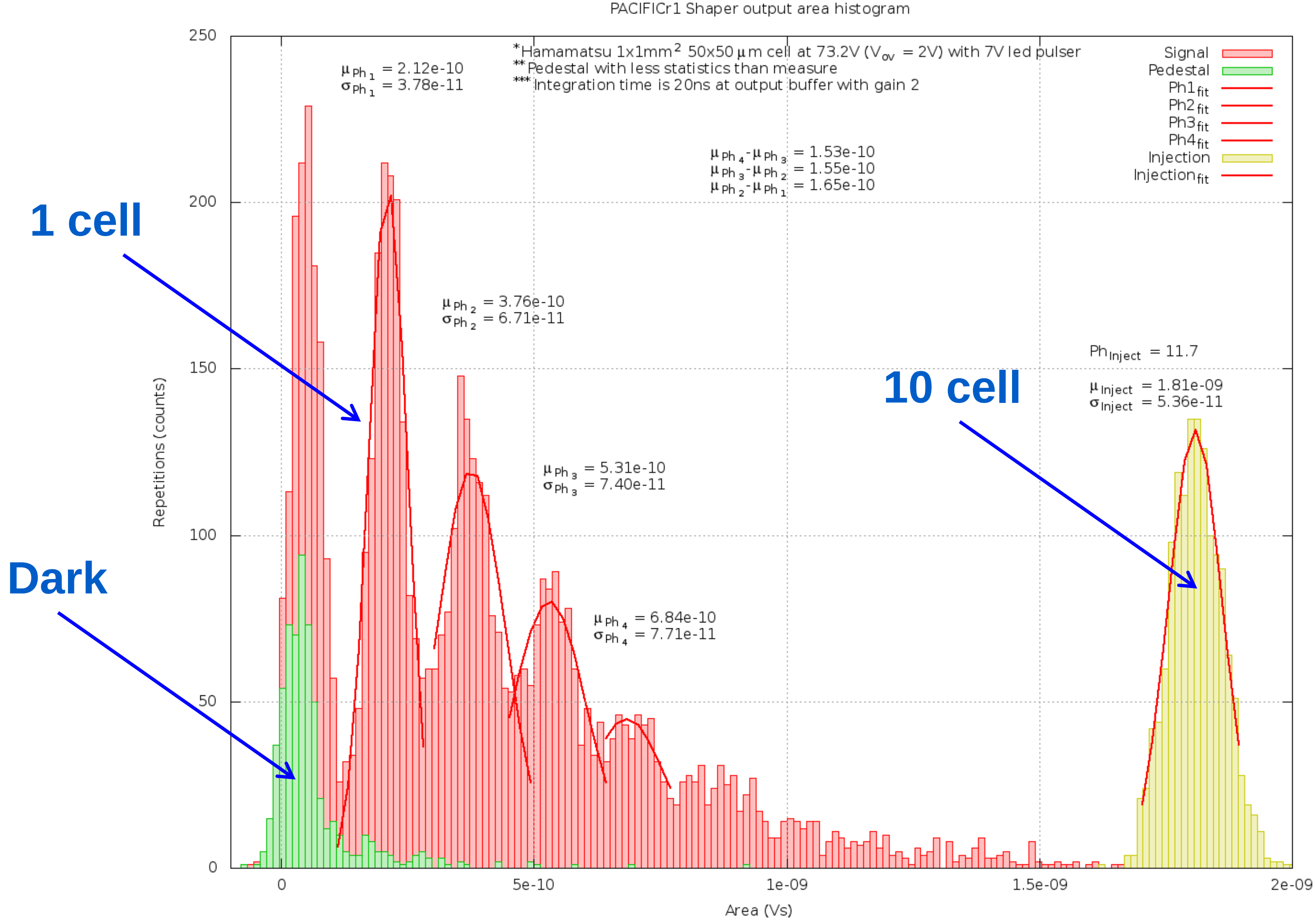
VII. Test results: PACIFIC1

- Good dynamic and linearity for different conveyor gains



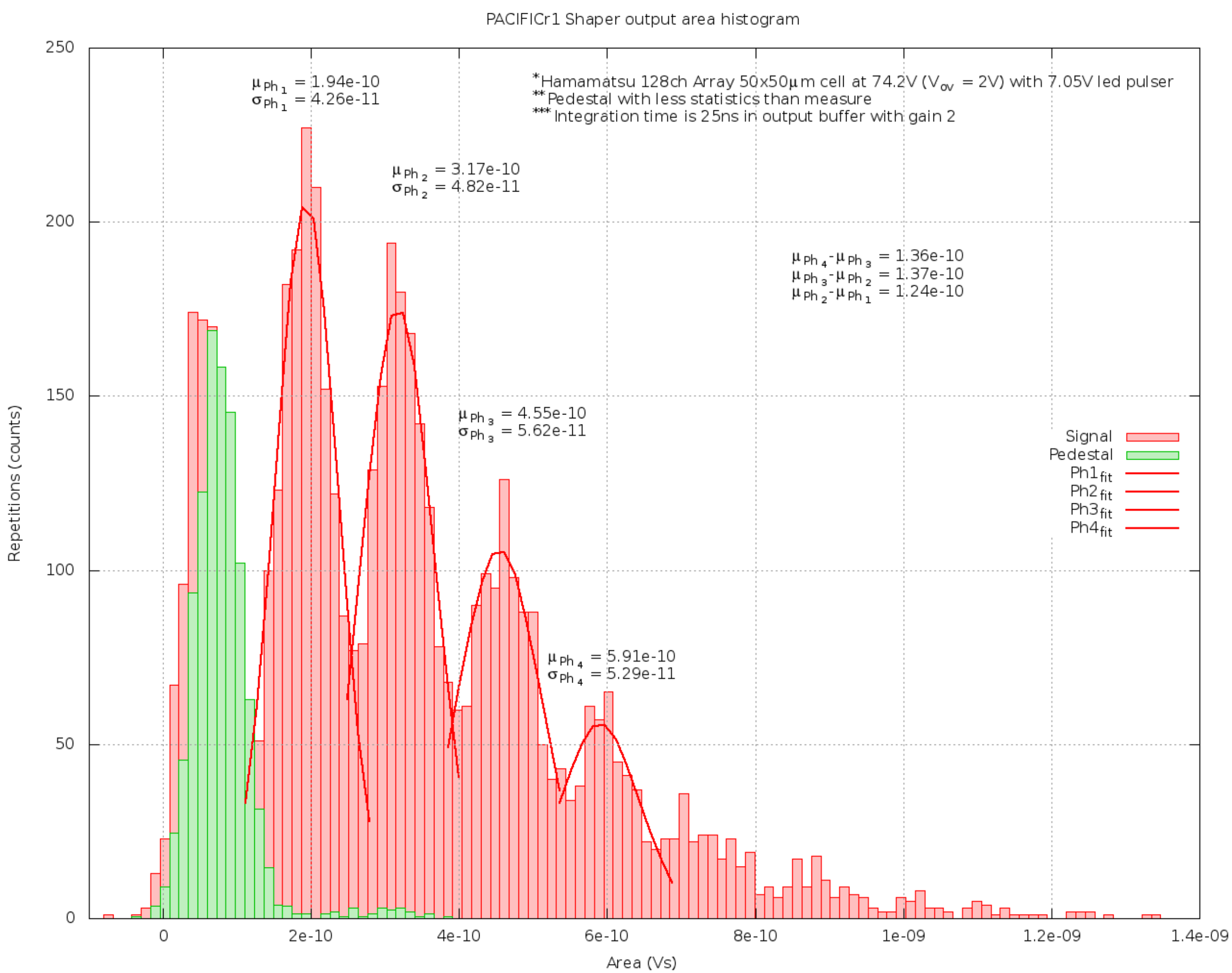
VII. Test results: PACIFIC1

- Charge resolution for an individual SiPM (S10362)
  - Using fast shaper (pole-zero) output through on-chip buffer (gain x1)
  - ***Resolution limited by set-up noise***



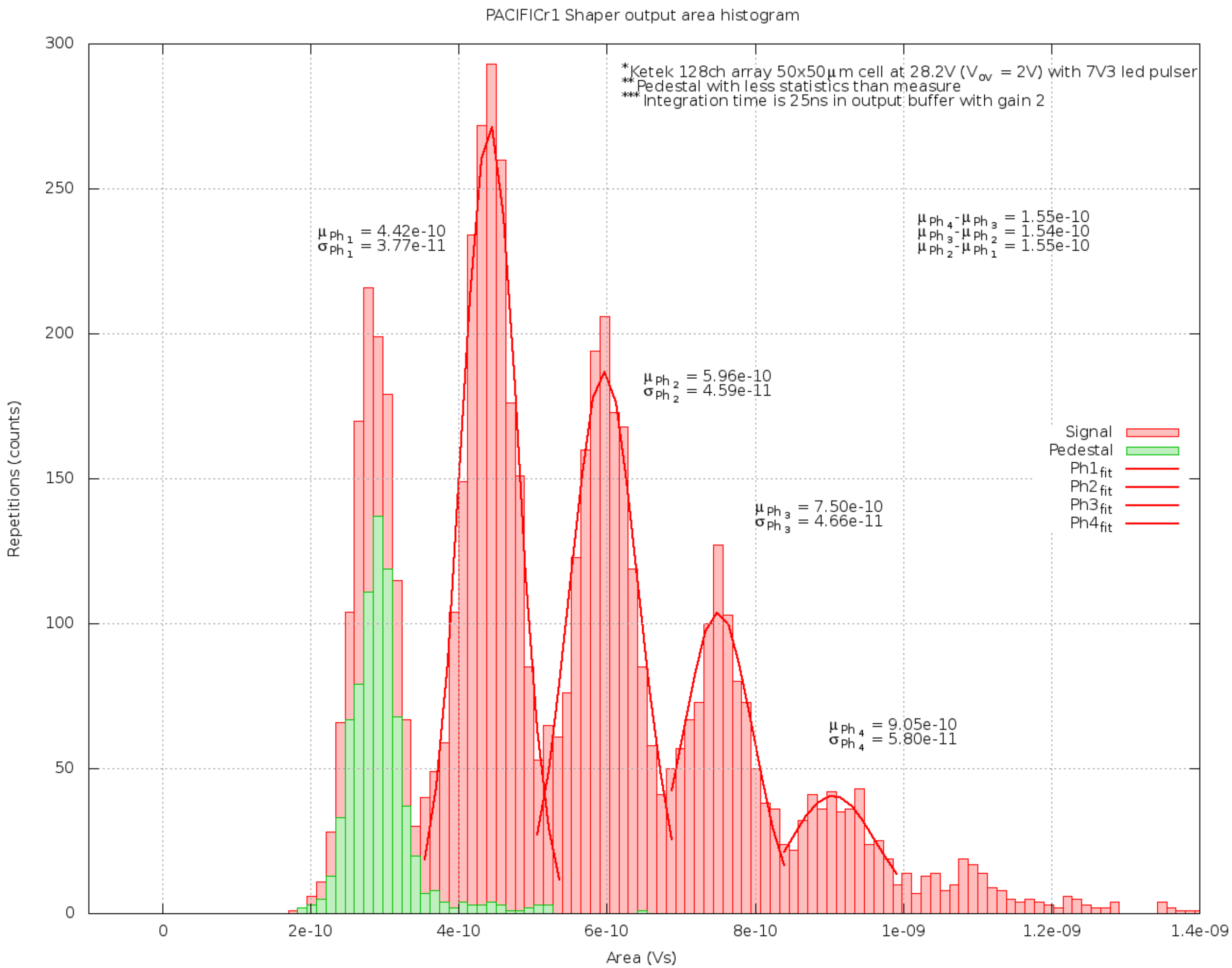
VII. Test results: PACIFIC1

- Charge resolution for Hamamatsu array
  - Tested with flex cable: no oscilation



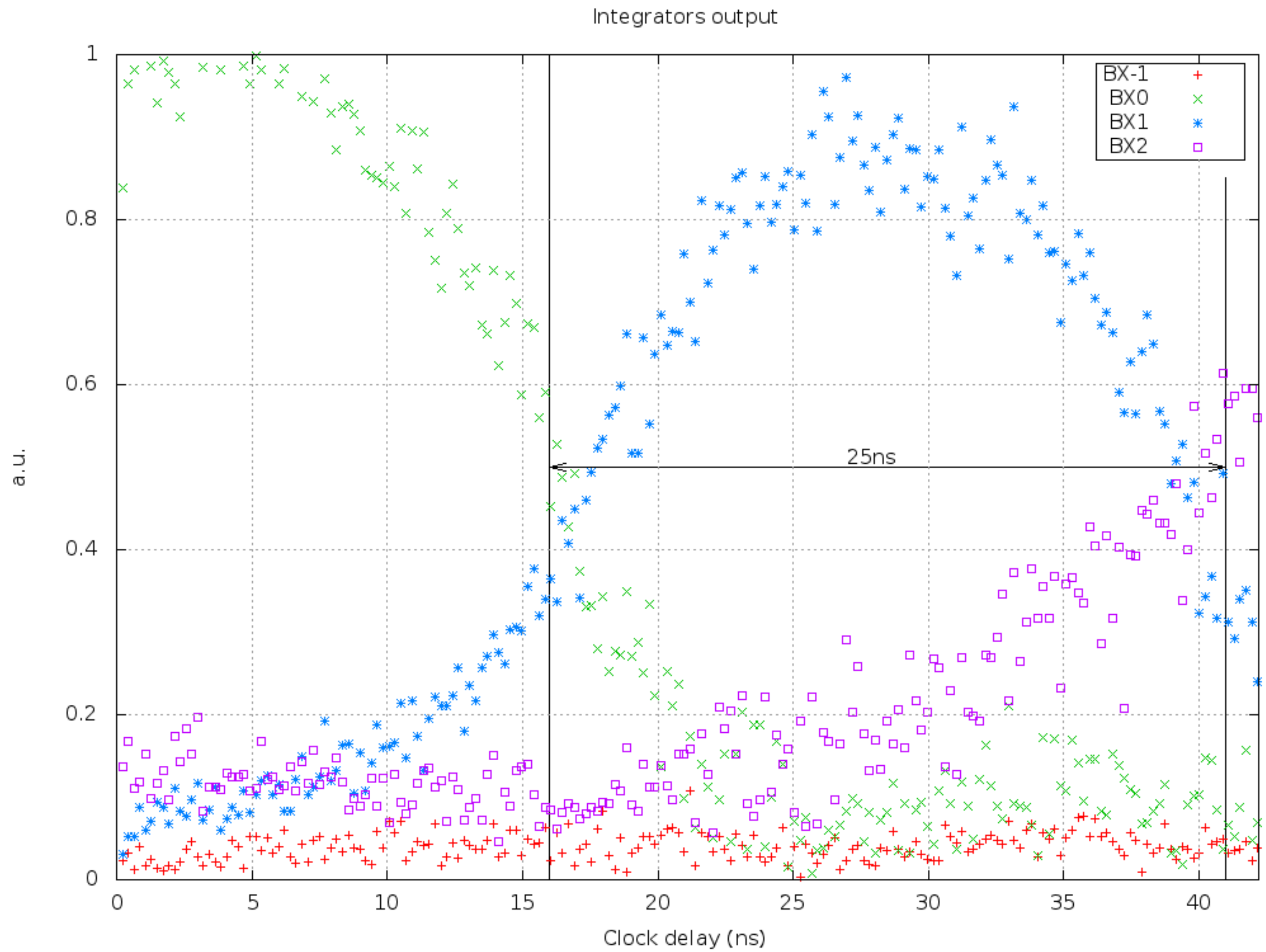
VII. Test results: PACIFIC1

- Charge resolution for Ketek array
  - Tested with flex cable: no oscilation



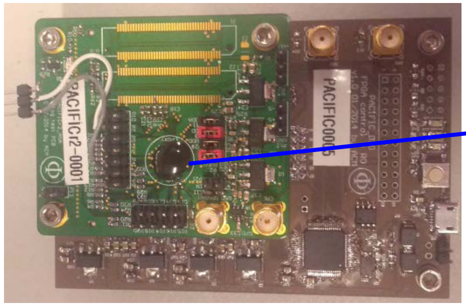
VII. Test results: PACIFIC1

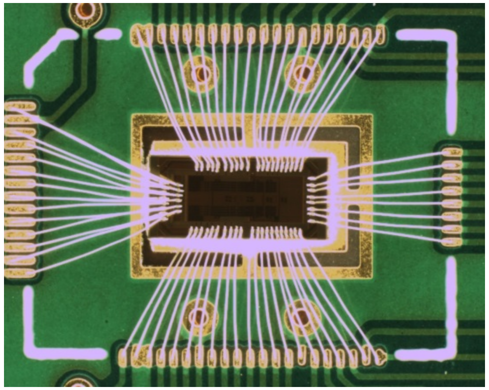
- Dual gated integrator response for typical Hamamatsu pulse as function of delay with respect to the system clock (10 cells signals)



VII. Test results: PACIFIC2

- Test set-up based on 2 PCBs
  - References, I2C, integrator clocks, etc

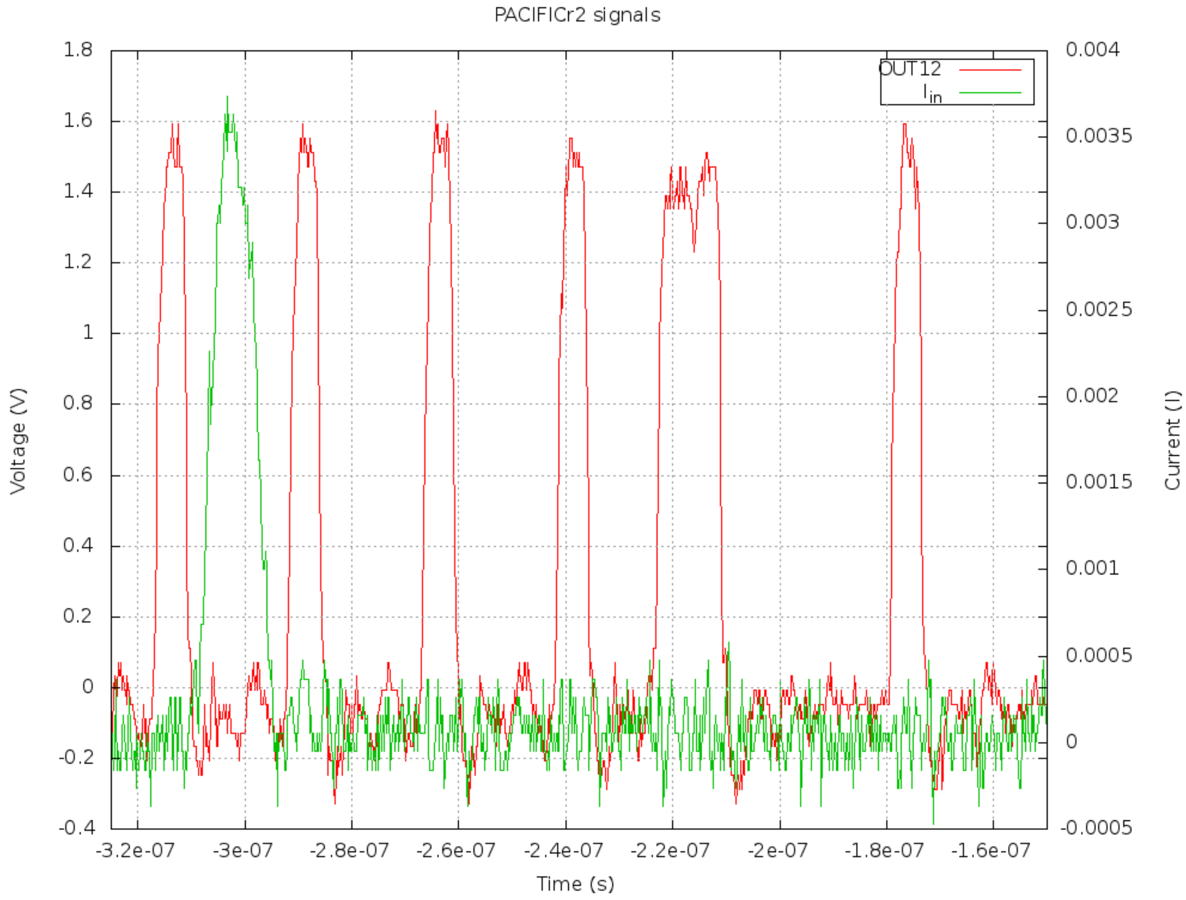




- After correct digital initialization voltages are set
  - Default parameters are set
    - Register hardware presets
  - Voltage references work as expected
- Power consumption as expected on simulations;
  - Consumption around 5mW/channel
- However a mistake in the connection of digital IO pad makes impossible change register values
  - PACIFIC2 has been resubmitted on August (1 week after receiving the proto)
- Despite this…

VII. Test results: PACIFIC2

- PACIFIC2 reacts to input signal as expected for nominal parameters
  - For mid and high threshold bits
  - Lower threshold bit is stuck to 1
    - Default threshold was very low, and cannot be changed
  - Serialization works



I. SciFi Detector
II. SciFi Electronics
III. PACIFIC ASIC
IV. Input stage
V. Shaping
VI. Digitization
VII. Test Results
VIII. Outlook

VIII. Outlook

- PACIFIC is an ASIC designed for fast scintillating fiber trackers
  - Fast shaping time
  - Gated integrator to deal with statistical fluctuations of the signal
  - Pole-zero cancellation to suppress long tails in SiPM signals
  - High degree of tunability of amplifier and shaper parameters:
    - Several SiPM companies
    - Different pulse shape
    - Different operating points
    - Fiber radiation degradation
- Basic analog signal processing is validated
- Detailed performance analysis with digitization requires corrected PACIFIC2 design
- We have started migration to TSMC
  - First designs look very good
  - Main problem will be that MIM capacitance is 4 times smaller
    - Problem for the PZ shaper

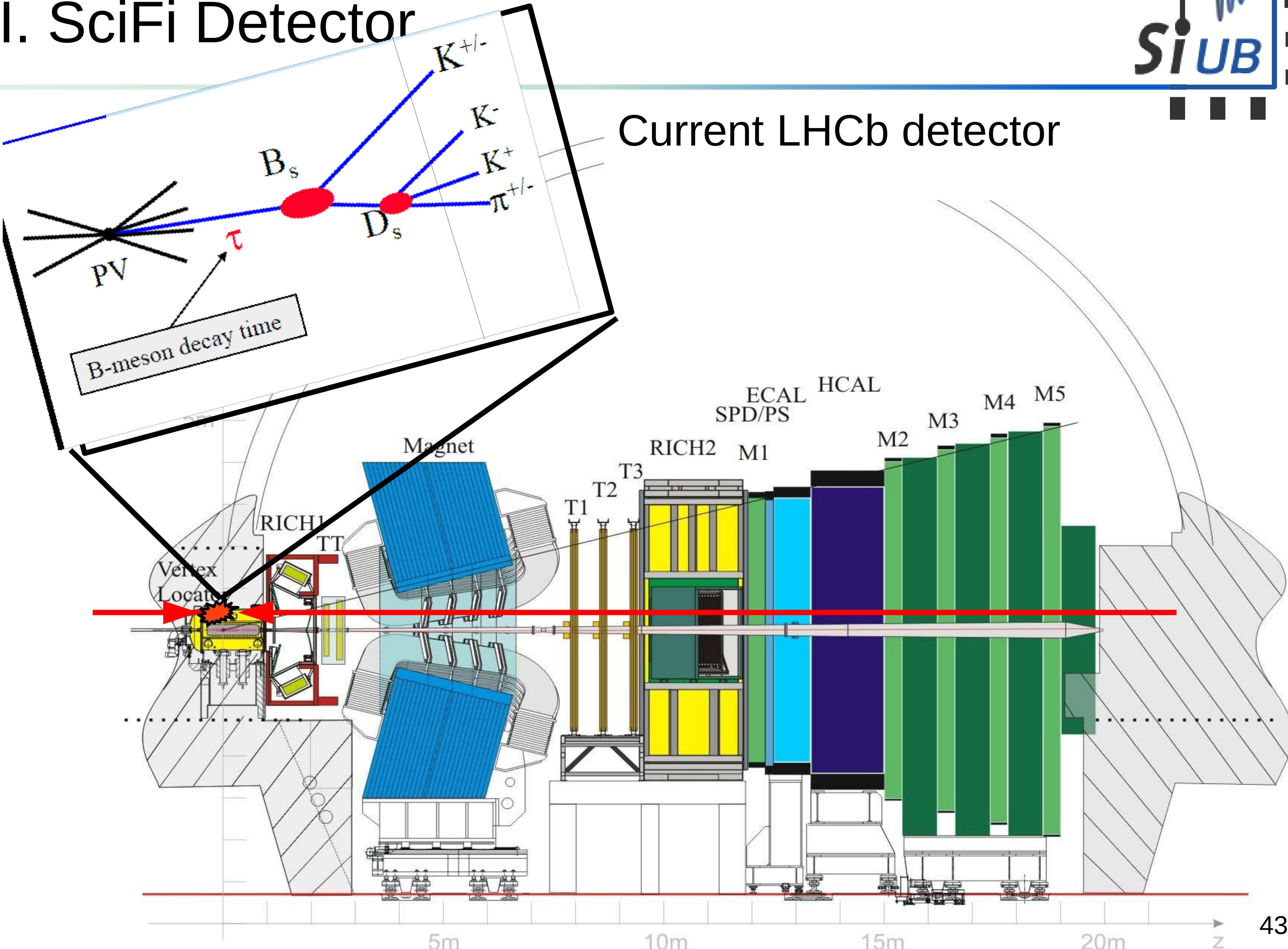
Acknowledgements:

Blake D. Leverington, Fred Blanc, Wilco Vink, Guido Haefeli, Zhirui Xu and many colleagues of SciFi project

Thanks a lot for your attention!

I. SciFi Detector

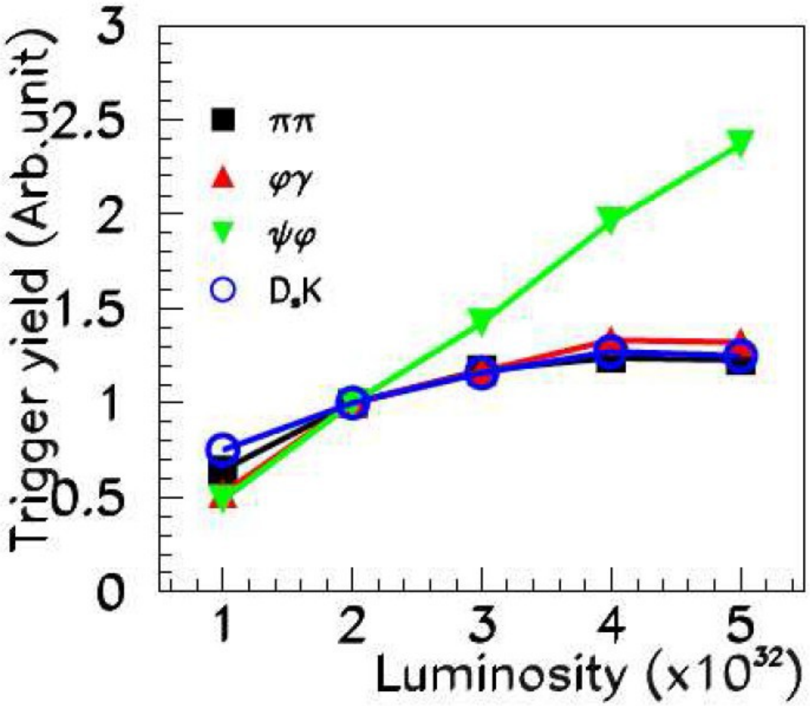
Current LHCb detector



I. SciFi Detector

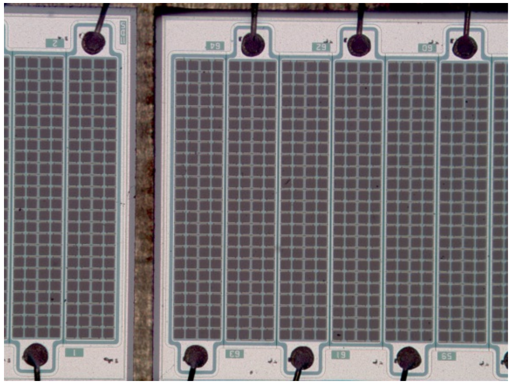
Why LHCb upgrade ?

- Almost every physics measurement in LHCb is limited by statistical uncertainties, not systematic
- LHCb collision rate is tuned to manage data rate (can be increased), but...
- Statistics are limited by the 1MHz hardware trigger rate and then detector occupancy



II. SciFi Electronics: SiPMs

- Demanding SiPM requirements
- High PDE:
  - The 2.5m long fibres and the radiation damage of the fibres in the center of the detector, reduce the light output.
- Low x-talk:
  - The noise cluster rate increases exponentially with x-talk. With the high DCR after irradiation, the noise cluster rate exceeds the acceptable level.
- Support the radiation environment:
  - DCR increases with neutron fluence.
- Small temperature dependence:
  - The operation temperature of the detector is set to -40°C. Temperature non- uniformity is expected for different regions of the detector.
- Small dead regions:
  - Dead regions at the edges between adjacent SiPM arrays reduce the overall hit detection efficiency.
- Thin entrance window!
  - The entrance window defuses the light and therefore the thick window increases the cluster size and makes the spatial resolution worse.
- Right now only two producers can provide suitable SiPMs
  - Hamamatsu
  - Ketek



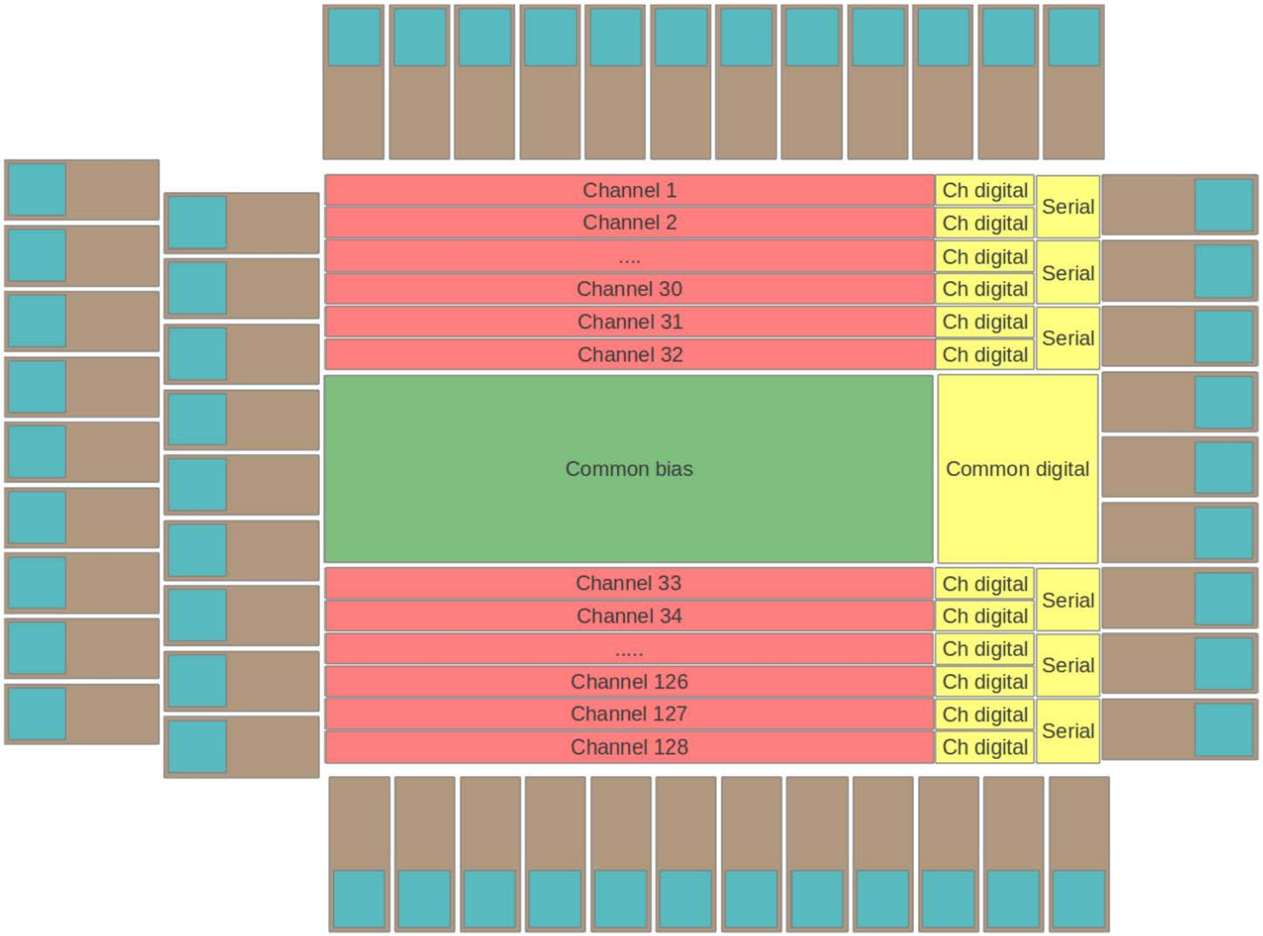
SiPM Flex Cable

Back-up: why 64 channels?

- Starting goal was 128 channels chip, but:
  - SiPMs form factor is 64 channels dies.
  - SiPMs HV will probably be different from die to die.
  - PACIFIC packaging with 128 channels seems difficult.
  - Die size and yeld could be a problem.
- In conclusion 64 channels seems a more natural and easy to handle number for this application.
- Staggered vs standard:
  - Staggered input presents smaller pitch, but...
  - Standard pitch is easily bondable on board by labs or companies.
  - Die rectangular shape does not seem a problem for bonding (for 64 channels).
  - Some isolation (shielding) can be introduced in 80µm pitch to avoid coupled crosstalk.
  - Testing on die would be easier.
- In conclusion standard 80µm pitch input pads seems to be the preferred solution.

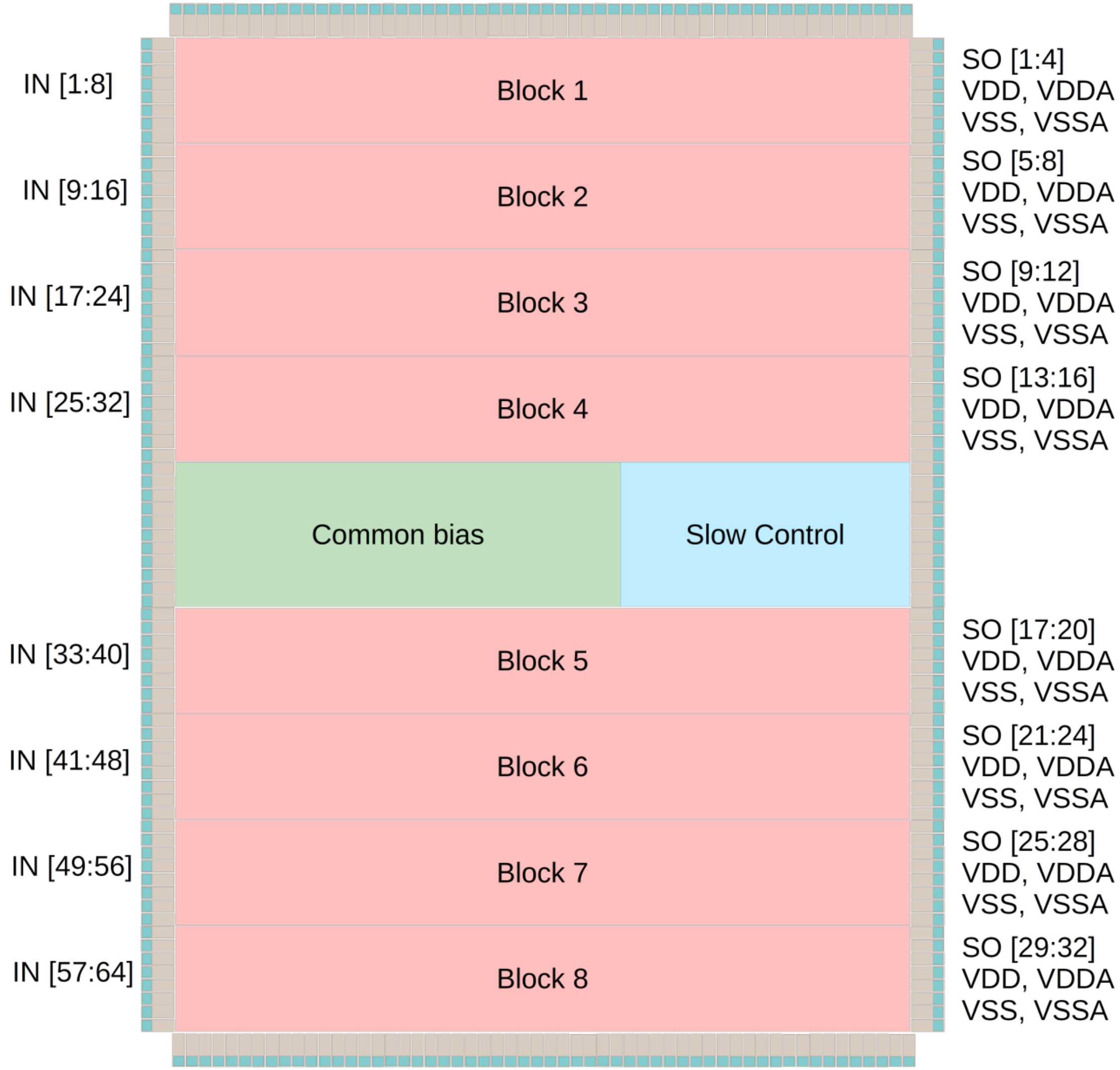
Back-up: why 64 channels?

- Initial 128 ch floorplan (40 um channel pitch)



Back-up: why 64 channels?

- Current 64 ch floorplan (80 um channel pitch)



Input impedance measurement

- Preliminary
- Discrepancy related to process variation on resistors
  - Happens also at low frequency
  - “Vertical” offset (about 5 Ω) wrt to simulations
  - And contributions of PCB parasitics at higher frequency (> 200 MHz)