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PACIFIC: A 128 Ch ASIC for Scintillating Fiber Tracking in LHCb Upgrade

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The design of a 128 channel ASIC (PACIFIC) for the upgrade of LHCb tracker system is presented. The detector will be made of scintillating fibers and read out by 128 channel SiPM arrays. PACIFIC chip will be connected to a SiPM without any external component. It includes analog signal processing and digitization. The first stage is a current conveyor followed by a tunable fast shaper (˜10ns) and a gated integrator. The digitization is done using a 3-bit non-linear flash ADC operating at 40MHz. The power consumption is below 8mW/Ch. The chip will use an 130nm CMOS technology.

Summary

The LHCb detector will be upgraded during the next LHC shutdown in 2018/19. The components of the tracker system will be replaced with new technologies in order to cope with the increased hit occupancy and radiation environment. A detector made of scintillating fibres read out by silicon photomultipliers (SiPM) is studied for this upgrade.

This work discusses the design of the low-Power ASIC for the sCIntillating FIbres traCker (PACIFIC) chip. It will be an 128 channel ASIC which can be connected to a SiPM without the need of any external component. PACIFIC will be low power (< 8mW/channel) and radiation tolerant. The chip will use an 130nm CMOS technology.

The input stage is a current mode preamplifier with the current flowing from the SiPM anode to the circuit. The goal is to achieve the following specifications in this block:
• High bandwidth (≈ 250MHz).
• Low input impedance (20Ω < Zin < 40Ω).
• DC voltage controllable at input node (≈ 0.5V range). It can be used to equalize SiPM response (overvoltage control).
• Good single cell (photoelectron) resolution for calibration.

The input stage is based on a current conveyor based on a novel approach of double feedback and it is optimized for a SiPM array with anode connection. The current conveyor is followed by a closed-loop transimpedance amplifier.
The signal from the SiPM extends over several LHC clock periods. There are two main factors contributing to the long signal tail: light generation and propagation in the fibre and SiPM recovery. The second factor completely depends on the SiPM. A shaper is used to perform tail cancellation prior to gated integration in order to minimize the spill over and the fluctuation of the integrated signal as a function of the signal arrival time.

The implementation consists of a double pole-zero shaper. The First time constant cancels the slowest time constant of the SiPM response, related to internal SiPM capacitances and the quenching resistor. The second one cancels the faster component of the SiPM signal, related to parasitic interconnect capacitance and the input impedance of the preamplifier. It is a closed loop shaper based on the same OTA used for the transimpedance amplifier of the input stage. It is an OTA with > 300 MHz GBW and with high sourcing current capability (fast rising edge), with low power consumption (700 µV). The poles and zeroes are tunable, and they have been calculated to be able to operate with the very different time constants of the two types of SiPM considered for the detector.

The integrator is the block located between the shaper and the A/D converter. In order to fit with the dispersion of the time of arrival of the signal in the 25ns window, two complementary integrators will be implemented. A closed loop baseline restoration is used to control the DC operating point at the input of the integrator. The digitization is done using a 3-bit non-linear flash ADC operating at 40MHz.

Simulation and test results will be presented.

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