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Development of the Read-out ASIC for Muon Chambers of the CBM Experiment

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A front-end ASIC for GEM detectors readout in the CBM experiment is presented. The design has the following features: dynamic range of 100 fC, channel hit rate of 2 MHz, ENC of 1000 e- at 50 pF, power budget of 10mW per channel, area efficient 1.2 mW at 50 Msps 6 bit SAR ADC. The chip includes 8 analog processing chains, each consisting of preamplifier, two shapers (fast and slow), differential comparator and SAR ADC. The chip also includes the threshold DAC and the digital part.

Summary

An 8-channel mixed-signal ASIC for muon chambers of the CBM experiment was designed and fabricated in a 0.18 um CMOS process.
GEM muon chambers will have projective segmentation with the smallest pad size being as small as 4.1 x 4.1 mm2 in the inner region and as large as 2.1 x 2.1 cm2 in the outer region of the chamber. The detectors will be operating at a high gas gain in the range of 1000 to 8000. This set up the following ASIC features:
- dynamic range of 1-100 fC;
- wide Cdet range of 1-50 pF;
- S/N maximization at the periphery pads;
- hit rate up to 2 MHz at the central pads;
- low (less than 10 mW/ch.) power consumption;
- area efficiency for all building blocks and ADC as the most critical one.

The block diagram and the design results for main building blocks are presented. This design was taken as a starting point (functional prototype) for a 64-channel circuit, to be developed according to the rad-hard by design technique.
The ASIC was designed and prototyped via Europractice by means of the 0.18 um CMOS MMRF process of UMC. The die size is 3240 x 1525 um2. The chip has 90 pads. ESD were added to all front-end pads as well as to control ones. The chip was packaged in CPGA120.
The chip block diagram includes 8 analog processing chains, 2 threshold DACs, 8 SAR ADCs and a digital part. Each analog channel contains the preamplifier, followed by two shapers (fast and slow) and differential comparator.
The preamplifier is based on the folded cascode CSA architecture with additional gain boosting. The preamplifier gain is 5 mV/fC and its noise level is estimated by ENC = 1000 el at 50 pF.
Since CBM MUCH GEMs will have different granularity, the requirements set to the front-end electronics, are also different in the central and peripheral parts. Thus, the preamplifier is followed by two chains: a slow channel optimized for S/N ratio in order to use it in the periphery, and a fast channel, adapted to the hit rate of the inner detector part, where the occupancy is the highest. Both channels are realized with CR-RC shapers with different peaking times, 60 ns and 260 ns accordingly. The shapers in both channels are finished by drivers, which make a single-ended to differential signal conversion. Then the signals are supplied to the differential comparator inputs.
The SAR ADC has a 6 bit resolution, an asynchronous internal clock. It is capable to operate at a maximum sampling rate of 50 Ms/s at a power consumption of 1.2 mW. The ADC area is 0.0255 mm2. The ADC switch

logic utilizes the dynamic D flip-flops to lower power consumption.
The digital part provides DAC codes loading, the control signals “start of conversion”for ADC, output data storage and synchronization functions.

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