Contribution ID: **70** Type: **Poster**

Clock and Data Recovery Implementation and Testing for the Readout Control Unit 2 in ALICE TPC.

Wednesday 24 September 2014 17:19 (1 minute)

A new readout control unit for the ALICE TPC in Run-2 - the RCU2 - has been designed in order to increase data throughput and radiation tolerance. Since the TTCrx ASIC project is disbanded, new ways to recover clock and data was implemented and tested. Two methods have been applied, one using the internal fabric resources of the SmartFusion2 FPGA and the other using a commercial component, the ADN2814. Clock jitter from the SmartFusion2 recovery method has shown comparable results as the TTCrx jitter performance. However, neither of the solutions performed well enough under radiation to be applicable for the RCU2 without major modification.

Summary

The present ALICE TPC readout electronics are readout and controlled by a total of 216 Readout Control Units (RCUs). The RCU communicates with all sub-systems, amongst other the Trigger, Timing and Control (TTC) system, of which provides each RCU with the 40.08 MHz LHC clock, used as a system clock for the TPC readout electronics. The LHC clock and the trigger data are sent over the TTC fiber using 80 Mb/s Time Division Multiplexed BiPhase Mark encoded signal. It is important to have a radiation tolerant solution to recover the clock with low jitter and with a predefined phase-offset to the LHC input clock. Presently, this is handled by the TTC receiver (TTCrx) ASIC sitting on the RCU.

Since the TTCrx is obsolete, new methods for Clock and Data Recovery (CDR) were considered for an upgrade of the existing Readout Control Unit for the ALICE TPC. The intention of the RCU2 is to double the readout rate and improve the radiation tolerance of the readout chain. The main FPGA of the RCU2 is the flash-based Microsemi SmartFusion2 SoC FPGA. The CDR solution is required to be radiation tolerant in our environment and with a clock jitter performance better than specified by the physics of the TPC.

This paper presents two implementation methods for CDR: (1) custom design in the fabric of the SmartFusion2 FPGA, and (2) by use of a commercial CDR IC (Analog Devices ADN2814). Since the configuration elements in the FPGA are flash-based, the SmartFusion2 is regarded radiation tolerant in our environment. The methodology for the clock recovery in the FPGA is dependent on a constant, linear delay. Post place and route simulations for SmartFusion2 have shown that creation of on-chip delay using a chain of buffers give irregularities in rise and fall times of the digital signal. These irregularities are traced back to wire length and logical element's unequal drive strength. The paper shows how this can be compensated for, giving constant delays for both rising and falling edges. Additionally, tight area constraining has been applied to ensure consistency in phase and jitter. Jitter measurements show that the performance is comparable to the TTCrx at an optimum of optical input power. The implementation using the commercial CDR IC is also proven on the RCU2 outside of radiation, where the clock and data is recovered without errors.

During radiation campaigns of the SmartFusion2 FPGA stand alone, the radiation tolerance of the custom CDR implementation is shown to be acceptable in our environment. However when irradiating the optical receiver, the CDR becomes unstable since it is not able to cope with the noise on the input signal coming from radiation effects of the photodiode in the optical receiver. For the commercial CDR chip in radiation the failure rate is at the same level as for the custom FPGA solution.

Based on these results, and on the fact that a large enough spare batch of TTCrx ICs came to our knowledge, a second RCU2 prototype have been designed that includes the TTCrx.

Primary author: TORGERSEN, Christian (University of Bergen (NO))

Presenter: TORGERSEN, Christian (University of Bergen (NO))

Session Classification: Second Poster Session

Track Classification: Trigger