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PEALL4: A 4-channel, 12-bit, 40-MSPS, Power Efficient and Low Latency SAR ADC

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The PEALL chip is a Power Efficient And Low Latency successive approximation register (SAR) ADC candidate designed for the upgrade of the ATLAS experiment at the CERN LHC. The full functionality of the converter is especially achieved by an embedded high-speed clock frequency conversion generated by the ADC itself. The design and test results of the PEALL chip implemented in a commercial 130nm CMOS process will be presented. The size of this four-channel ADC, with embedded voltage references and sLVDS output serializer, is 2.8x3.4 mm2, while the total power dissipation is less than 27mW per channel.

Summary

With the increased instantaneous LHC luminosity expected beyond 2019, the ATLAS calorimeter trigger system will have to be fully redesigned. The new architecture will especially include a first level decision implying fully digital information. The new trigger digitizer board is the key electronics board to be built by this time. Installed in the front-end crates of the ATLAS LAr calorimeters, its main duty is to digitize each channel at the 40MHz sampling rate and prepare the data to be transmitted by optical links. It will host a high performance analog digital converter (ADC) characterized by a 12-bit dynamic range, low power consumption and low latency. This ADC is also supposed to sustain the harsh radiation conditions expected until the end of the LHC.

Several options are currently considered for the choice of the ADC. One of them consists in a successive approximation register (SAR) ADC named PEALL with the following characteristics: 4 channels, short latency (less than 40ns), 12-bit resolution, 40 Msamples/s sampling speed and low power consumption (below 27 mW per channel). The input dynamic range of the converter is 2V over an analog power supply of 1.5V. One innovative feature of this chip is a high-speed clock internally generated by the ADC from a regular external 40MHz clock. In comparison to a classical SAR ADC design, this feature helps to save a significant amount of power. The SAR ADC is based on a switched capacitor DAC segmented in two to reduce the total value of the capacitors seen by the input nodes during the sampling phase, and also to reduce the total area of the chip. Since this segmentation could create non-linearity and distortions, a trimming capacitor is added to compensate.

A four-channel prototype with embedded analog voltage references and LVDS output provided from the chip was produced in December 2013 in a commercial 130nm CMOS process. It is thoroughly tested since then. The preliminary results indicate a Total Harmonic Distortion (THD) of –60dB and a Spurious-free dynamic range (SFDR) of 60dB at the design frequency of 40MSamples/s. The behavior in terms of Single-Event-Effect (Single-Event-Upset and Latch-up) sensitivity will be tested in June 2014 at the Louvain cyclotron.

The talk will present the current performance achieved, as well as plans for improvement in a future version already under design.

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