ATLAS Tile Calorimeter Electronics and Future Upgrades

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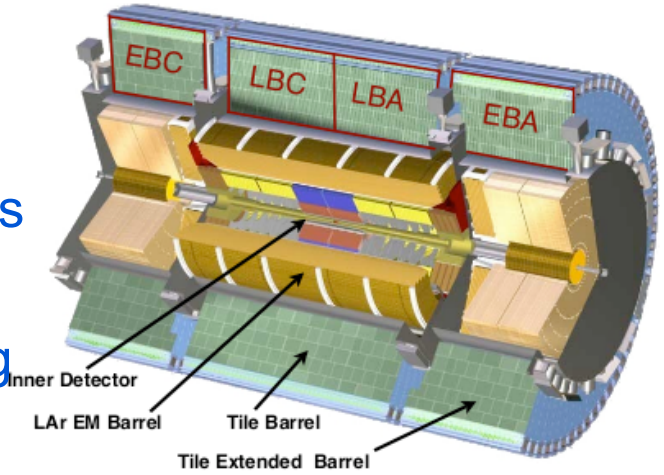
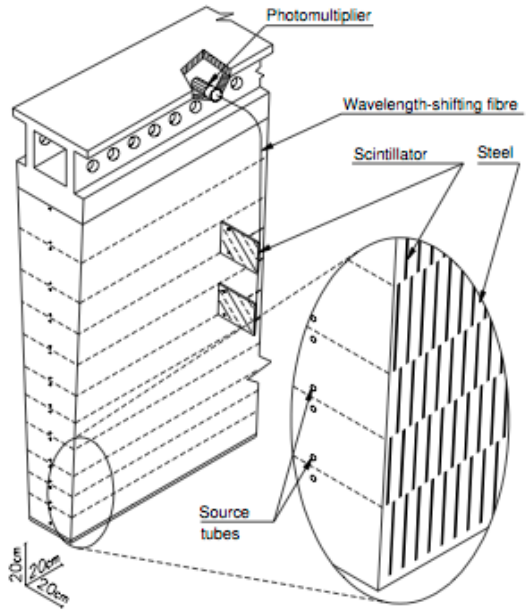
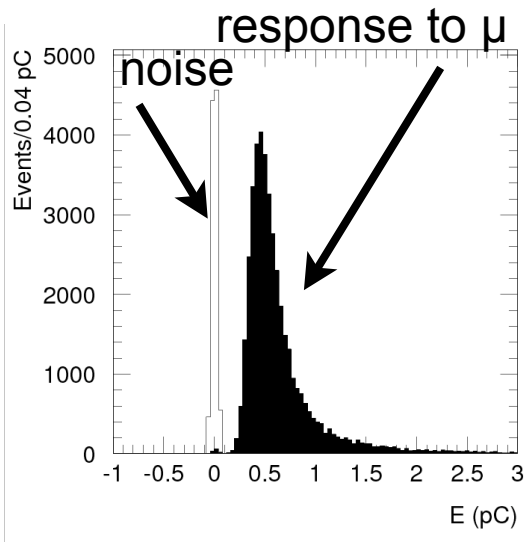
(on behalf of the ATLAS Tile Calorimeter system)

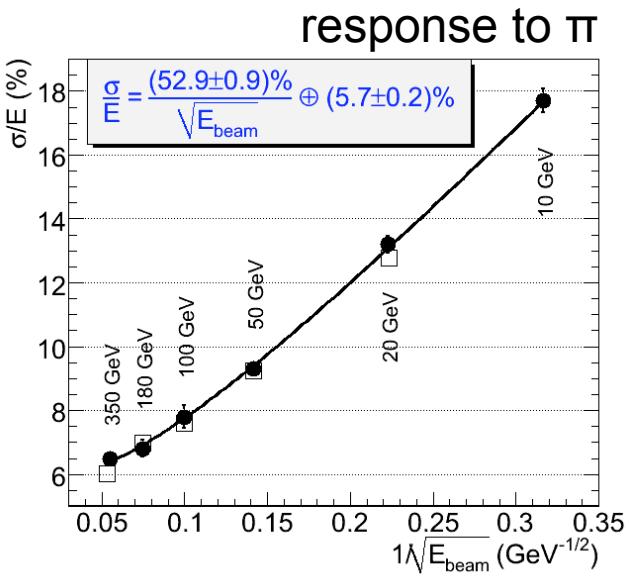
The ATLAS Tile Calorimeter

- is the central hadronic calorimeter made of plastic scintillator tiles and steel. Measures hadrons and jet energy and direction
- the scintillators are read out on opposite sides by two PMTs using WLS fibres
- PMTs and FE electronics mounted in 3m long drawers (Super-drawers) at the outer radius

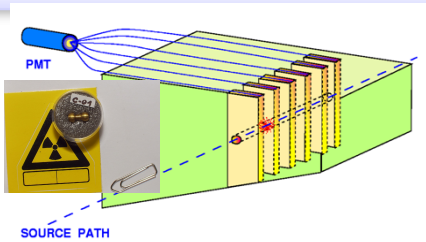








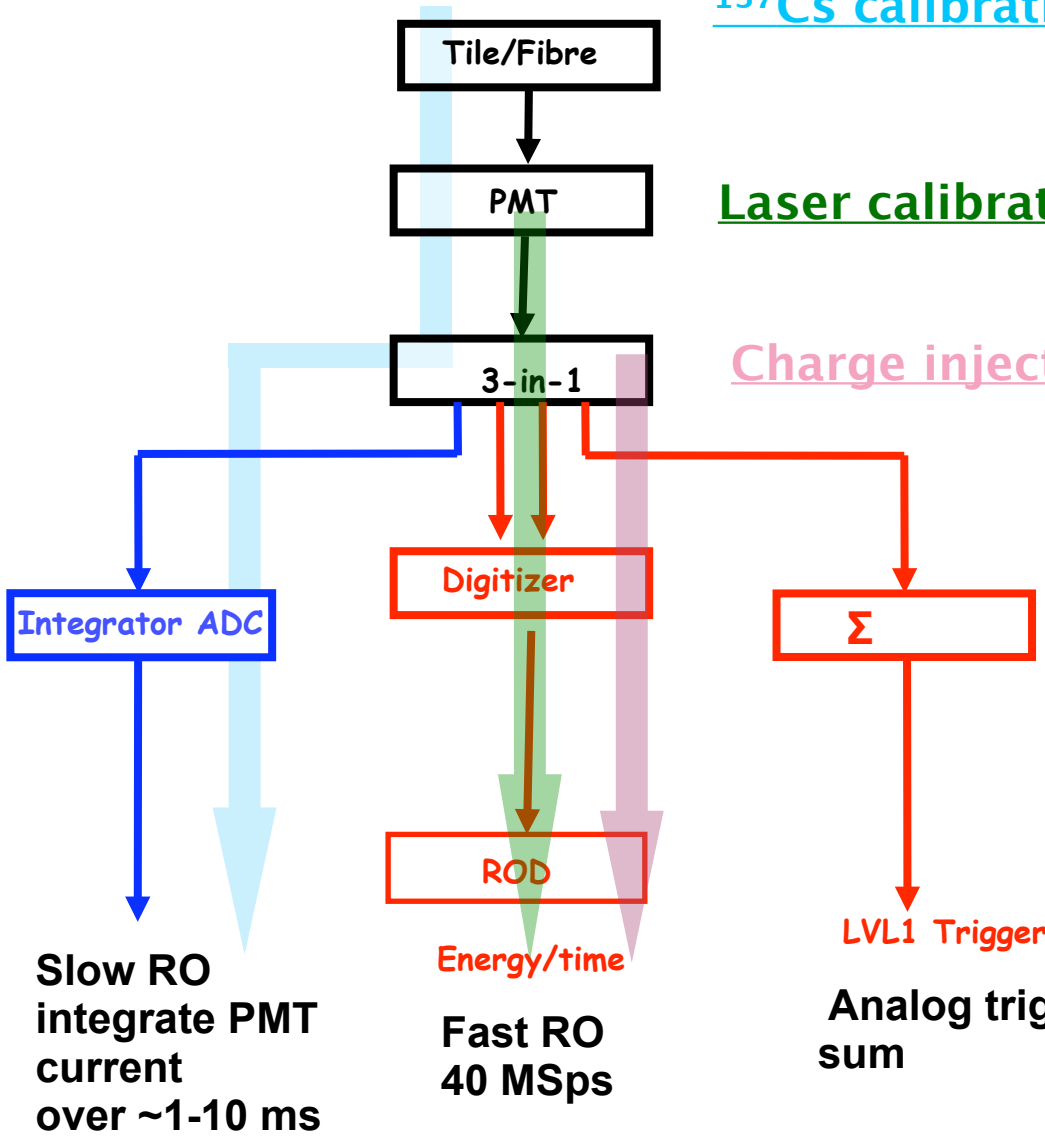
Read-out and calibration concepts



^{137}Cs calibration

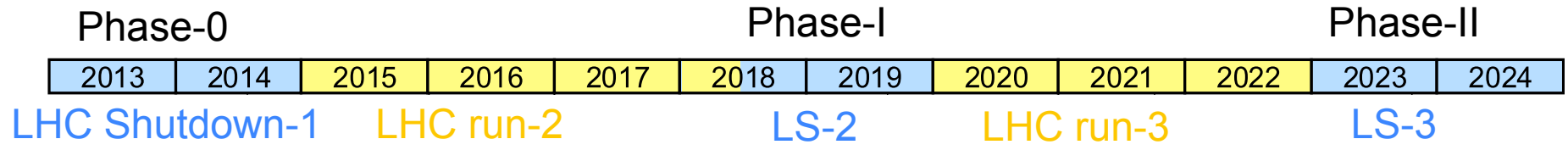
Laser calibration

Charge injection calibration



- Analog trigger sum for LVL1 trigger
- digital readout, 16 bit dynamic range obtained using a bi-gain chain with 10 bit ADCs
- DC integrator read-out for calibration and Luminosity Monitor

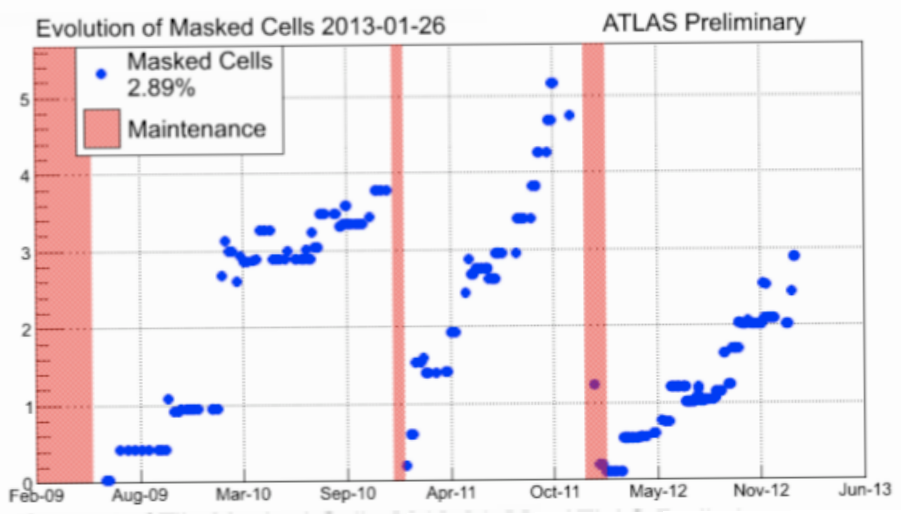
Tile Calorimeter upgrades timeline

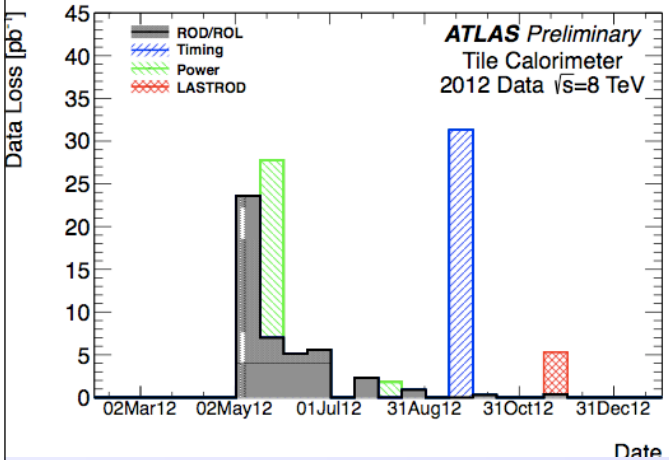


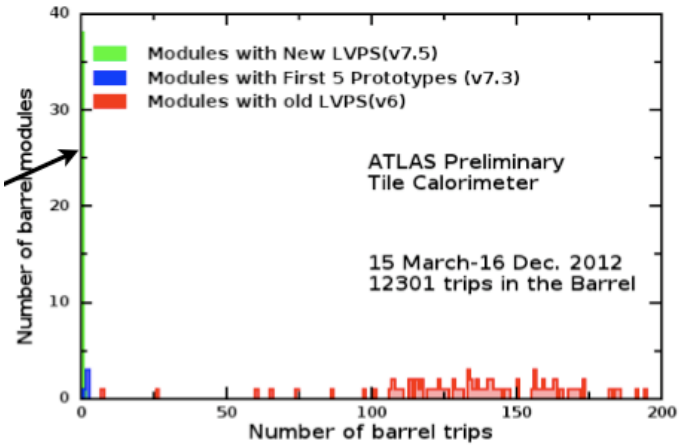
- Run-1 (2009-2012): redesign LVPS on test 40 units
- Phase-0 (2013-2014): install the new LVPS, new MBTS, maintenance of FE boards, Tile 3rd layer in the Muon Trigger logic in $1.3 < |\eta| < 1.5$
- Phase-I (2019): replacement of gap scintillators
- Phase-II (2023): complete upgrade of the FE and BE electronics
  - discussed in this talk

Operation & experience during run-1

- permanent failures in the read-out:
  - PS and power distribution
  - severe errors in data/signal transmission
- temporary failures:
  - 15k PS trip
  - loss of configurations
- Data taking inefficiency: contribute ~9% to ATLAS inefficiency



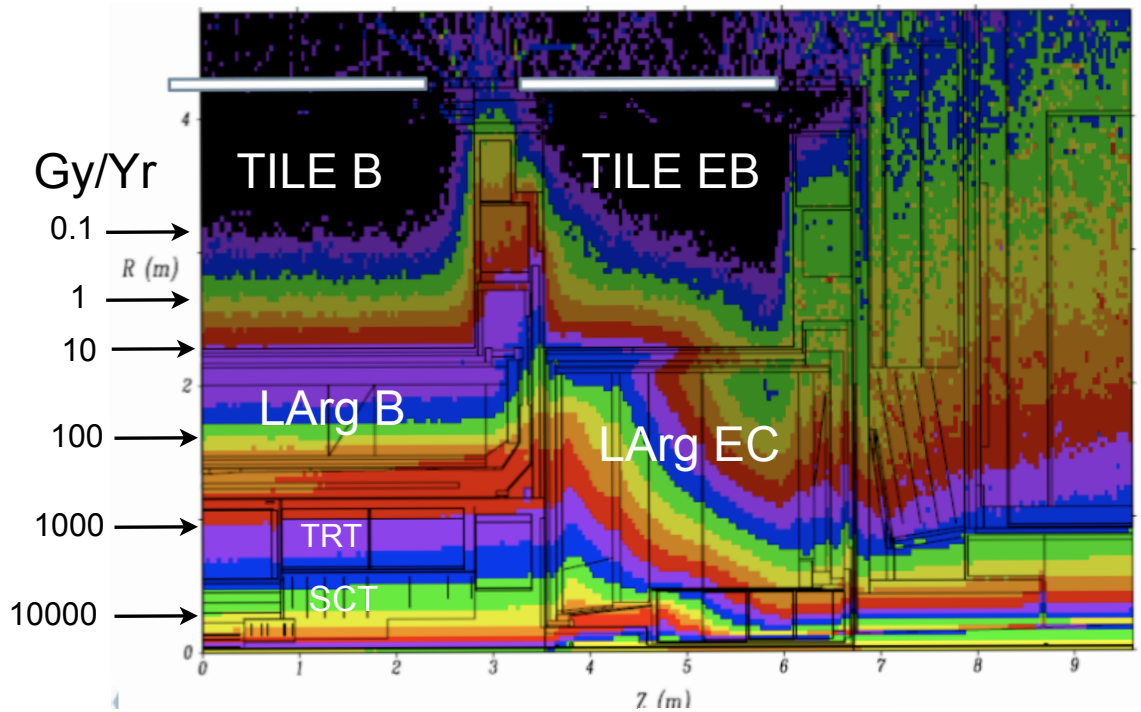




Motivations for the Tile upgrade

- LHC upgrade in 2023 aim for a luminosity of (5-10)*10^{34} $cm^{-2}s^{-1}$
  - better radiation tolerance is desirable
  - increased interaction rate demands for a better precision and finer granularity in the trigger
- ageing of components
  - exceeding the design lifetime
- improve the reliability
  - reduce/simplify the maintenance needs
- improve the accessibility
  - ALARA considerations

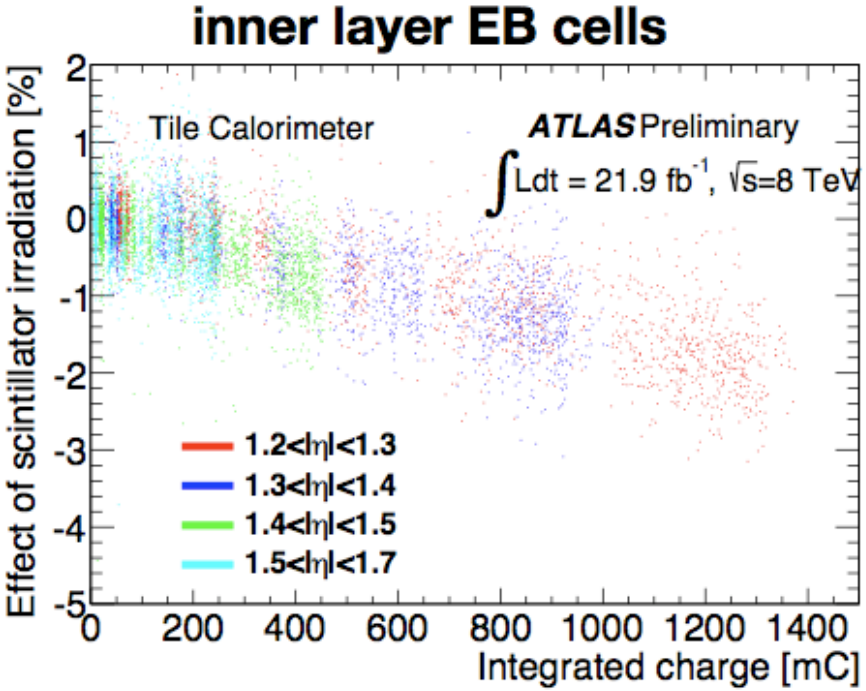
TID simulation (design Luminosity)

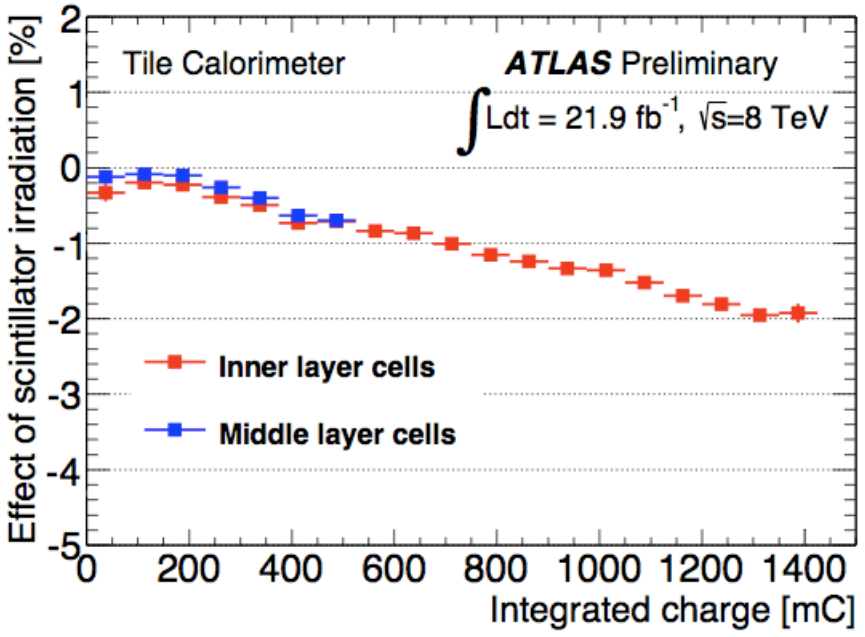


Phase 2 Radiation Tolerance Requirements (Estimate), TileCal HV_Opto					
Type	**Simulated Dose/Yr**	**Simulation Safety Factor**	**Low Dose Rate Safety Factor**	**Lot Variation Safety Factor**	**Total 10 Year Operation**
TID	8.13E-01 Gy/yr	1.5	5	4	2.44E+02 Gy
NIEL	7.62E+10 n/cm^2/yr	2	1	4	6.10E+12 n/cm^2
SEE	1.85E+10 p/cm^2/yr	2	1	4	1.47E+12 p/cm^2

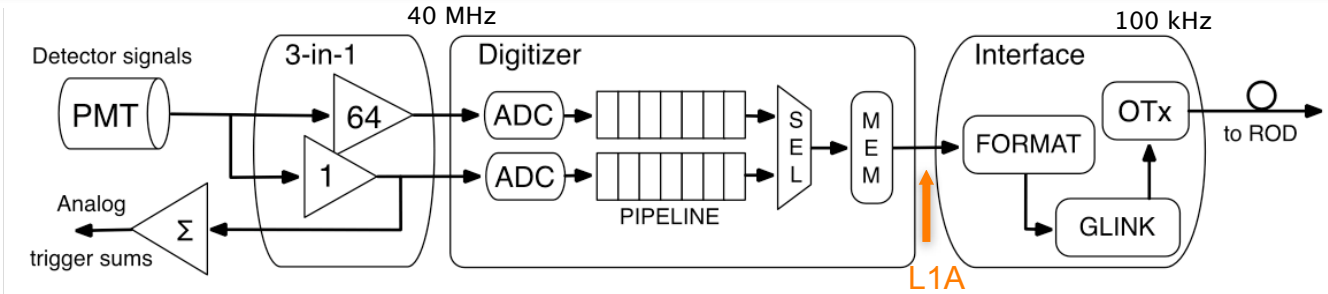
Irradiation effects on scintillator

- difference between the Cs (Minimum Bias) and Laser response is interpreted as the effect of the irradiation on the scintillator:≤ 2% for the worst case cells
- Cell light budget is fairly large (~70 phe/GeV), a factor X2 loss is expected not to be critical. Detailed study ongoing



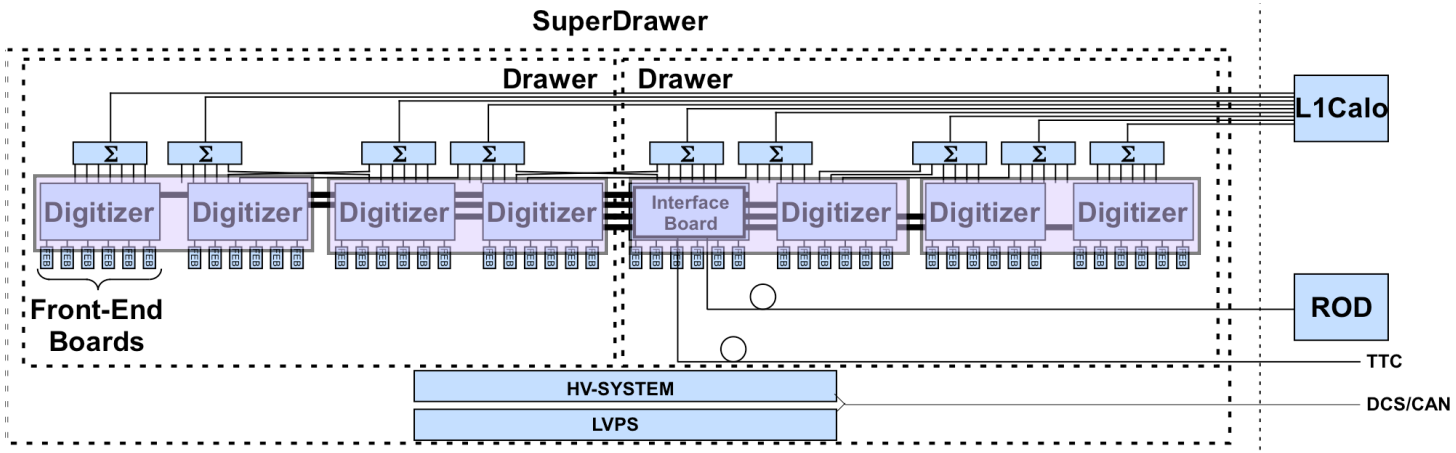


Present read-out system

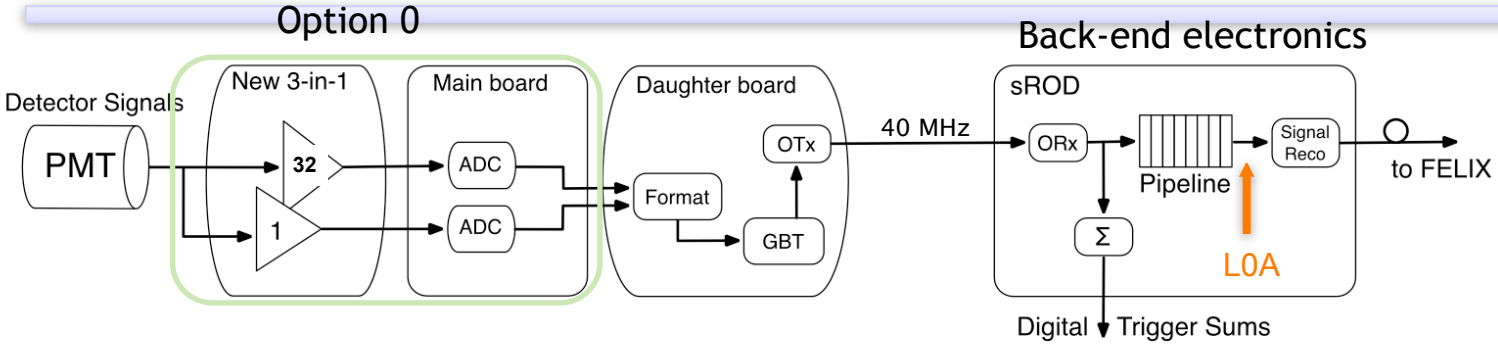


- 3-in-1 FE board: shaping, amplification, integration
- Mother board: programing and powering of FE boards
  - int ADC, TTCrx, trigger summing boards, CANbus
- Digitizer cards:TTCrx,Digitization at 40MSps, pipelines
- Interface card: Otx to the ROD, TTC Orx

Total data rate	~165 Gb/s
Number of links	256 (+256)
Data rate per link	640 Mb/s
Links per super-drawer	1 (+1)

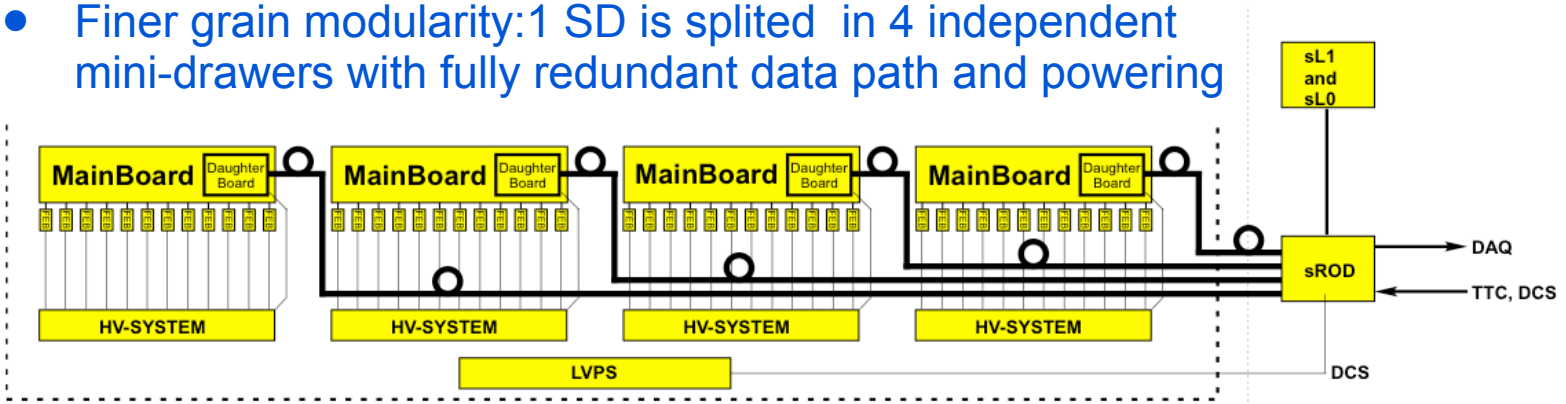


Future read-out system



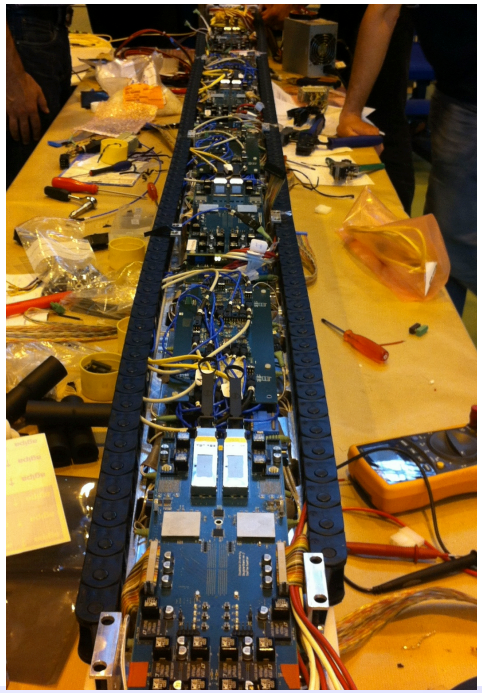
- Simplification: reduced no. of boards and less inter-connections
- Daughter board: high speed optical communication for transmission of full data at 40 Mbps to the sROD in USA15
- Pipelines and de-randomizers in the sROD, control and monitor. Digital information for the LVL0/LVL1 Trigger system
- Finer grain modularity:1 SD is splited in 4 independent mini-drawers with fully redundant data path and powering

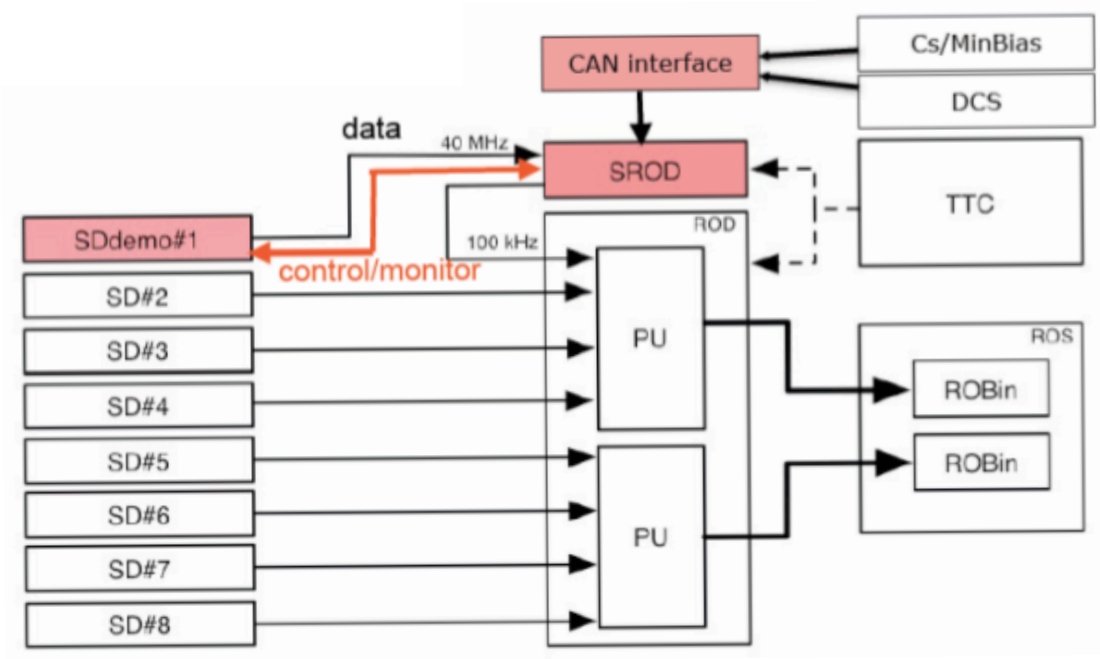
Total data rate	~80 Tb/s
Number of links	4096 (+4096)
Data rate per link	10 Gb/s
Links per Duper-Drawer	4x4 (+4x4)
Data rate per SD	160 (+160) Gb/s



The demonstrator project

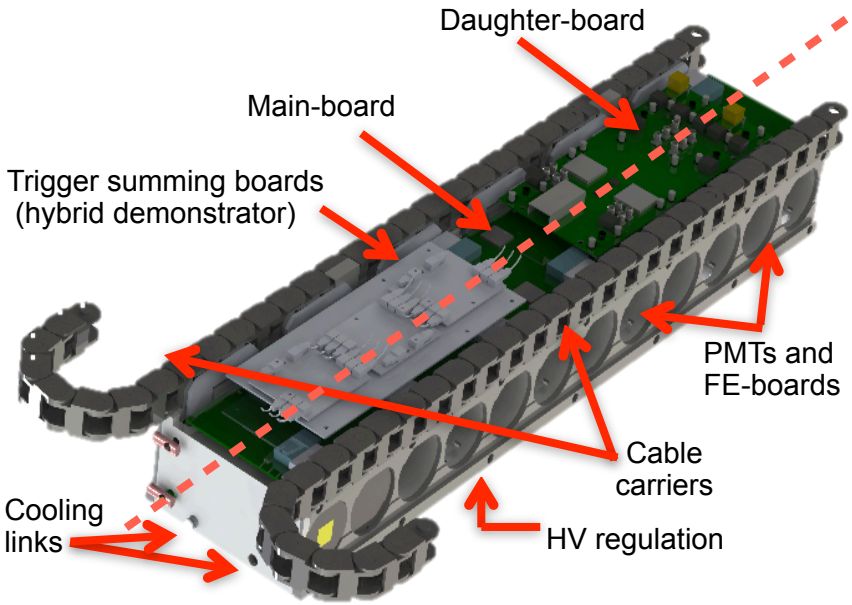
- Hybrid slice of the future system to be integrated asap in the current detector to evaluate the design/technology.
  - As similar as possible to the phase-II system but maintaining full compatibility with the current system.
  - receive TTC/CANbus commands from sROD
  - send data to the ROD trough the sROD
  - provide both analog and digital trigger output

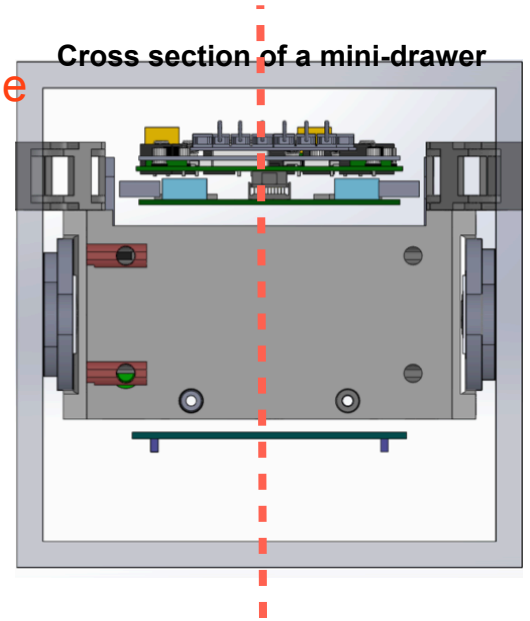




Mini-drawers

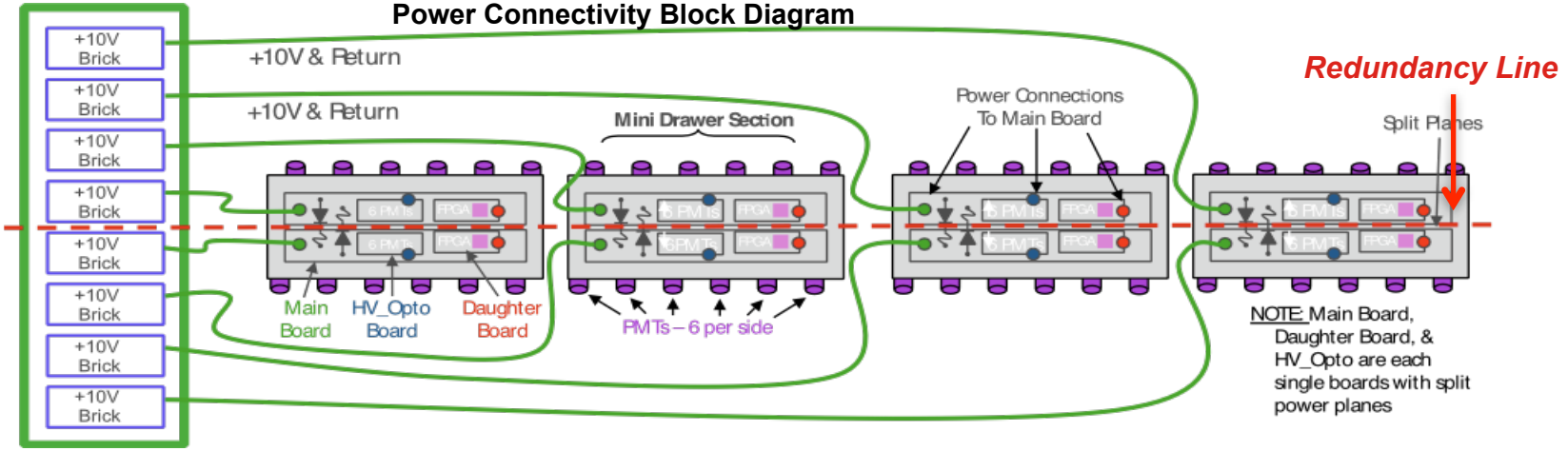
- The Super-drawer will be spit further to simplify the handling and allow acces in partial detector opening
- 4 independent mini-drawers, each one with 2 independent read-out sections:
  - 12 PMTs and FE boards reading out 6 cells. (3-in-1 or other 2 future options)
  - 1 main-board: for the corresponding FEB option
  - 1 daughter-board: single design
  - 1 HV regulation board: HVOpto or HVRem options
  - 1 adder base board + 3 adder cards: only for hybrid demonstrator



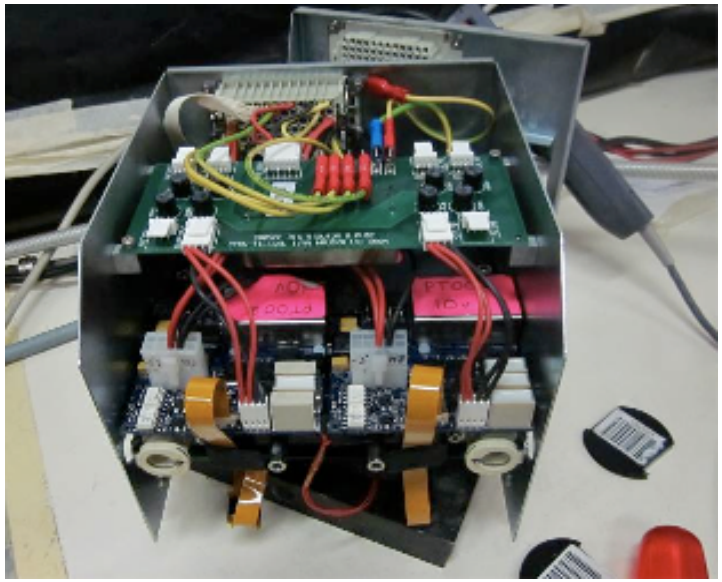


Low Voltage Power Distribution

Now
+5V MB
-5V MB
+15V MB
+5V DG
+3.3V DG
+15V HV
+5V HV
-5V HV

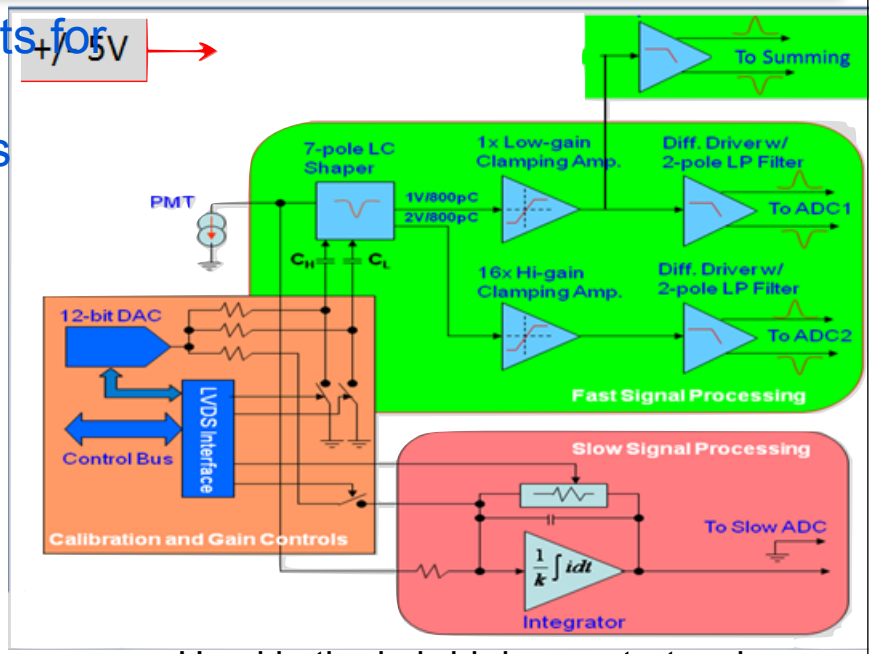


- three-stage power distribution system
- bulk 200VDC PS in USA15
- "finger LVPS": custom evolution of the used DC/DC converter
  - 8 separate units providing only +10V
  - Each unit powers half of a mini-drawer but can power both for redundancy (diode OR)
  - first unit fully operational
- Point-of-load regulators
  - mounted on Main Board, Daughter Board and HV Opto
  - Completed TID tests on 5 COTS regulators, marginal results for -5V regulator
  - NIEL and SEU tests to be done in December 2014

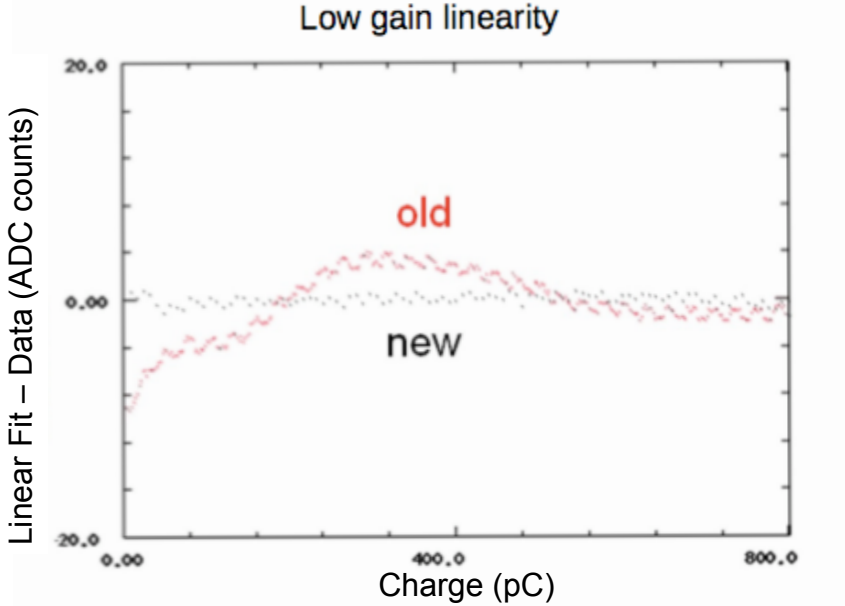


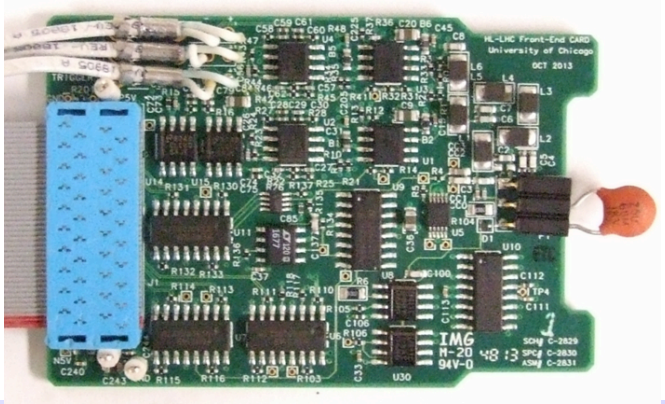
3-in-1 FE board

- Based on current FE. Only analog components for shaping and integration:
  - High/Low gain and trigger analog outputs
  - Charge injection calibration
  - Integrator read-out
- higher radiation tolerance
- improved noise performance
- improved linearity performance
- prod.version manufactured and qualified.



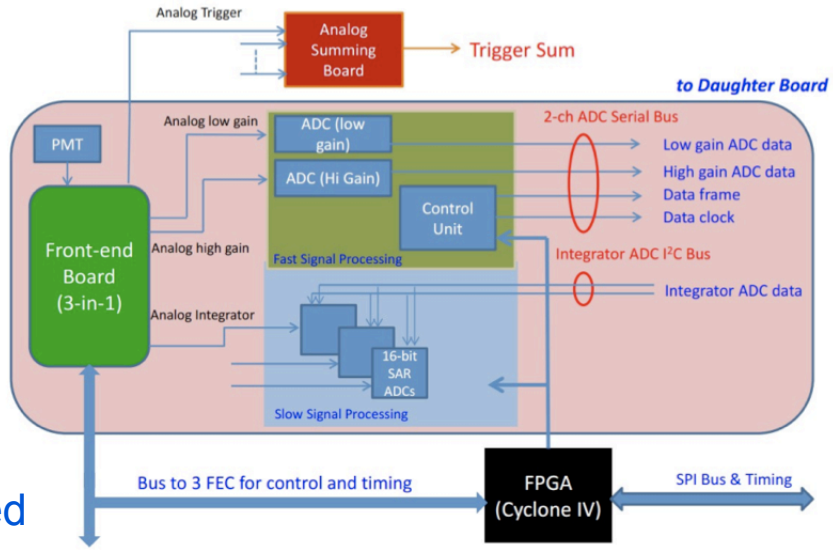
Used in the hybrid demonstrator,since provides analog output to the LVL1 trigger

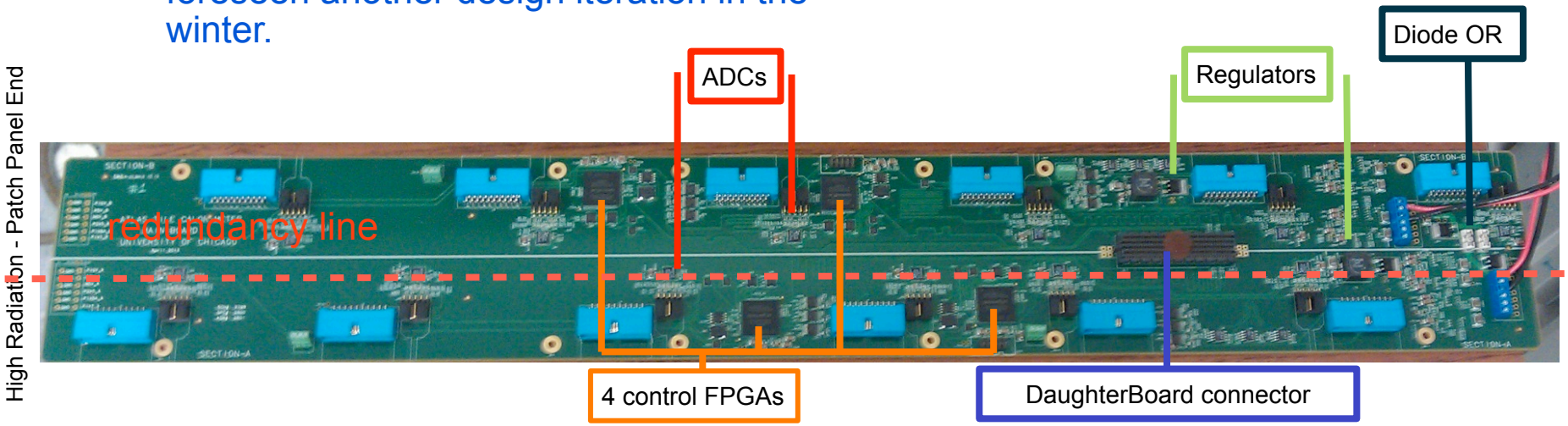




Main-board for new 3-in-1 FEBs

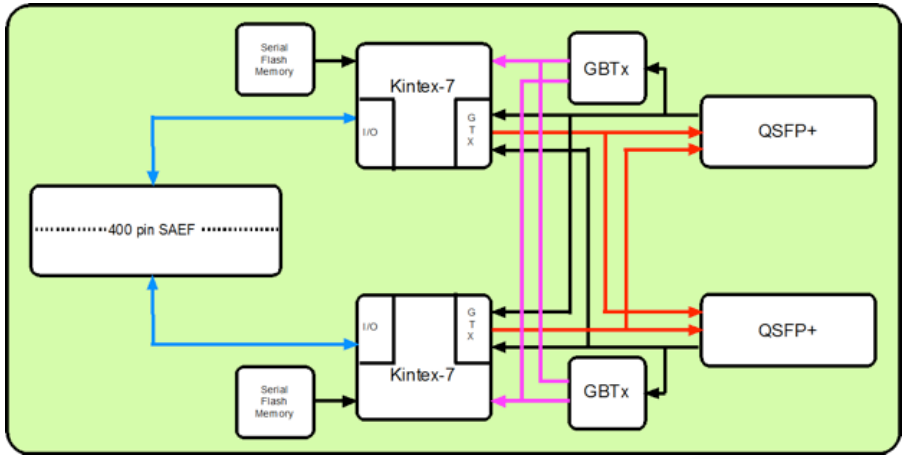
- Made of two completely independent sides. Power included.
- Local voltage regulator (±5V ,+2.5V,1.2V),
- FPGA for clock distribution control and monitoring of 12 FEBs (6 on each side)
- ADCs for HG/LG and integrator FEB outputs
- LVDS communication to the daughterboard at 560 MHz
- Status:
  - version 3 manufactured and validated. Used in the first demonstrator prototype. We foreseen another design iteration in the winter.



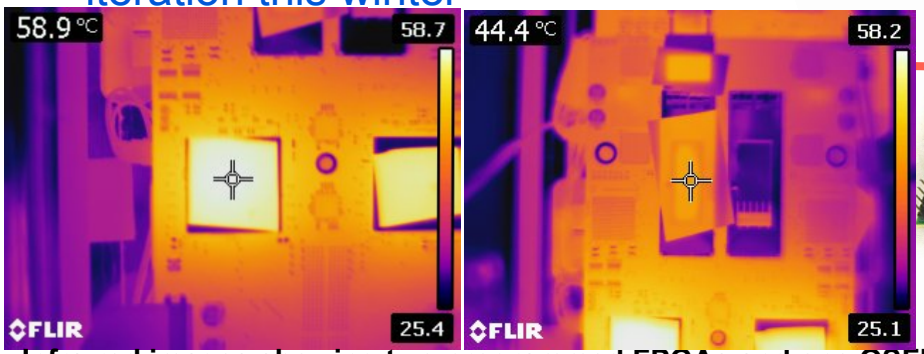


Daughter-board

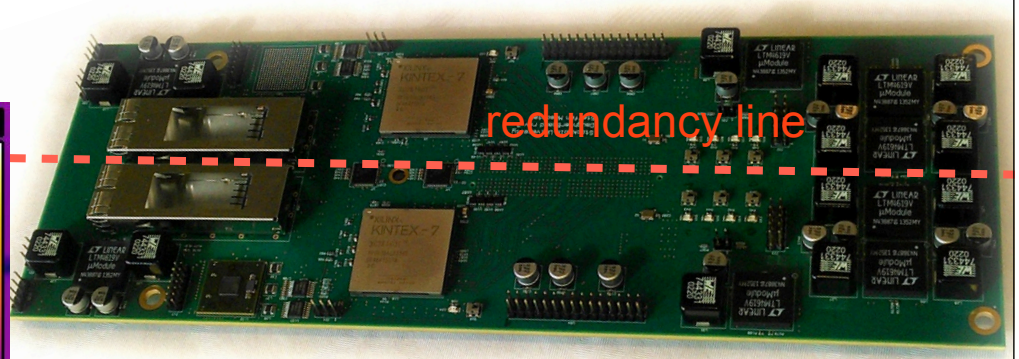
- provides high speed communication with the back-end electronics
  - collects format and transmits the read out and DCS data.
  - receives and routes commands and configurations from ROD and DCS
  - two completely independent sides with Kintex-7 FPGA, QSFP, GBTx
  - uses triple redundant FPGA programming, scrubbing and partial reconfiguration
  - Firmware can be uploaded through the optical link
- Status: Produced 4+4 units of the third version. We foreseen a further design iteration this winter



Conceptual design of daughter-board (third prototype)



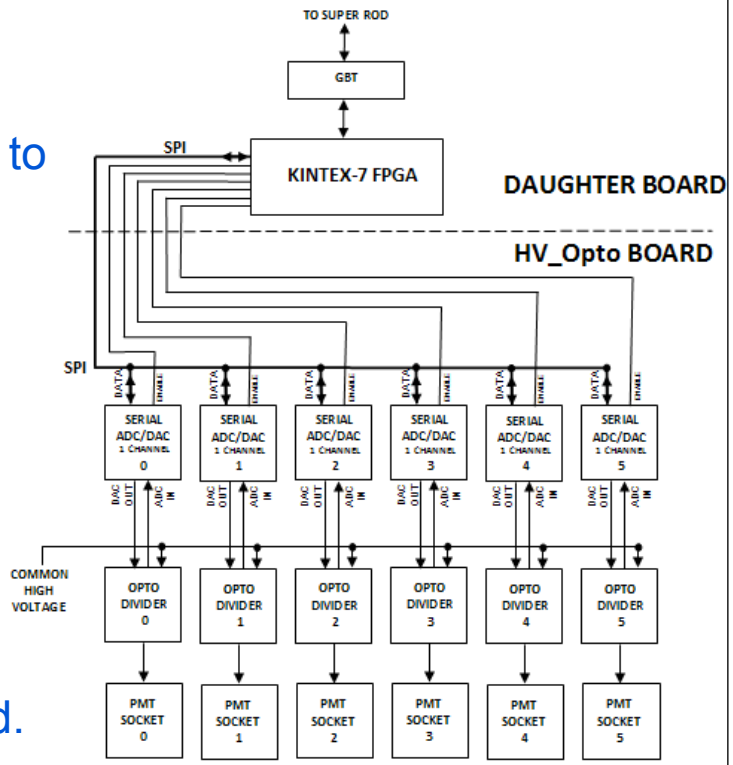
Infra-red images showing two programmed FPGAs and one QSFP



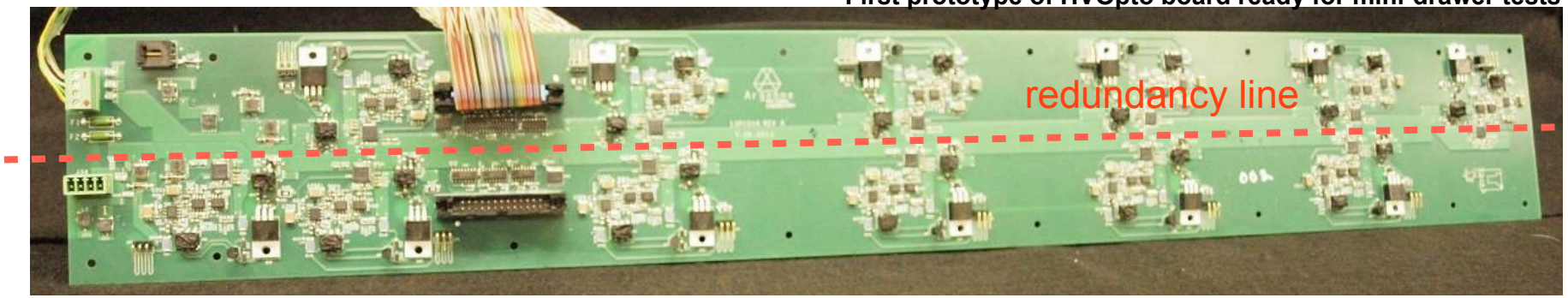
daughter-board (third prototype)

High voltage regulation & distribution

- two options under investigation: remote (HVRem) and local HV regulation (HVOpto)
- HVRem: the existing local regulation system is moved to USA15 and individual cables are routed to the PMTs. First prototype built, under testing.
- HVOpto: largely based on the existing system use Kintex-7 FPGA in the daughter board for control of HV settings and monitoring
  - Introduce possibility of switching on/off individual PMTs
  - First 4 boards tested and performance meets specifications
  - First TID,NIEL,SEU tests show no hard failures. Sensitivity in some components being investigated. Mitigation of the observed SEU seems viable.

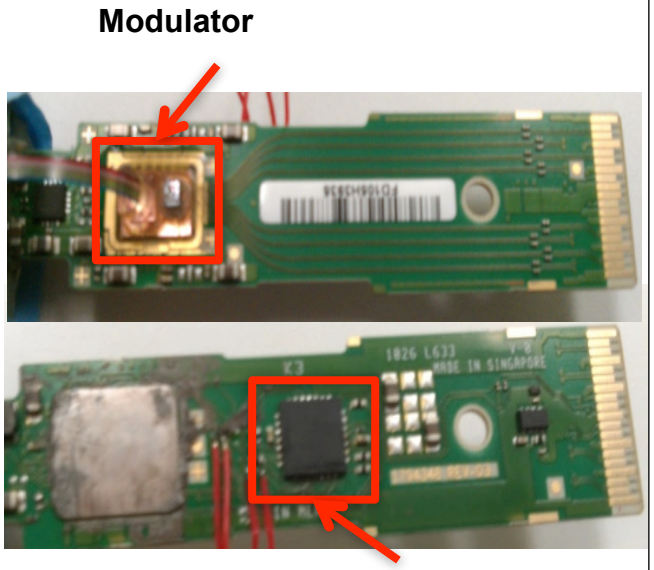


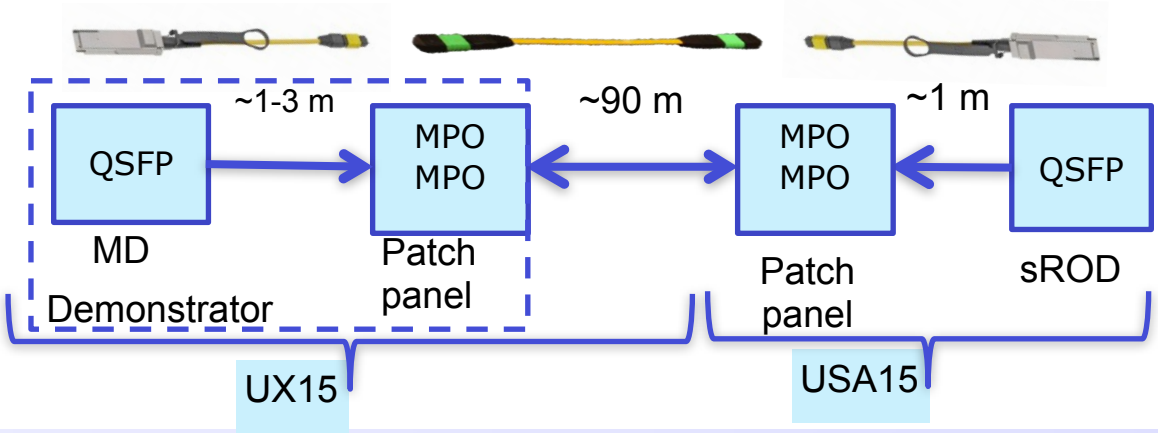
First prototype of HVOpto board ready for mini-drawer tests



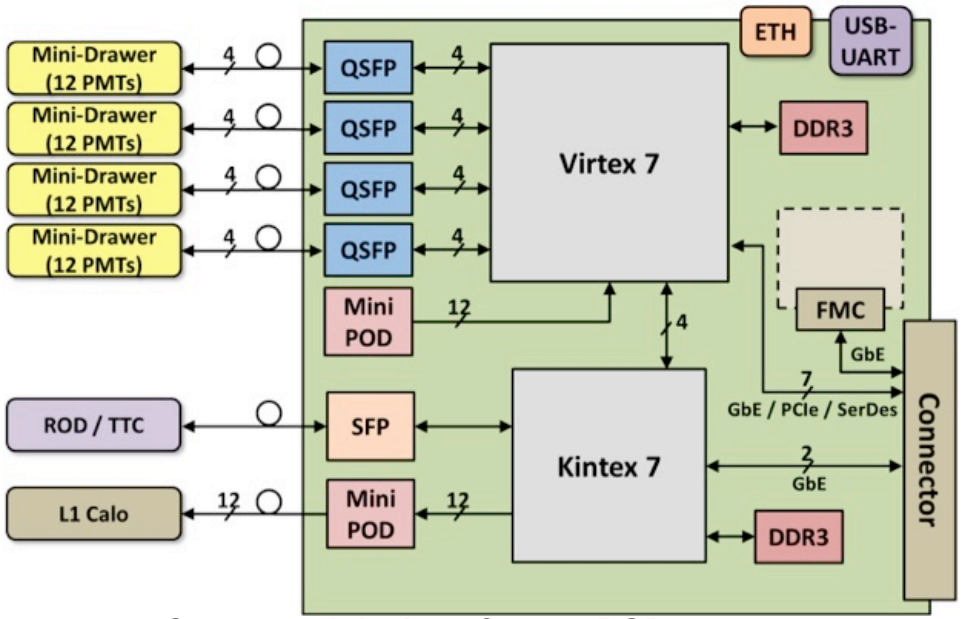
Read-out links

- 8 read-out links/super-drawer: 1+1 (redundancy) x 4 mini-drawers
- Luxtera Active Optical links:
  - 4 bi-directional channels: 1-14 Gbps/ch
  - excellent error rate: BER < 10^{-18} (~1err/3y)
- Made out of 130 nm Silicon On Insulator CMOS
- TID: tested up to 165 kRad passed but the PIC (used for configuration) fails at ~20 kRad. Replacement with an FPGA under investigation.
- SEU: tested under fluence of 1.2×10^{12} p/cm^2 operating at 10Gbps show ~0 Tx errors, few Rx errors. Still under investigation.

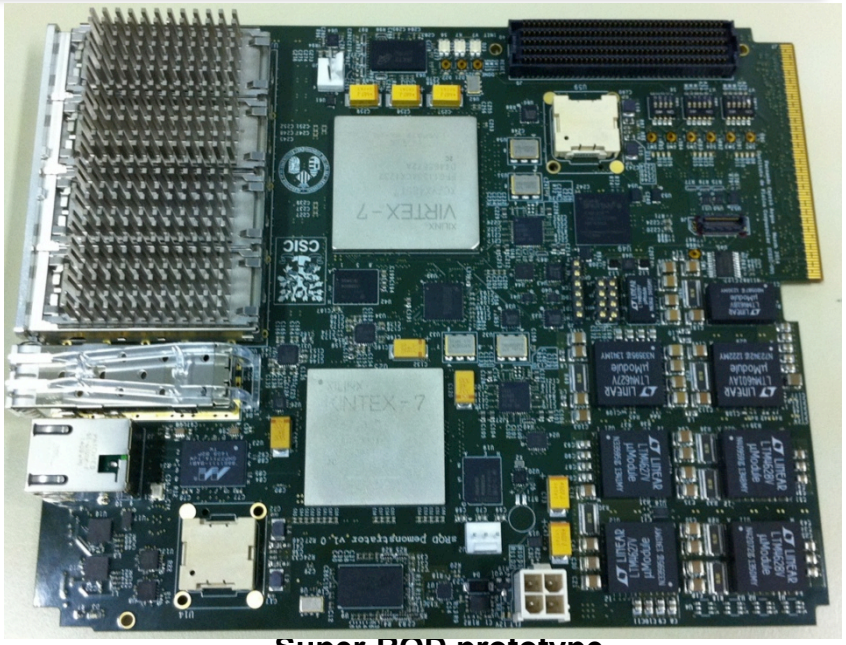




Super-ROD demonstrator prototype



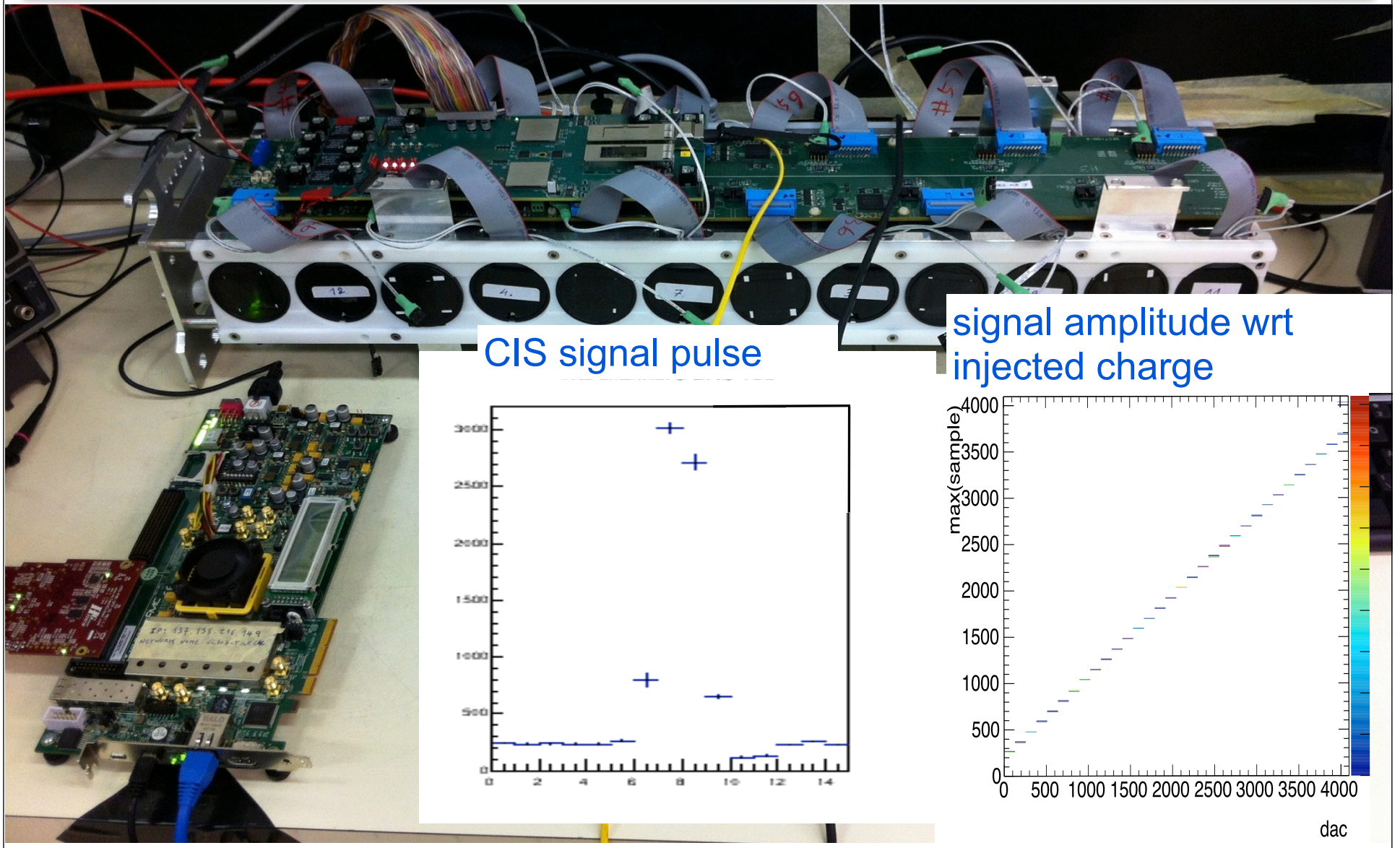
Conceptual design of super-ROD prototype



Super-ROD prototype

- Super-ROD interfaces the FE with current ROD and DCS
  - Prototype compliant with midsize AMC (180.6 mm x 148.5 mm)
  - Read-out of a complete super-drawer (4 mini-drawers) with QSFPs
  - Corresponding to 1/8 of input links of the design for phase-II
  - 1 Xilinx Virtex 7 FPGA 48 GTX@10Gb/s for data/DCS input and TTC/DCS output
  - 1 Xilinx Kintex 7 FPGA 28 GTX@10Gb/s to interface current ROD/TTC and L1Calo
  - 512 MB DDR3 SDRAM and 1 Gb flash per FPGA
- Status: first prototype received, testing ongoing.

Test-bench @ CERN



CIS signal pulse

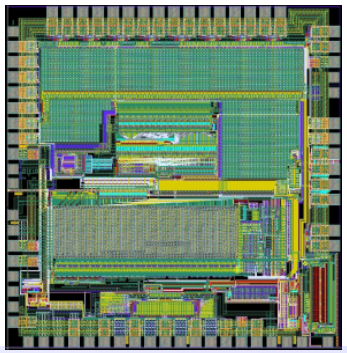
signal amplitude wrt injected charge

R&D of other FE options

QIE ASIC

- Charge Integrator and Encoder (QIE) chip from Fermilab
- Current splitter with multiple ranges and gated integrator + on-board flash ADC
  - Dead-timeless digitization (No pulse shaping) at 40 MHz operation
  - 17-bit dynamic range in 10 bits
- Status:
  - 40 chips in hand
  - Test of TID completed SEU ongoing.
  - Design review to improve resolution
  - integration in a FEB for 2015

QIE v10.5

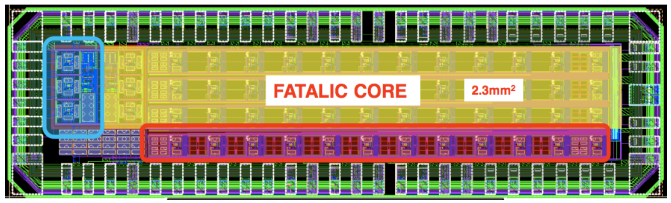


FATALIC

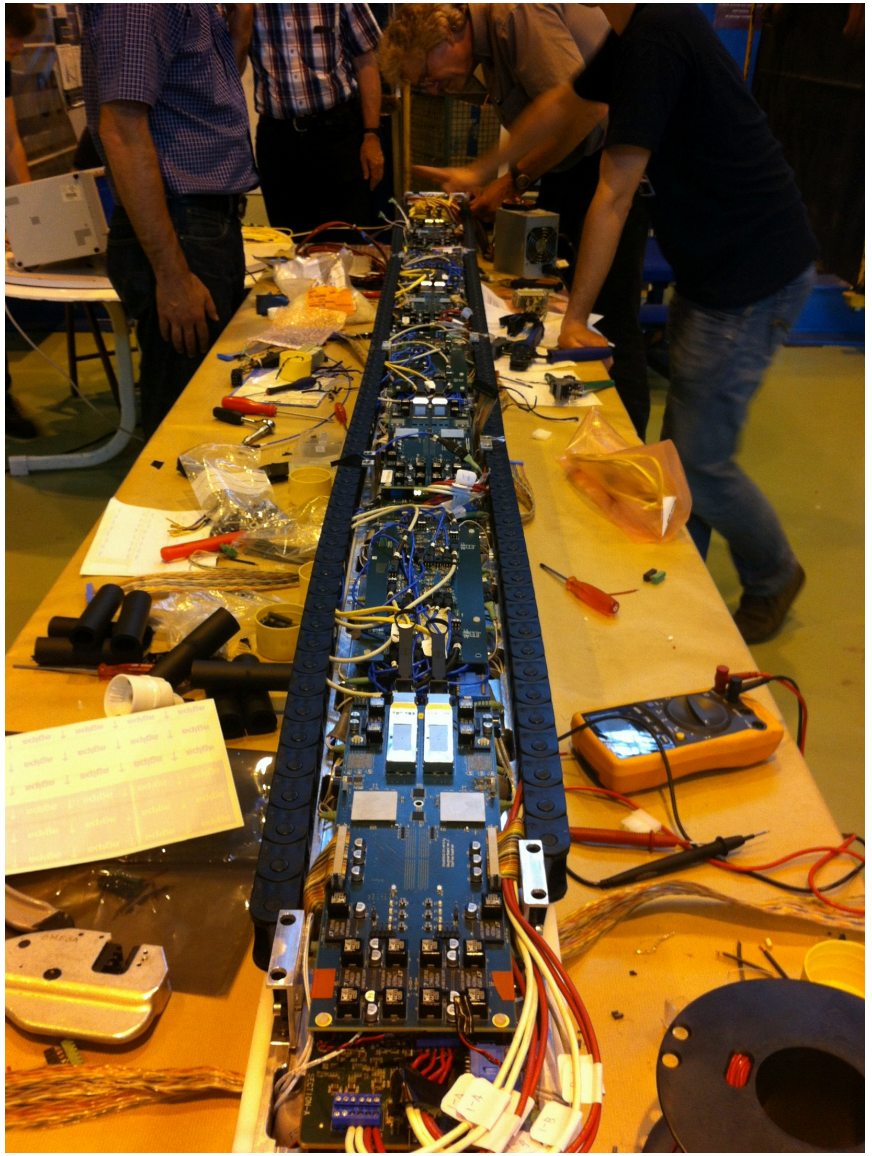
- FATALIC 4 ASIC:
  - Current conveyor
  - Shaping stage with 3 different gain ratios (1, 8, 64)
  - 3 x 12-bit ADCs
  - 40 MHz operation
- Status:
  - received in September, first test ongoing
  - integration into a FEB for 2015

All 3 options will be extensively tested for performances and radiation tolerance

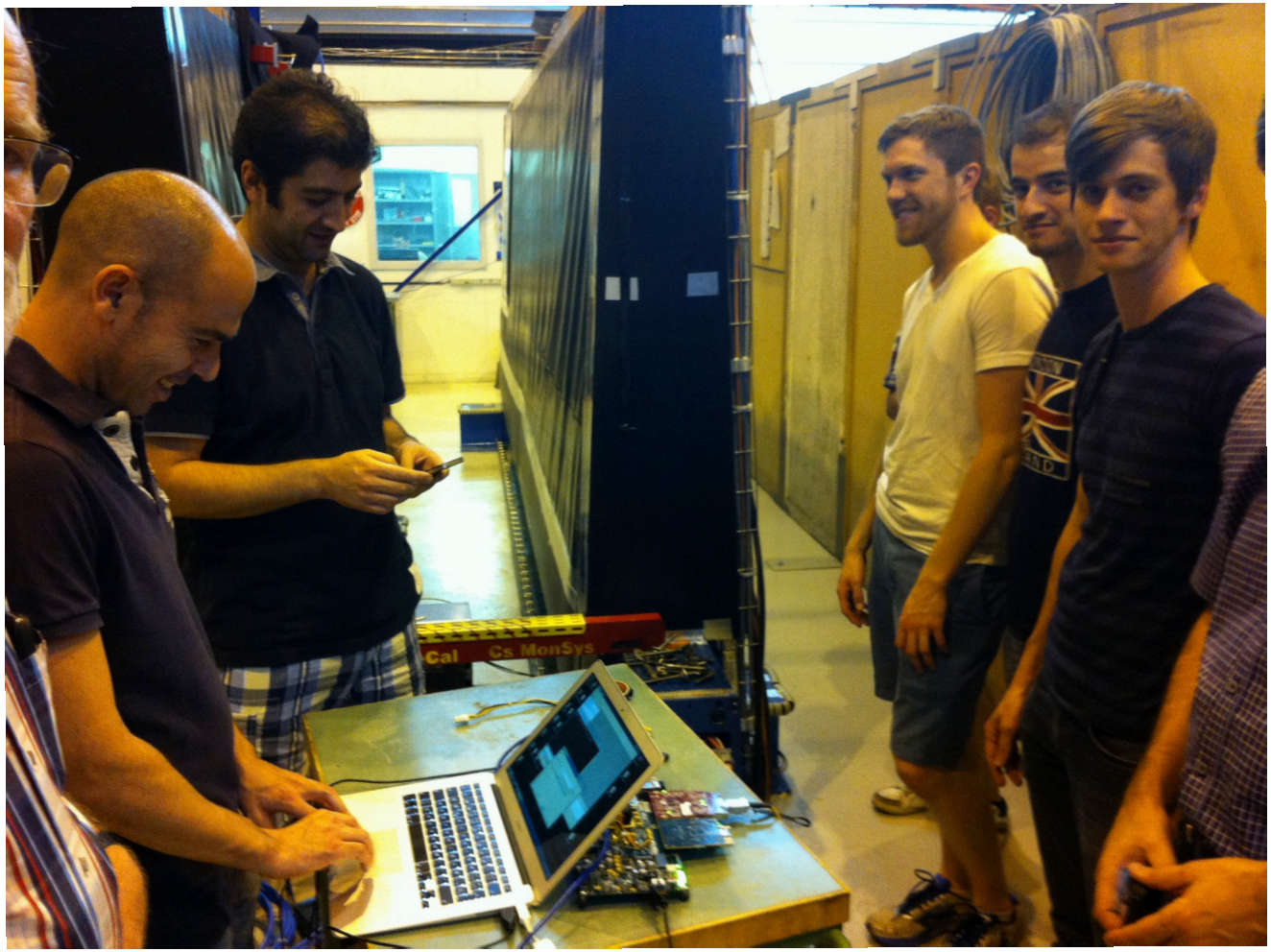
FATALIC-4



Demonstrator assembly in June 2014



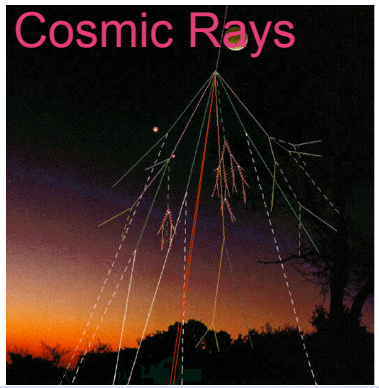
Insertion in the spare module and first tests



test/calibration using Cesium source

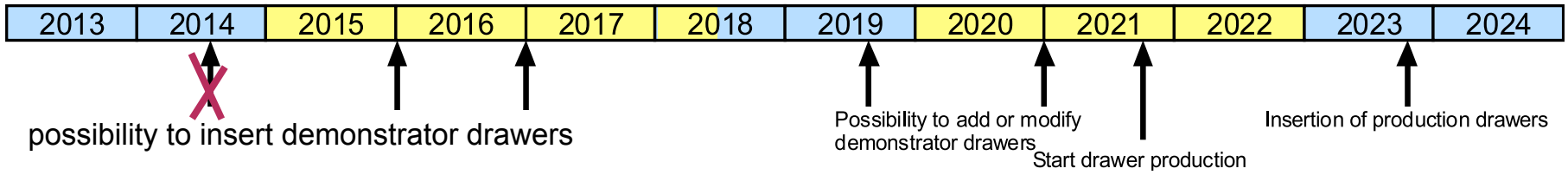
test/calibration using Laser

test/calibration using Cosmic Rays



Summary

- The project to upgrade the Tile calorimeter for HL-LHC is moving full steam ahead.
- The overal design is in good shape. Few alternative choices need to be fully evaluated under beam tests and with an early slice integration into ATLAS.
  - The first complete hybrid prototype (SD+sROD) originally target for insertion into ATLAS this year is under extensive testing in the LAB
  - additional mini-drawer prototypes with the different front-end options are expected to join the testing in 2015
- A beam test campaign is starting, targeting Summer 2015 and 2016.

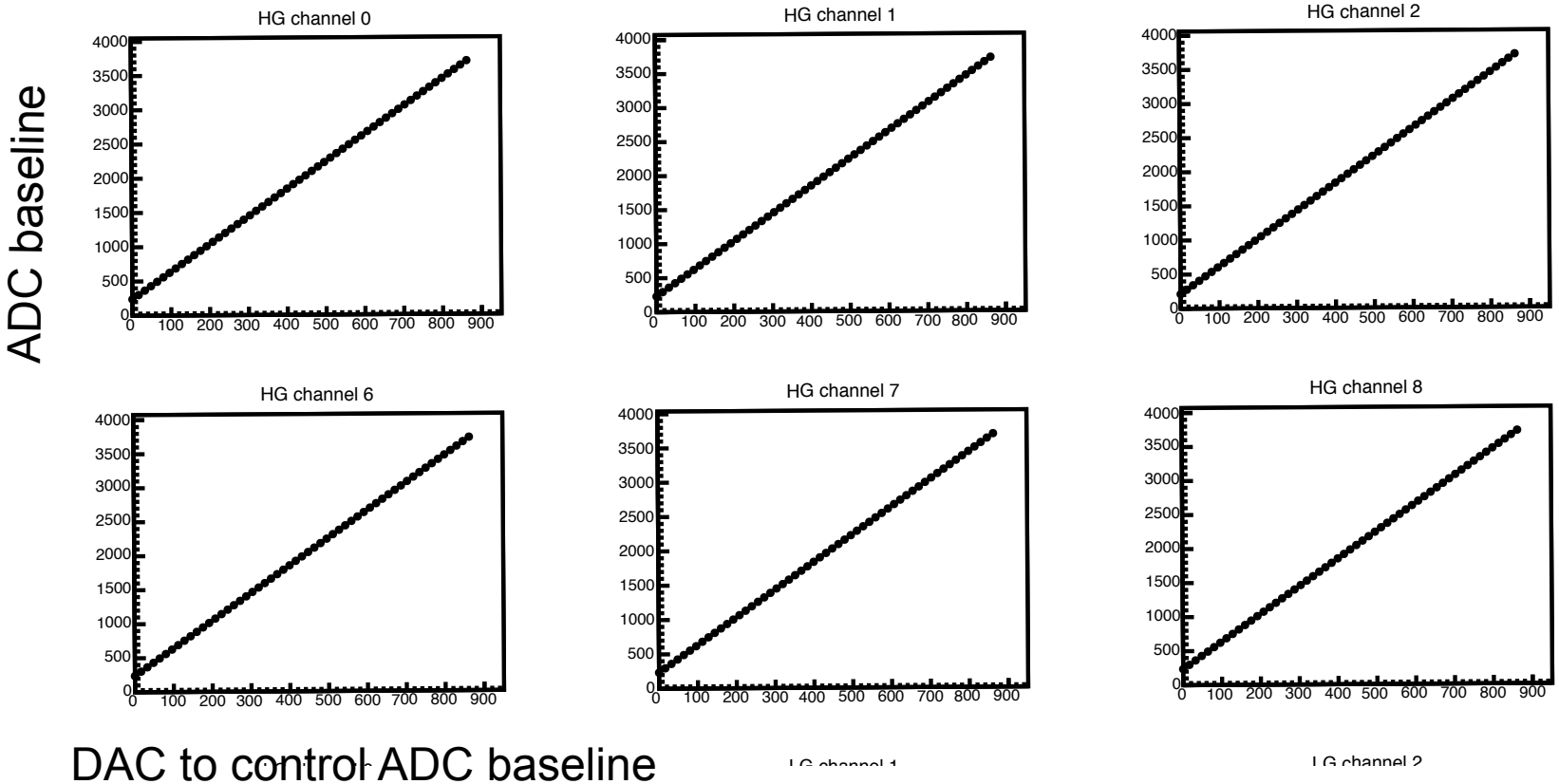


Backup

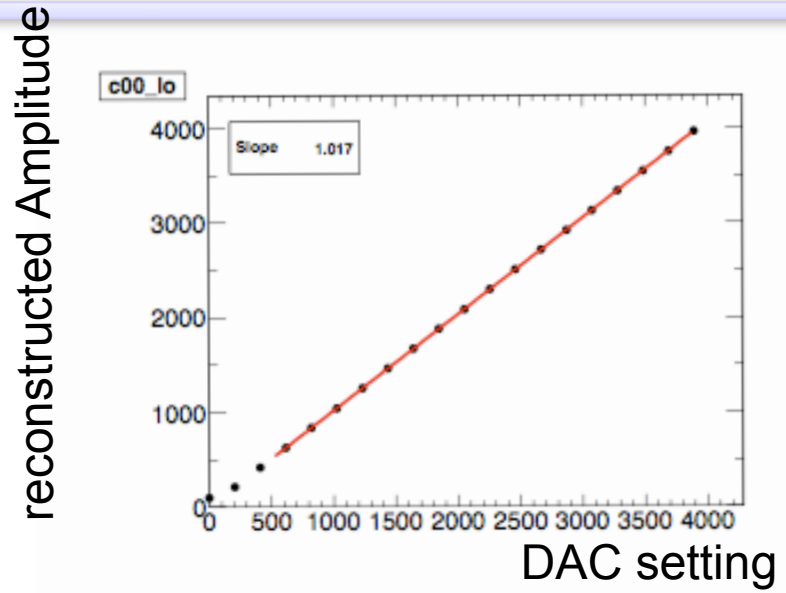
Basic operation tests
linearity of ADC baseline settings

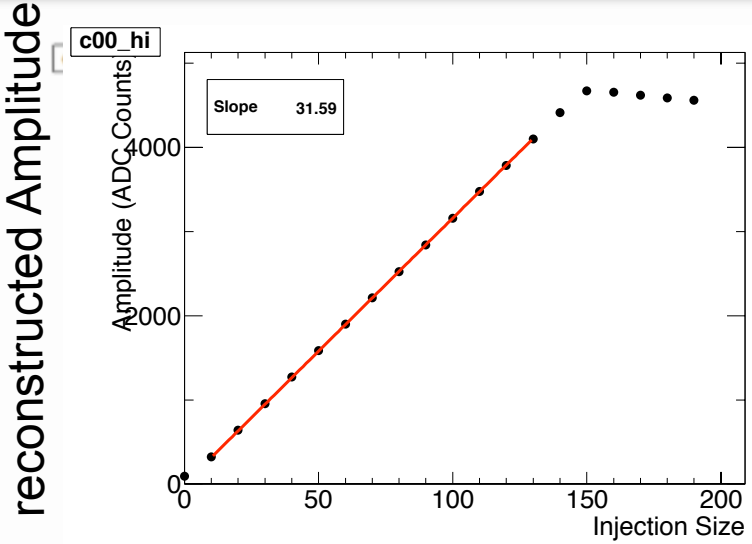
- simple operations of FADC read-out to test the alignement

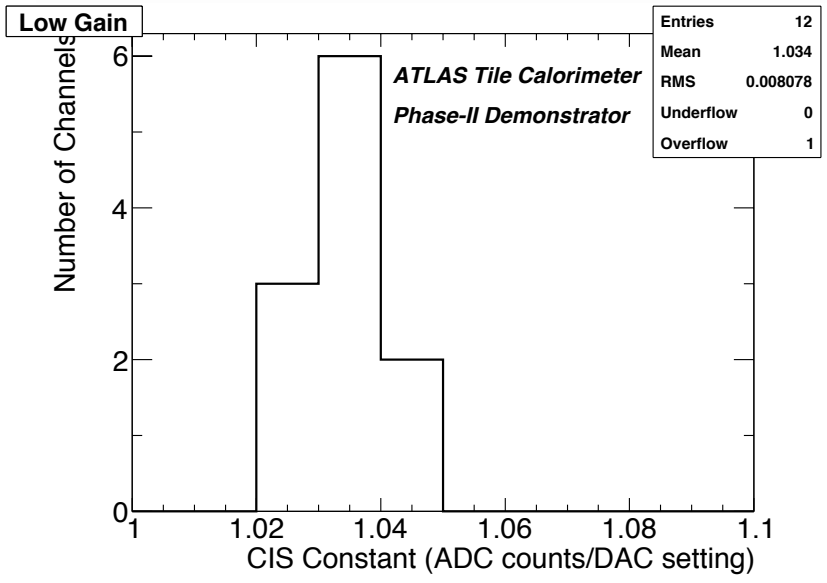
A. Valero

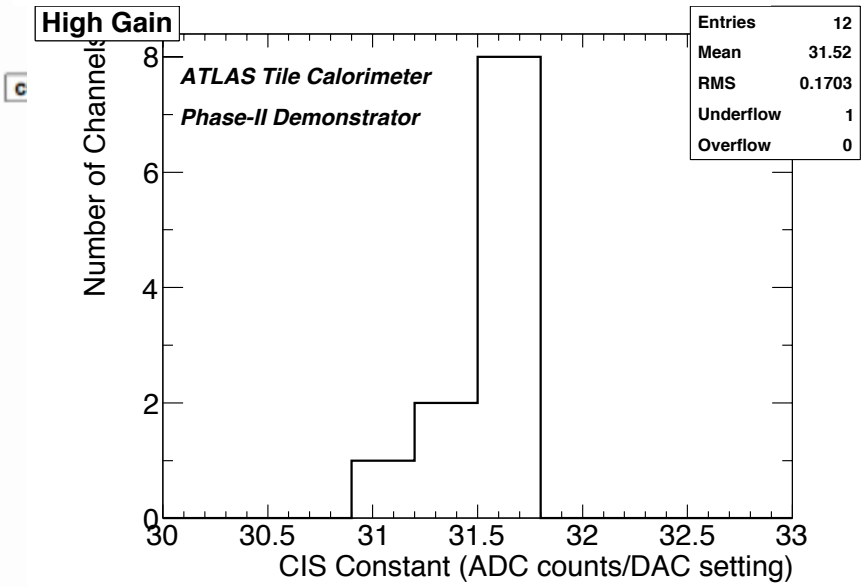


Basic operation tests
first look at calibration constant



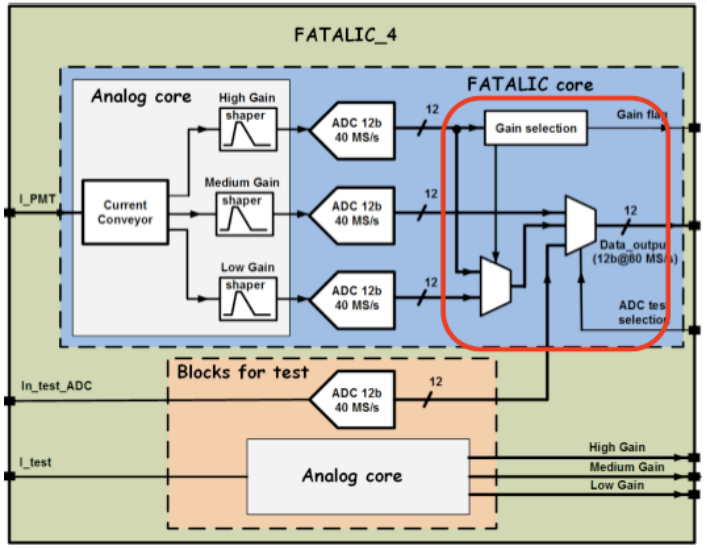




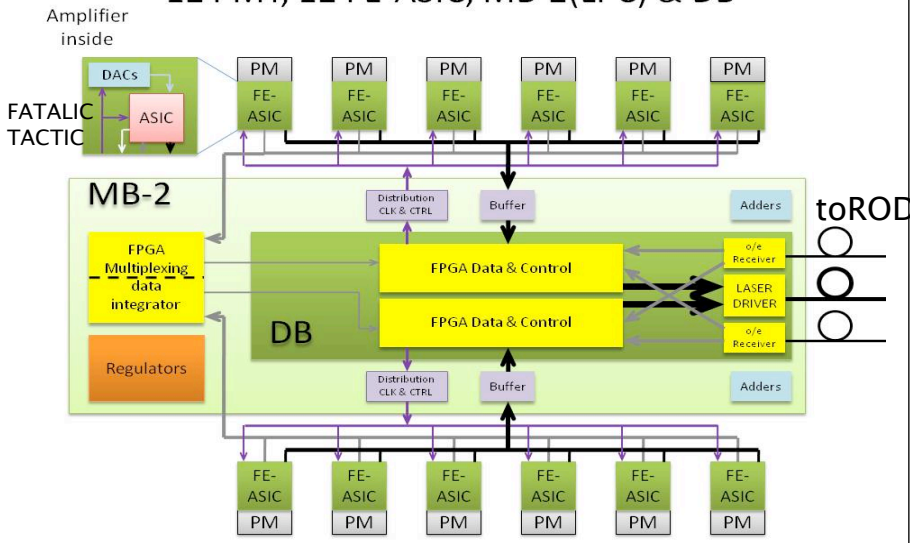


PMT read-out. Option 2 – FE-ASIC

- Based on the **FATALIC** chip family + TACTIC ADC
- IBM 130 nm technology. Shaping, 3 gain ranges (1, 8, 64)
- First prototypes (FATALIC 1/2) tested
  - Linearity and signal symmetry problems– under evaluation
- Version FATALIC 3 tested.
  - Circuit corrections + integrator amplifier
  - Reduced parasitic self effects
- New version FATALIC 4 foreseen very soon.



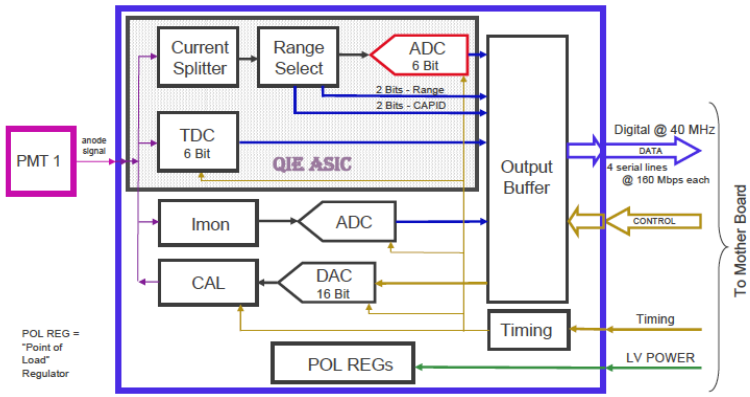
12 PMT, 12 FE-ASIC, MB-2(LPC) & DB

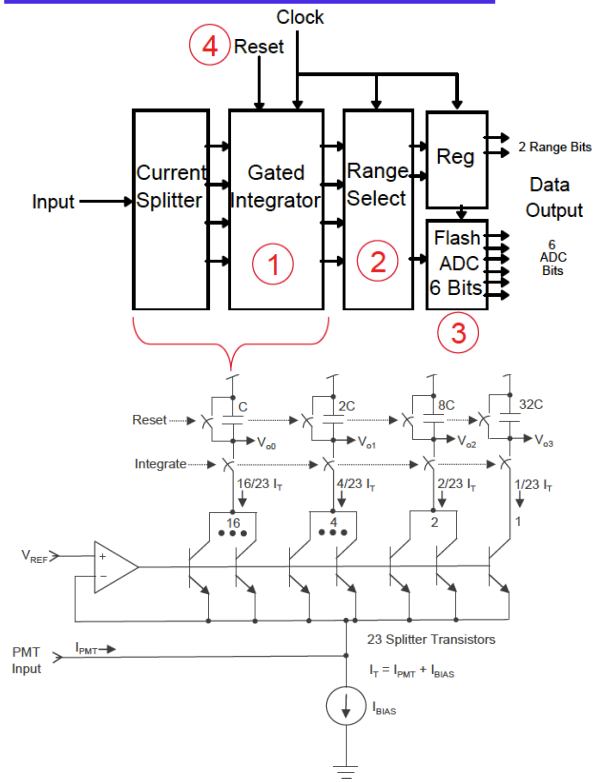


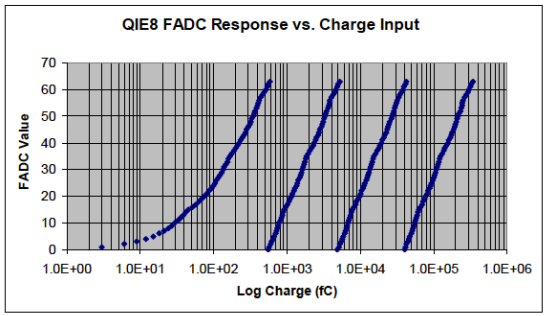
PMT read-out. Option 3 – QIE ASIC

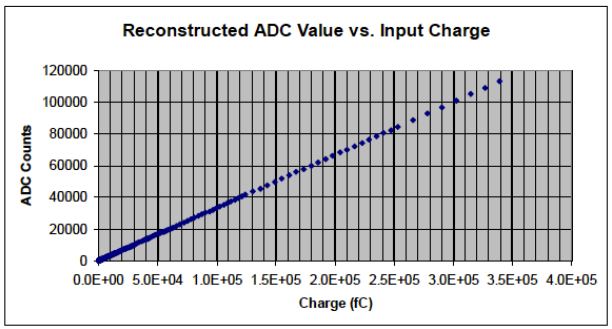
- Introduction:
  - Different concept – charge integrator
  - 4 clock cycles to acquire the data
- Data Output : 10 bits encodes a 17-bit dynamic range
  - 6-bit ADC value, 2 bits range (4 ranges), 2 bits CAPID
- Good progress on 1st chip;
  - Problems identified, understood and were fixed in QIE10.3b
- Version 10.4. Target submission date: Nov., 2012.
  - Will be fully-functional, including data drivers and TDC
  - Availability: needed by CMS for 2015 installation.
  - Should be significant numbers of chips for testing
  - Possibility to piggy-back on CMS production
- PLANS:
  - First tests with QIE at CERN lab in late summer, 2013
  - Beam tests at CERN in 2015; Maybe at FNAL in 2014

A Conceptual Design of the QIE Front End Board

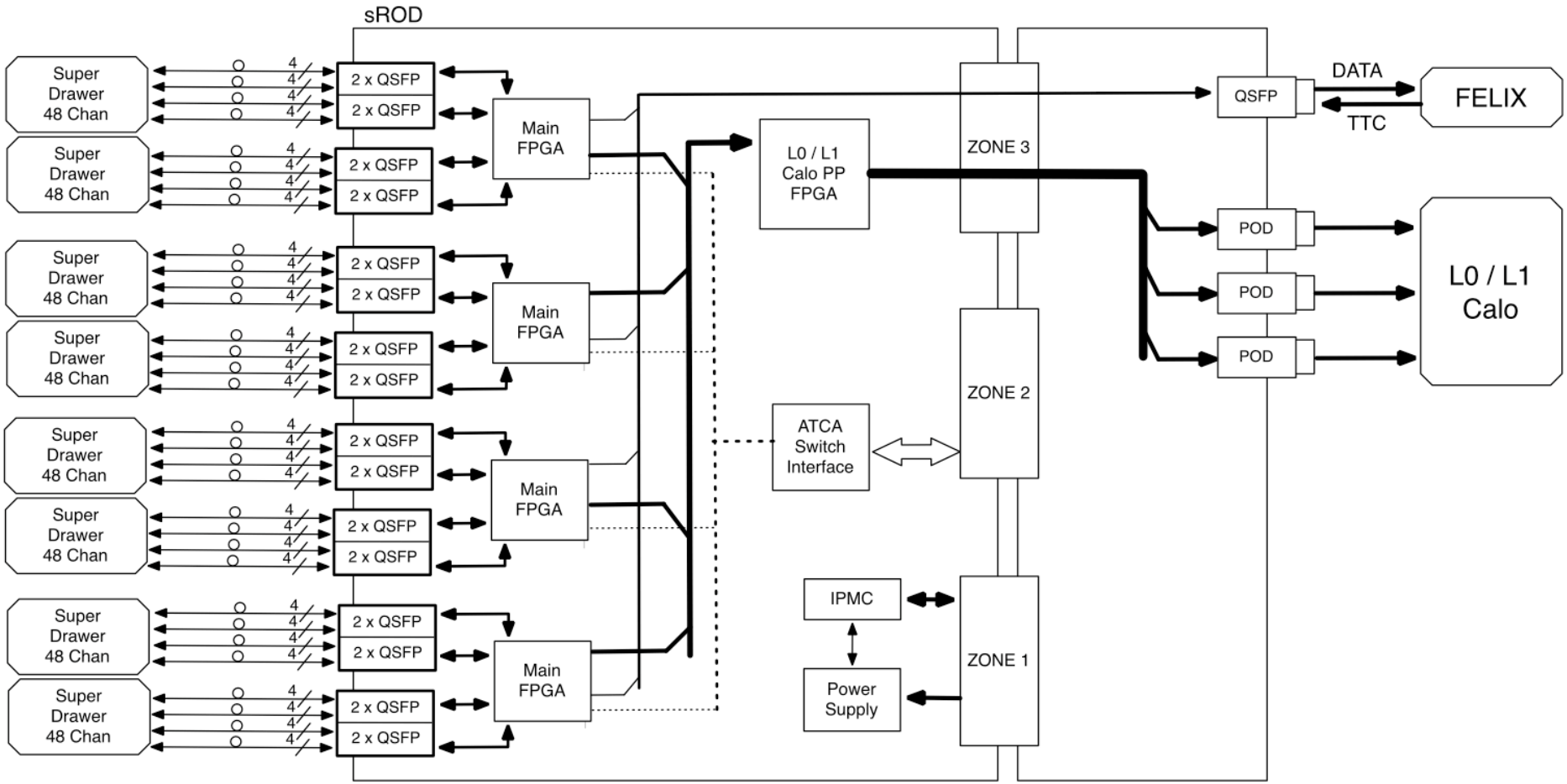








Possible layout for sROD



Readout dataflow in Phase-II