TWEPP 2014 - Topical Workshop on Electronics for Particle Physics

Wednesday, September 24, 2014

Second Poster Session (4:30 PM - 6:30 PM)

-Conveners: Mitchell Franck Newcomer

time	[id] title	presenter
4:45 PM	[151] Adaptive power supply for the gain stabilization of SiPM	POLAK, Ivo
4:46 PM	[150] Architectural Improvements and Technological Enhancements for the APEnet+ Interconnect System	BIAGIONI, Andrea
4:47 PM	[152] New Approach to Preamplifier-Shaper Design	ATKIN, Eduard
4:49 PM	[115] Optimisation of the Front-End Electronics of Drift Tube Chambers for High-Rate Operation	SCHWEGLER, Philipp
4:50 PM	[61] Zero Suppression Logic of the ALICE Muon Forward Tracker Pixel Chip Prototype PIXAM and Readout Electronics Development	Dr FLOUZAT, Christophe
4:53 PM	[135] MicroTCA and AdvancedTCA Equipment Evaluation and Customization for LHC Experiments	DI COSMO, Matteo
4:54 PM	[67] Readout Electronics Upgrade on ALICE/PHOS Detector for Run 2 of LHC	Dr WANG, Dong
4:55 PM	[83] The Readout Chain for the PANDA MVD Strip Detector	Mr SCHNELL, Robert
4:57 PM	[86] Low-Power Clock Distribution Circuits for the Macro Pixel ASIC	GAIONI, Luigi
4:58 PM	[171] High-Resolution Time To Digital Converters for the KM3NeT Neutrino Telescope	CALVO, David
4:59 PM	[85] Development of GEM Electronics Board (GEB) for Triple-GEM Detectors	TALVITIE, Joonas Petteri
5:00 PM	[20] Development of a FEI4 Wafer Level Stress Compensation Layer for Improvement of Thin Pixel Modules 3D Assembly	PARES, Gabriel
5:01 PM	[21] MicroTCA.4 for Industry and Research – Experiences with the Introduction of a New Crate Standard	FEIN, Katharina
5:02 PM	[22] Test Bench Development for the Radiation Hard GBTX ASIC	VICENTE LEITAO, Pedro
5:03 PM	[23] Secondary Particle Acquisition System for the CERN Beam Wire Scanners upgrade	SIRVENT BLASCO, Jose Luis
5:04 PM	[108] The Clock and Control System for the EuXFEL 2D Detectors: Firmware and System Integration	MOTUK, Erdem
5:05 PM	[119] SET Detection and Compensation and Its Application in PLL Design	Prof. CHEN, Jinghong
5:06 PM	[44] A Digital Readout System for the CMS Phase I Pixel Upgrade	STRINGER, Robert
5:07 PM	[29] Analogue Sum ASIC for L1 Trigger Decision in Cherenkov Telescopes Cameras	FREIXAS COROMINA, Lluís
5:08 PM	[41] Architecture of the Upgraded BCM1F Backend Electronics for Beam Conditions and Luminosity Measurement - Hardware and Firmware	ZAGOZDZINSKA, Agnieszka Anna
5:10 PM	[96] The CMS HCAL FEE Control Module	GOADHOUSE, Stephen
5:11 PM	[147] Thermal Analysis of the Proto-VIPRAM2D Chip	ZHANG, Tao

5:12 PM	[142] A 12GHz Low-Jitter LC-VCO PLL in 130nm CMOS	Prof. CHEN, Jinghong
5:14 PM	[77] FBCT Fast Intensity Measurement Using TRIC Cards	Mr ALLICA, Juan Carlos
5:15 PM	[121] JTAG-based Remote Configuration of an FPGA Over Optical Fibers	LIU, Tiankuan
5:16 PM	[122] The Clock Distribution System for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade Demonstrator	LIU, Tiankuan
5:18 PM	[72] Development of the Read-out ASIC for Muon Chambers of the CBM Experiment	MALANKIN, Evgeny
5:19 PM	[70] Clock and Data Recovery Implementation and Testing for the Readout Control Unit 2 in ALICE TPC.	TORGERSEN, Christian
5:20 PM	[92] The Upgrade Plans and Challenges of the ATLAS First-level Trigger Towards the HL-LHC	GRADIN, Per Olov Joakim
5:22 PM	[78] PEALL4: A 4-channel, 12-bit, 40-MSPS, Power Efficient and Low Latency SAR ADC	RARBI, Fatah
5:23 PM	[111] The GBT-FPGA Core: Features and Challenges	BARROS MARIN, Manoel
5:24 PM	[133] The ATLAS Level-1 Muon Topological Trigger Information for Run 2 of the LHC	SILVA OLIVEIRA, Marcos Vinicius
5:25 PM	[98] A Pattern Recognition Mezzanine Based on Associative Memory and FPGA Technology for L1 Track Triggering at HL-LHC	MAGALOTTI, Daniel
5:26 PM	[98] The VFAT3-Comm-Port : A Complete Communication Port for Front-end ASICs Intended for Use within the High Luminosity Radiation Environments of the LHC.	DABROWSKI, Mieczyslaw Maria
5:28 PM	[119] Depleted Monolithic Active Pixel Sensors with LF 150 nm CMOS	KISHISHITA, Tetsuichi
5:29 PM	[91] CMS ECAL Electronics Developments for HL-LHC	HANSEN, Magnus
5:30 PM	[96] Research and Design of the Electronics System for the Underground Dark Matter Detection Experiment in IHEP	Dr HU, Jun
5:31 PM	[95] Design and Testing of Combined GEM+CSC Trigger Algorithm Firmware for the CMS Muon Endcap System	TATARINOV, Aysen
5:32 PM	[169] 3D Simulation and Dopping Profile Measurements of Planar Pixel Sensors	GKOUGKOUSIS, Vagelis
5:33 PM	[82] Development of a Custom On-line Ultrasonic Vapour Analyzer and Flowmeter for the ATLAS Inner Detector, with Application to Cherenkov and Gaseous Charged Particle Detectors.	Mr KATUNIN, Sergey
5:34 PM	[136] ProtoVIPRAM2D: Realization and Testing	LIU, Tiehui Ted
5:35 PM	[81] Demonstrator System for the Phase-I Upgrade of the Trigger Readout Electronics of the ATLAS Liquid-Argon Calorimeters	FRAGNAUD, Jasmin
5:55 PM	[162] NaNet: a Configurable NIC Bridging the Gap Between HPC and Real-time HEP GPU Computing	LONARDO, Alessandro