



ATLAS Upgrades

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on behalf of the ATLAS Collaboration

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(Werner-Heisenberg-Institut)

Physics at LHC and beyond
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MAX-PLANCK-GESELLSCHAFT



Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

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The ATLAS detector in Run 1

Muon spectrometer

□ Tracking
Toroid Magnets

Precision Tracking:

- MDT (Monitored drift tubes)
- CSC (Cathode Strip Chambers)

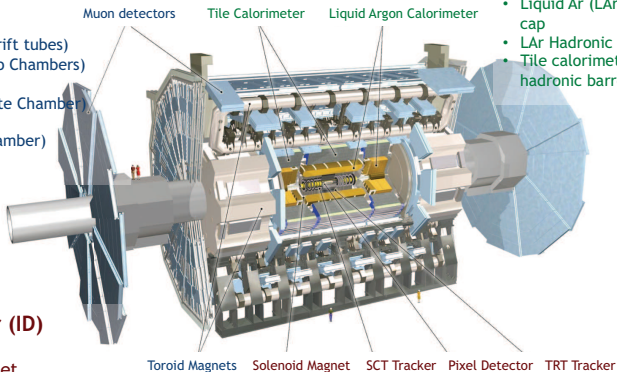
Trigger:

- RPC (Resistive Plate Chamber) Trigger
- TGC (Thin Gas Chamber)

Calorimeter system

EM and Hadronic energy

- Liquid Ar (LAr) EM barrel and end-cap
- LAr Hadronic end-cap
- Tile calorimeter (Fe-scintillator) hadronic barrel



Inner Detector (ID)

Tracking
2T Solenoid Magnet

- Silicon Pixels 50 x 400 μm^2
- Silicon Strips (SCT)
80 μm stereo
- Transition Radiation Tracker (TRT)
up to 36 points/track

Three Level Trigger system

- L1 - hardware: 70 kHz, 2.5 μs latency
- L2 - software: 6.5 kHz, 10 ms latency
- EF - software: 600 Hz, 1-2 s latency

Timeline of LHC and Atlas Upgrades

New LHC schedule beyond LS1

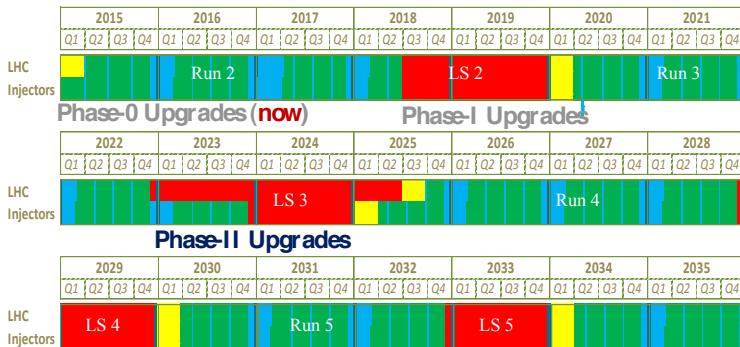
Approved by CERN
on 02.12.2013

Only EYETS (19 weeks) (no Linac4 connection during Run2)

LS2 starting in 2018 (July) 18 months + 3months BC (Beam Commissioning)

LS3 LHC: starting in 2023 => 30 months + 3 BC

injectors: in 2024 => 13 months + 3 BC



N.B.: Phase- n Upgrade \Leftrightarrow Long shutdown LS($n+1$) \Rightarrow followed by Run($n+2$)



Phase-0 Upgrade

LHC prepares for design energy and nominal luminosity:

- Consolidation of superconducting splices
- $\sqrt{s} = 13 - 14 \text{ TeV}$ with 25ns bunch spacing
- $\mathcal{L} \approx 1 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$

• New beam pipes

- Al beam pipes \rightarrow less muon background
- close to IP: smaller diameter Be beam pipe \rightarrow less activation

• Insertable B-Layer (IBL)

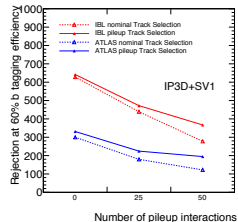
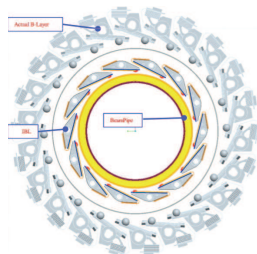
- 4th pixel layer, mounted on new beam pipe
- Highly improved b -tagging performance
- Test of new 130nm CMOS technology (25% 3D and 75% n -in- n planar) to be used for Phase-II ITk

• Pixel: new Services Quarter Panels (nSQP)

• Diamond Beam Monitors (DBM)

• Muon spectrometer consolidation

- Installation of Endcap Extension (EE) Muon Chambers to address low efficiency in barrel-endcap transition region
- Repair/replacement of several chambers



Phase-I Upgrade

- Inner Detector
 - Fast Tracker (FTK) for Level-2 Trigger
- Calorimeter
 - Higher Granularity Level-1 Trigger
- Muon Spectrometer
 - **New Small Wheel (NSW)**
 - Consolidation of Muon Chambers coverage

N.B.: This is not a complete list



Fast TrackKer (FTK) for Level-2 trigger

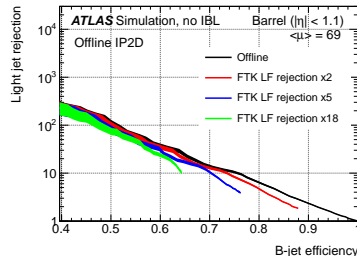
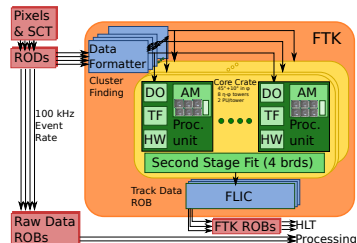
Motivation: maintain efficiency and low thresholds in high pileup environment

- need tracking information for L2
- ! software-based tracker limited by processing time/computing capacity

Dedicated, hardware-based track finder

- Runs after L1, on duplicated read-out links
- Provides full-event tracking input for L2
- Two sequential steps of increasing resolution:
 - Hit pattern matching to pre-stored 'roads' using Associative Memory ASICs
 - Linear fitting of full resolution hits in FPGAs
- Global track reconstruction with near offline resolution
 - Event rate < 100 kHz
 - Latency $< 100\mu\text{s} \Rightarrow$ L2 full track reconstruction $\mathcal{O}(100\text{ms})$

Vertical Slice to be installed in ATLAS during Run2



Level-1 Calorimeter Trigger Readout Strategy

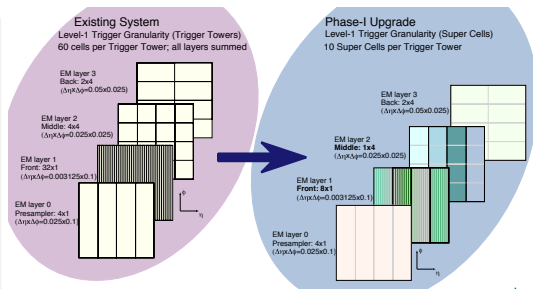
Goal: Retain low transverse energy (E_T) threshold despite higher rates

Limitations

- L1 trigger rate limited by bandwidth of front-end electronics to 100 kHz
- L1 latency limited by depth of front-end pipeline memory to 2.5 μs

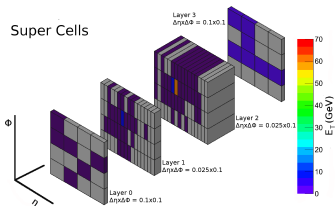
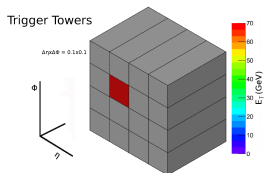
Strategy

- Retain transverse energy in each layer instead of summing
→ longitudinal shower information
- Use finer granularity in front and middle layers (Super Cells)
- More effective energy calculation algorithms



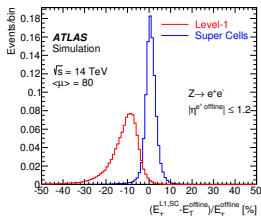
Level-1 Calorimeter Trigger: Expected Performance

A 70GeV-electron as seen by current (left) and upgraded (right) L1 Calorimeter trigger:

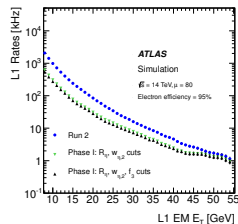


- Forward compatible with Phase-II Upgrade
- Improvement in electron reconstruction, isolation, energy resolution

improved energy resolution



lower trigger rate

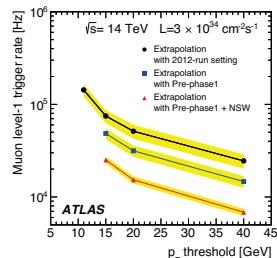
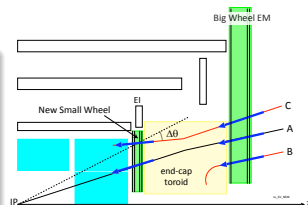


New Small Wheel

Muon small wheel (part of EI) is located between end-cap calorimeter and end-cap toroid and exposed to highest cavern background flux

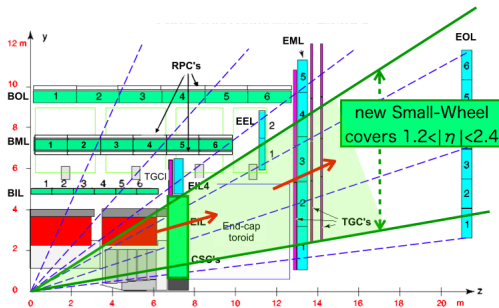
Goals of small wheel upgrade

- Precision tracking in high luminosity conditions (position resolution $< 100\mu\text{m}$, angular resolution $< 1\text{mrad}$)
- Real-time segment reconstruction for L1 trigger \rightarrow background triggers can be reduced by requiring a track segment in EM to be matched by corresponding segment in EI



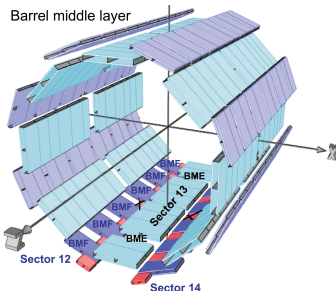
Detector types

- MicroMegas (tracking)
- sTGC (trigger)



Consolidation of Muon Spectrometer coverage

Tracking chambers:



Trigger chambers:

- No trigger chambers in Barrel Inner Small (BIS) sectors (large sectors partly covered by TGC doublets in EIL4+5)

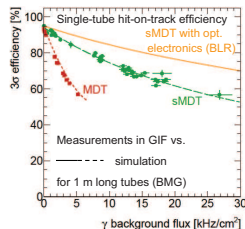
⇒ Add RPC chambers in BIS 7+8

- 3-layer setup to allow stand-alone capability
- Additionally replace BIS 7+8 MDTs with sMDTs

12 new BMG sMDT chambers in Sectors 12+14
inside detector feet between BMF chambers

sMDT chambers

- drift tube diameter 15mm instead of 30mm
- lower occupancy
- shorter deadtime
- less gain loss due to space charge field
- up to twice the number of layers



Phase-II Upgrade

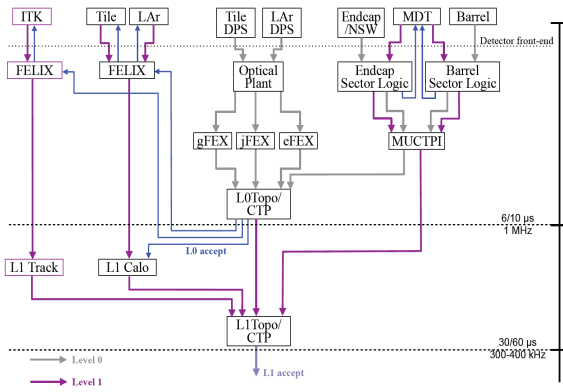
- New Trigger and DAQ architecture
- **New Inner Detector (ITk)**
- Calorimeter
 - New LAr and Tile Calorimeter electronics
 - Possible Forward Calorimeter upgrade
- Muon Spectrometer
 - New read-out electronics
 - MDT-based trigger

again: not a complete list



Two-Level Trigger Scheme for Phase-II

- Two-level system: current L1 becomes L0 and new L1 includes precise muon and inner tracking
- Take advantage of Phase-I improvements (NSW and L1-Calo)
- Requires changes to detector FE electronics feeding the trigger system
- Need higher trigger rates to keep thresholds at acceptable levels



Level-0

Muon + Calo
1 MHz, 6/10 μ s latency
define Rols for L1

Level-1

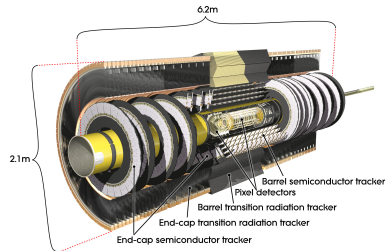
Muon + Calo + ITk
300-400 kHz, 30/60 μ s latency
trigger decision off-detector



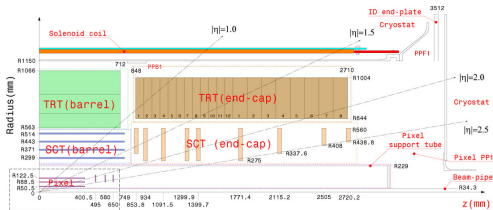
ID: New All-Silicon Inner Tracker (ITk)

Limiting factors for HL-LHC

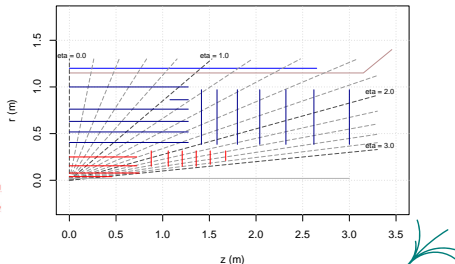
- Radiation damage (Pixel, SCT)
- Occupancy
 - Bandwidth saturation (Pixel, SCT)
 - Performance deterioration (TRT)



⇒ Complete replacement with all-silicon tracker



Current Inner Detector

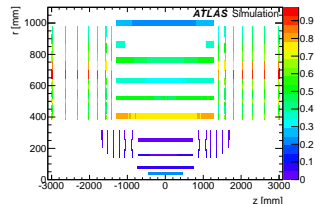
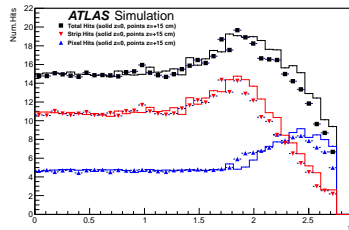
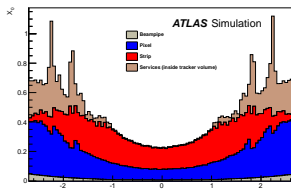
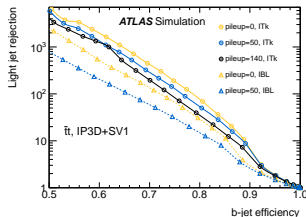


ITk layout from Lol



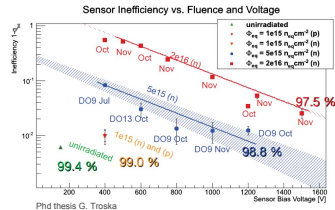
ITk: Performance Studies

- Robust tracking (14 hits/track for $|\eta| \lesssim 2.3$)
- Occupancy < 1% for maximum μ of 200
- Reduced material compared to current ID (less than $0.7X_0$ for $|\eta| \leq 2.7$)
- Maintain and improve detector performance (p_T -resolution, tracking efficiency, two-particle separation, vertexing, b -tagging) in high-pileup environment

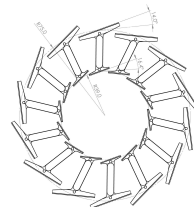
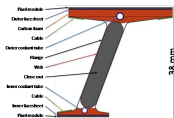
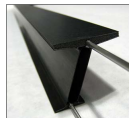
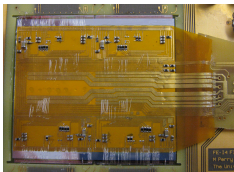
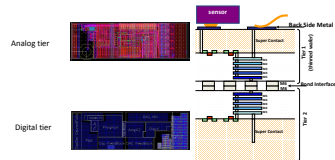


ITk: Pixel Detector

- Various technologies tested for radiation hardness: *n*-in-*n*, *n*-in-*p* planar, 3D (some already implemented in IBL), CMOS, diamond
- Vertical integration for compact modules: Through Silicon Vias (TSV)
- Front-end electronics: 3D test chip FE-TC4-P1 with two tiers in 130nm CMOS technology with TSVs and surface bonding pads
- Prototype in 65nm technology
- Two buffers for two-level trigger
- I-beam staves for inner two layers



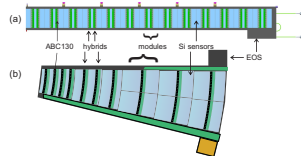
FE-TC4-P1 demonstrator



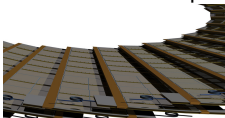
ID: Strip Detector

Basic element for mechanical support and electrical and cooling services:

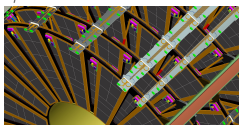
- Barrel (5 concentric cylinders): 236 **staves (a)** on each side with 13 modules on each face
- End-cap (7 disks on each side): 32 **petals (b)** per disk with 9 modules on each face



Overlap in ϕ -direction

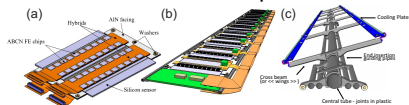


Turbopan



Castellated layout

stave alternative: supermodule



Sensors and electronics

- AC-coupled n -in- p FZ silicon sensors
- Two hybrids mounted on each sensor
- 10 ABC130s (130nm CMOS ASICs) per hybrid
- 256 readout channels for each ABC130
- Two buffers \rightarrow compatible with two-level trigger scheme



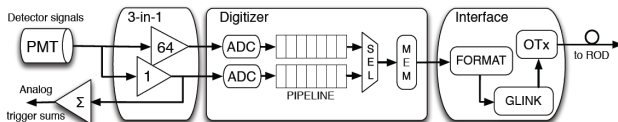
Calorimeter Electronics

Complete replacement of front-end and back-end electronics
for both LAr and Tile Calorimeters

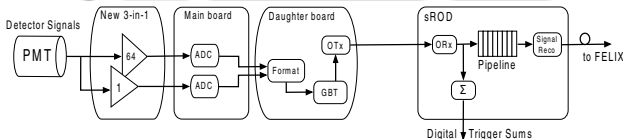
Signals from **all readout channels** are digitized at 40MHz and transferred off-detector

- Full calorimeter granularity available for L1 trigger at every bunch crossing
- Front-end electronics impose no constraints on latencies or rates
- Flexibility for potential evolution of trigger architecture

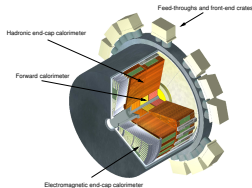
Present Tile:



Phase-II Tile:



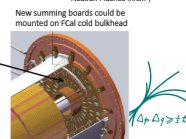
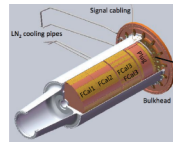
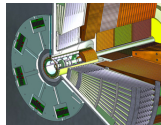
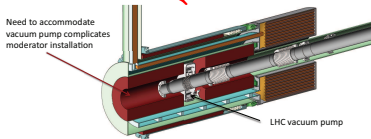
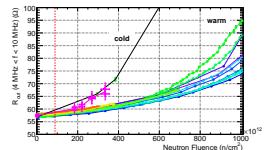
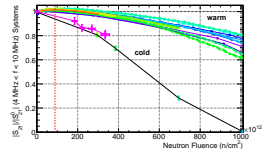
LAr Calorimeter: HEC cold electronics and FCAL



- HEC cold electronics inside cryostat
- Not designed to withstand HL-LHC radiation levels
- Expected doses seem manageable; aging might be issue

Options

- 0: No replacement of HEC cold electronics nor FCAL
- 1: HEC cold electronics need to be replaced
 - Opening of large cold cover
 - FCAL must be removed; replace by sFCAL
- 2: No replacement of HEC electronics; installation of **sFCAL**
 - FCAL replacement only; no opening of cold cover
- 3: No replacement of HEC electronics; installation of **MiniFCAL** in front of existing FCAL to absorb energy



$\Delta p, \Delta g, \Delta t$

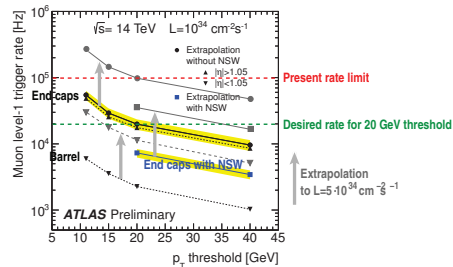
Muon System: Electronics Upgrade

Tracking chambers (MDTs)

- Performance of MDTs (including NSW) sufficient for HL-LHC
- L0/L1-trigger scheme and increased rates necessitate new read-out electronics

Trigger chambers (RPCs in barrel, TGCs in endcaps):

- L0/L1-trigger scheme requires new read-out electronics
 - TGCs: Keep existing on-chamber Amplifier-Shaper-Discriminator (ASD) chips
- Upgrade electronics to include pulse information for estimate of charge deposition
 - RPCs: Time-over-threshold mode → centroid of charge distribution for improved track resolution



Move trigger circuits from on-detector to radiation free zone (USA15) using high-bandwidth optical links

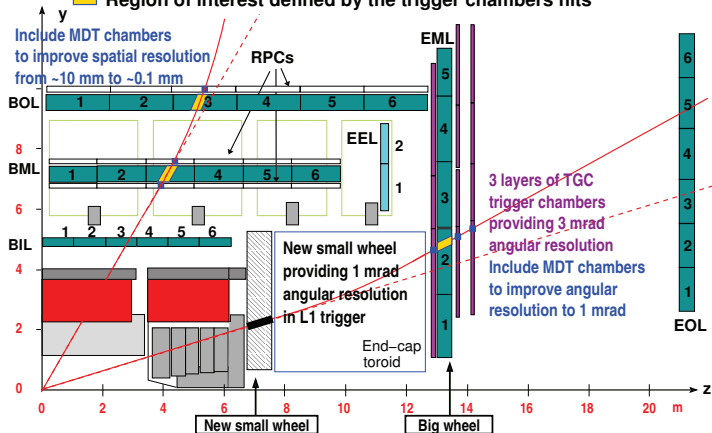
- use of FPGAs instead of dedicated ASICs for trigger algorithms
- higher level of flexibility



MDT-based Trigger Concept

- Precise MDT tracking information currently only used at L2
- Incorporation of MDT in L0/L1-trigger decision requires new MDT electronics with a fast chain of reduced time/spatial resolution
- Plan: replace MDT read-out electronics in BO, BM, and big wheel

- Hit cluster in trigger chambers
- Region of interest defined by the trigger chambers hits



Summary

- Coherent overall upgrade program for ATLAS from Phase-0 through Phase-II
 - Timelines and performance parameters consistent with LHC planning
- Staged upgrade program to take advantage of latest R&D results
 - Phase-0: Successfully on-going
 - Phase-I: Projects well-defined with TDRs approved
 - Phase-II: Lol completed in January 2013, TDRs in preparation (2016)
- Sufficient flexibility and headroom to accommodate:
 - Changes in schedule
 - Evolution of LHC operational parameters
 - Evolution of trigger architecture
 - Directions from New Physics signals

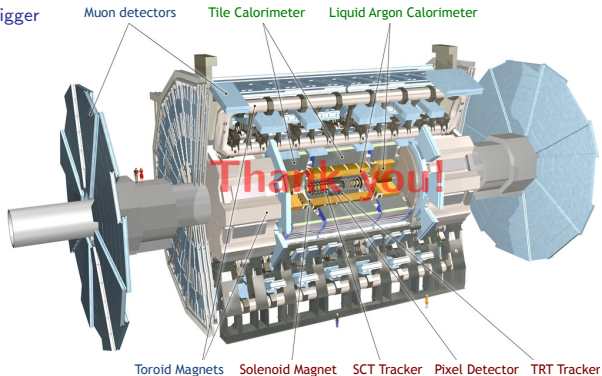


Muon spectrometer

- New Small Wheel
- Additional BMG chambers sectors 12&14
- BIS 7-8 RPCs in transition region
- Replacement of read-out electronics
- MDT-based trigger

Calorimeter system

- New L1 trigger (Super Cells)
- LAr and Tile electronics replacement
- Replacement of HEC cold electronics, FCAL?



Inner Detector (ID)

- Fast Tracker for L2 trigger
- New All-Silicon Inner Tracker

Two Level Trigger system

- L0: 1MHz, 6/10 μ s latency
- L1: 300-400kHz, 30/60 μ s latency

Extra slides



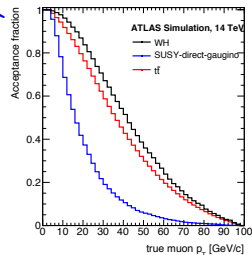
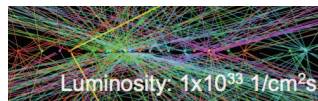
Detector challenges from HL-LHC

- Higher instantaneous luminosity means that more protons will collide in one event
 - Up to 200 pileup events per bunch crossing
 - Increased detector occupancy
 - Transmission bandwidth saturation
 - Larger event size

Trigger rates cannot increase in sync with luminosity
 \Rightarrow essential to refine hardware and software trigger to maintain sensitivity to physics

- Keep threshold for single isolated leptons as low as possible to avoid loss in acceptance
- Maintain high pileup rejection

- Higher integrated luminosity means higher total particle flux through the detector
 - Increased radiation damage especially close to the beam pipe
 - Increased activation of the detector materials

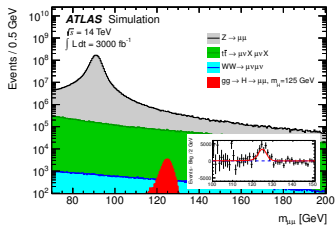
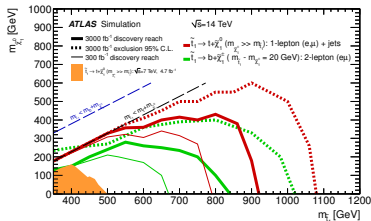


Physics motivation for LHC Upgrades

The European Strategy for Particle Physics - Update 2013:

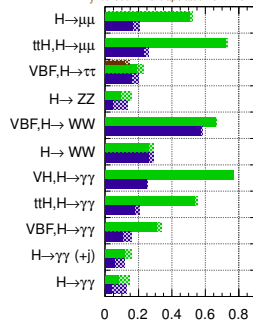
c) The discovery of the Higgs boson is the start of a major programme of work to measure this particle's properties with the highest possible precision for testing the validity of the Standard Model and to search for further new physics at the energy frontier. The LHC is in a unique position to pursue this programme. *Europe's top priority should be the exploitation of the full potential of the LHC, including the high-luminosity upgrade of the machine and detectors with a view to collecting ten times more data than in the initial design, by around 2030. This upgrade programme will also provide further exciting opportunities for the study of flavour physics and the quark-gluon plasma.*

- Higgs boson precision measurements
 - Mass, width, quantum numbers
 - Couplings to fermions and bosons
 - SM Higgs rare decays
- Investigation of electroweak symmetry
 - Enhancement of weak boson scattering amplitudes
 - Direct search for SUSY or other New Physics
 - Indirect effects of NP



ATLAS Simulation

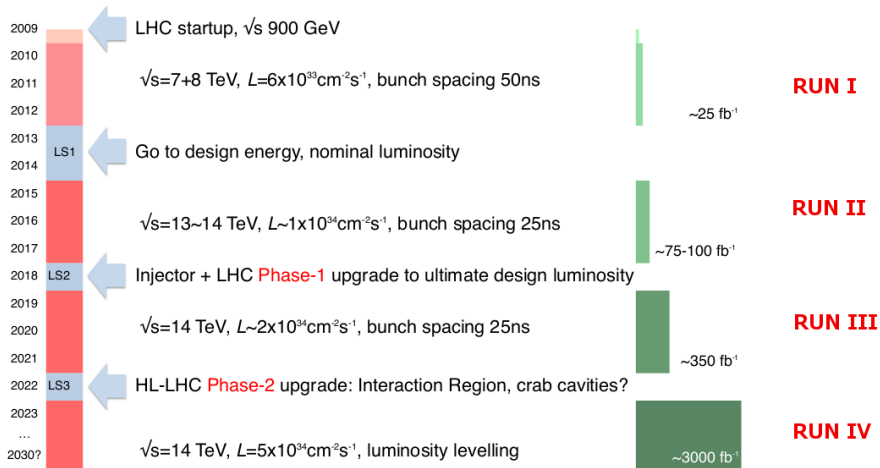
$\sqrt{s} = 14$ TeV: $\int L dt = 300 \text{ fb}^{-1}$; $\int L dt = 3000 \text{ fb}^{-1}$
 $\int L dt = 300 \text{ fb}^{-1}$ extrapolated from 7+8 TeV



$\frac{\Delta\mu}{\mu}$



Timeline of LHC and Atlas Upgrades (outdated)

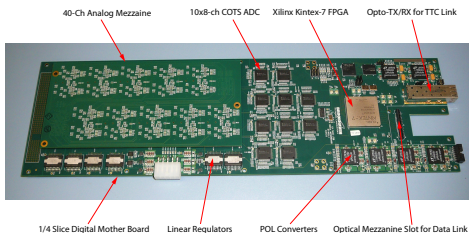


N.B.: Phase- n Upgrade \Leftrightarrow Long shutdown LS($n+1$) \Rightarrow followed by Run($n+2$)



R&D Activities for Calorimeter Phase-I Electronics Upgrade

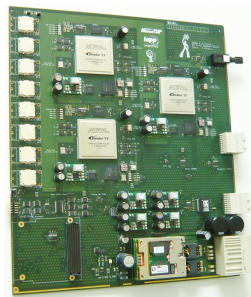
Mixed signal front-end ASICs



- High-speed serializer with 5.12 Gbps optical link
- 320 super cells per board
- 124 boards
- Total power < 156 W per board
- 12-bit ADC at 40 MHz

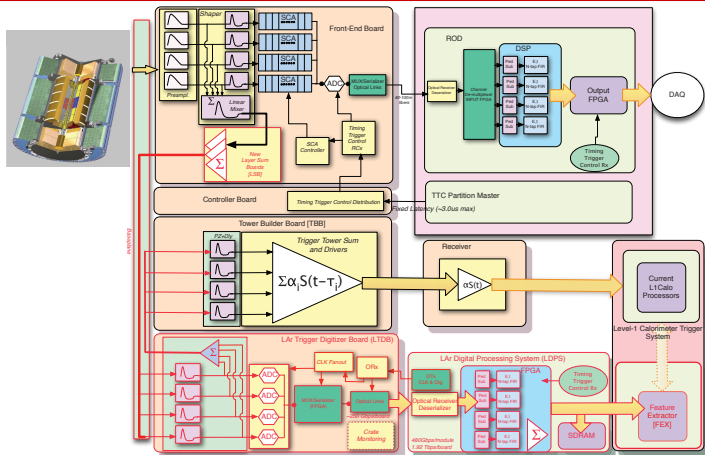
High-speed/high-density DSP units

- 4 Advanced Mezzanine Cards (AMC) per board
- 1 AMC handles 48 fibers each for reception and transmission
- 14 bunch crossings latency
- Filter algorithms use history of digital samples to suppress pileup



LAr Calorimeter: Level-1 Trigger Readout Architecture

new components in red



LAr Trigger Digitization Boards (LTDB, on-detector)

- Build analog sums as input for tower builder boards (TBB)
- Digitize Super Cell analog signals for LDPS
- Radiation-hard for HL-LHC, low power consumption

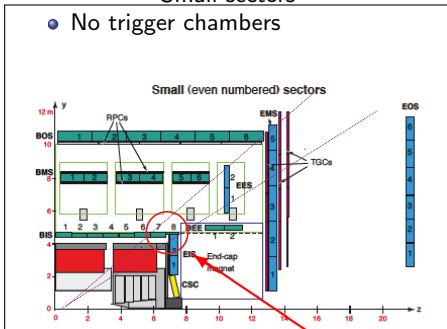
LAr Digitization Processing System (LDPS, off-detector)

- Receive digital signals via fast optical links
- Apply digital, FPGA-based filtering technique

Additional Muon RPCs in transition region BIS 7+8

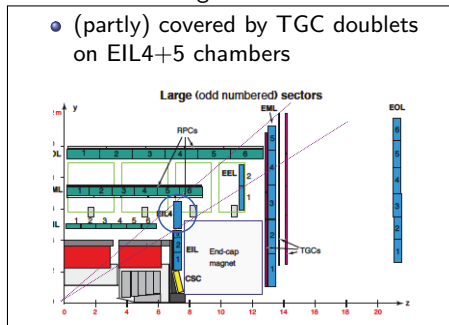
Small sectors

- No trigger chambers



Large sectors

- (partly) covered by TGC doublets on EIL4+5 chambers

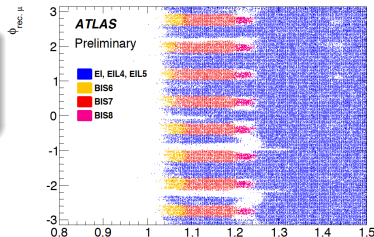


BIS78-Project

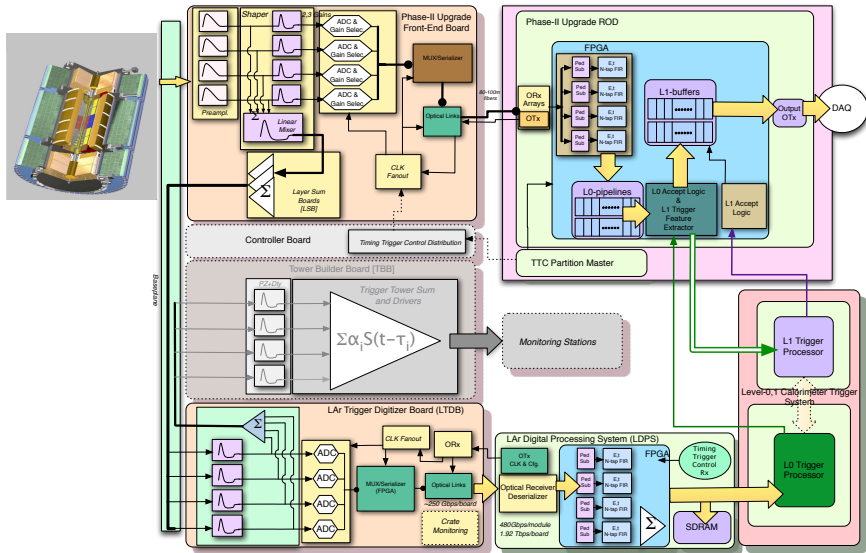
- add 3-layer RPC chambers in **BIS7** and **BIS8**
- 3-layer setup to allow stand-alone capability

Also: replace BIS7 and BIS8 MDTs with sMDTs

- More space to host RPCs
- Better performance at high rates



LAr Calorimeter Electronics for Phase-II



LAr front-end readout architecture for Phase-II

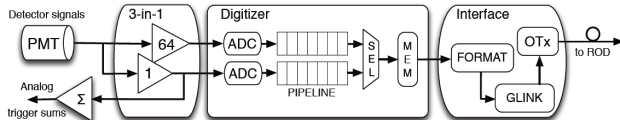


Tile Calorimeter Electronics for Phase-II

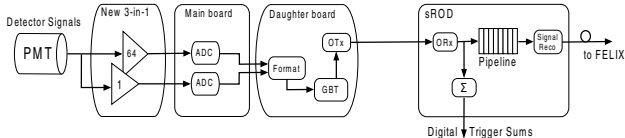
Complete replacement of front-end and back-link electronics

- Digitization and data transfer off-detector of all readout channels at 40MHz
- Digital information to L0/L1 trigger

Present:

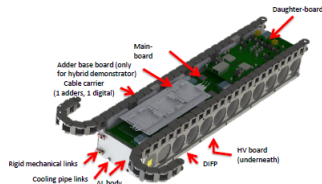


Phase-II:



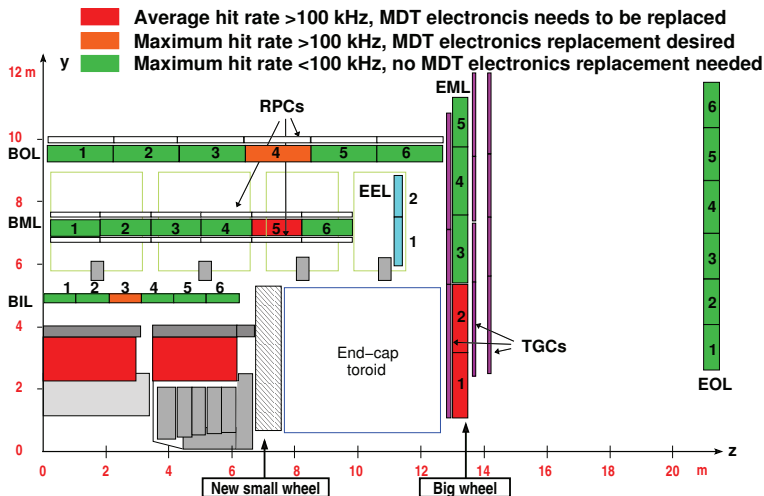
Mini-Drawers

- Reduced complexity, half the size
- Independent modules (separate power, cooling ...)
- Redundant and independent readout incl. optical transmission



Replacement of MDT Electronics in Phase-II

Replacement of MDT read-out electronics on chambers with high background rates:

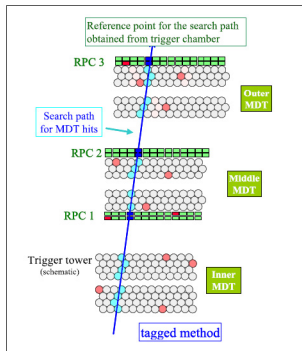


- Capable of L1 trigger rate and long latency in high background regions
- Additional fast read-out chain for MDT L0/L1-trigger



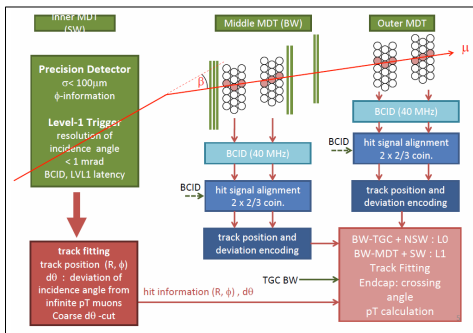
MDT precision coordinates for Phase-II trigger

Rol seeded method:



Use Rol of high- p_T track defined by trigger chambers as a search road for MDT hits

Self seeded method:



Search for track segments with small deflection angle β

