FPGAs in ATLAS Front-End Electronics

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ASICs or FPGAs in on-detector electronics?

Three parameters influence the choice: flexibility requirement, radiation environment and cost
ASICs – mostly NRE cost -> total cost decrease with increased number
FPGAs – mostly unit cost -> only a small decrease with increased number

If you need a moderate number of complex front-end electronics units where you can anticipate future modifications placed in a moderate radiation environment RAM based FPGAs are a strong alternative.

TileCal is definitely such a case also some places/functions in Liquid Argon and the Moun detector as well.

Liquid Argon Calorimeter Electronics and FPGA

For the Liquid Argon Tower Builder Board demonstrator, we are planning to use Kintex 7 primarily to route signals from ADCs to the optical links.

The board will be place in the liquid argon calorimeter barrel and end cap crates

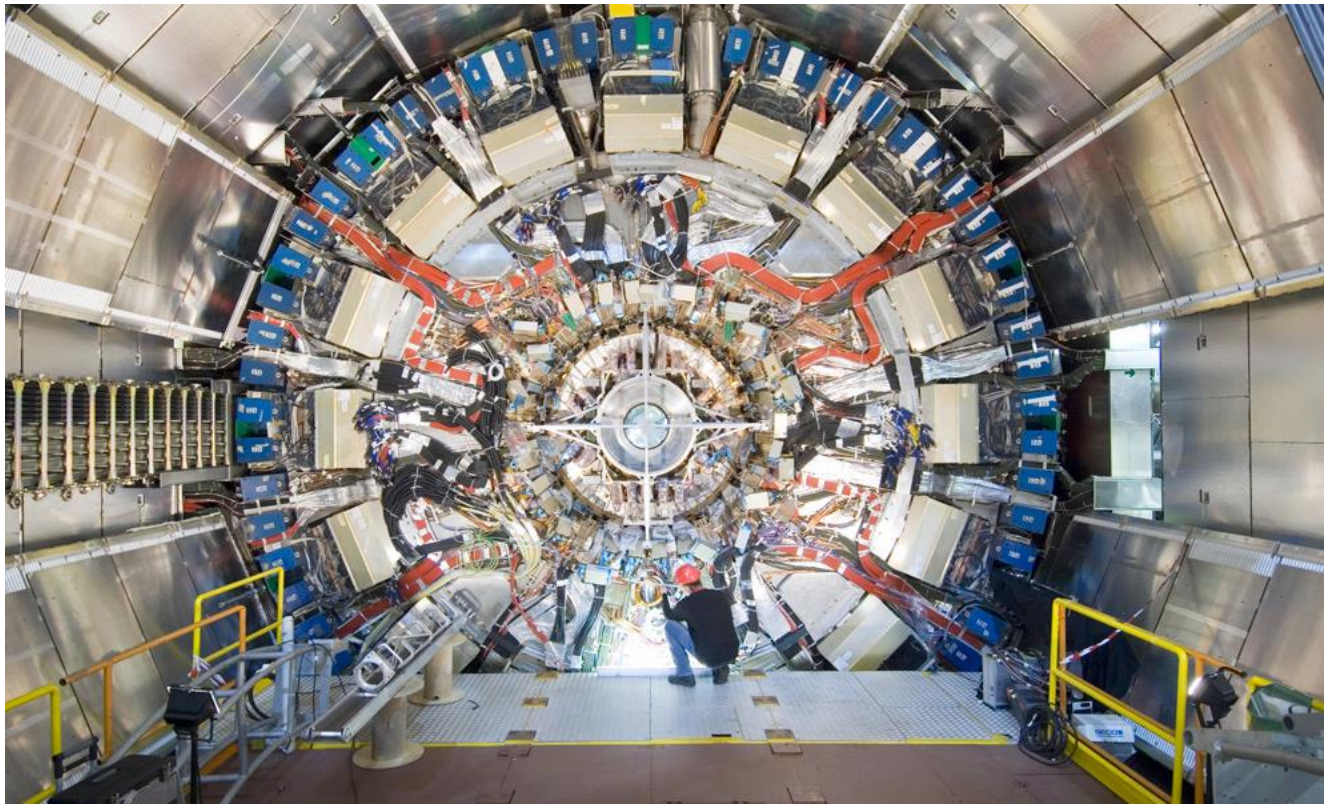
At these positions the FPGA is subjected to low ionization dose but a high flux of high energy hadrons

We expect 100 kRad of ionizing dose for 3000 fb^{-1} of integrated luminosity

The total flux of high energy hadrons is 2.84×10^8 hadrons/ cm^2 fb^{-1}

Thus the major problem that we need to cope with is single event upset.

(Slide from H Takai)



Rad-tolerant FPGAs for the New Small Wheel

Background is still uncertain: shielding design not final

On rim of NSW: TID: 9 kRad, NIELS: $2\times10^{13}/cm^2$

- sTGC Pad trigger:
  - Input: ~40 × 5G GTX serial or 108 diff serdes @ 1.6G or 192 @ 800M
  - Large combinatorial logic and/or LUTs
  - Prototype is Kintex
- sTGC Router:
  - Input: 16 x 5G GTP serial
  - Output: 3 x 5G GTP serial
  - Prototype is Artix, IGLOO2 could be possible

On chamber: worst case: TID: 340 kRad, NIELS: $8 \times 10^{14}/cm^2$

- Trigger data serializers:
  - Input 96-128 DDR diff serdes
  - Output 1 × 5G GTP serializer
  - Baseline: ASIC, 130nm IBM

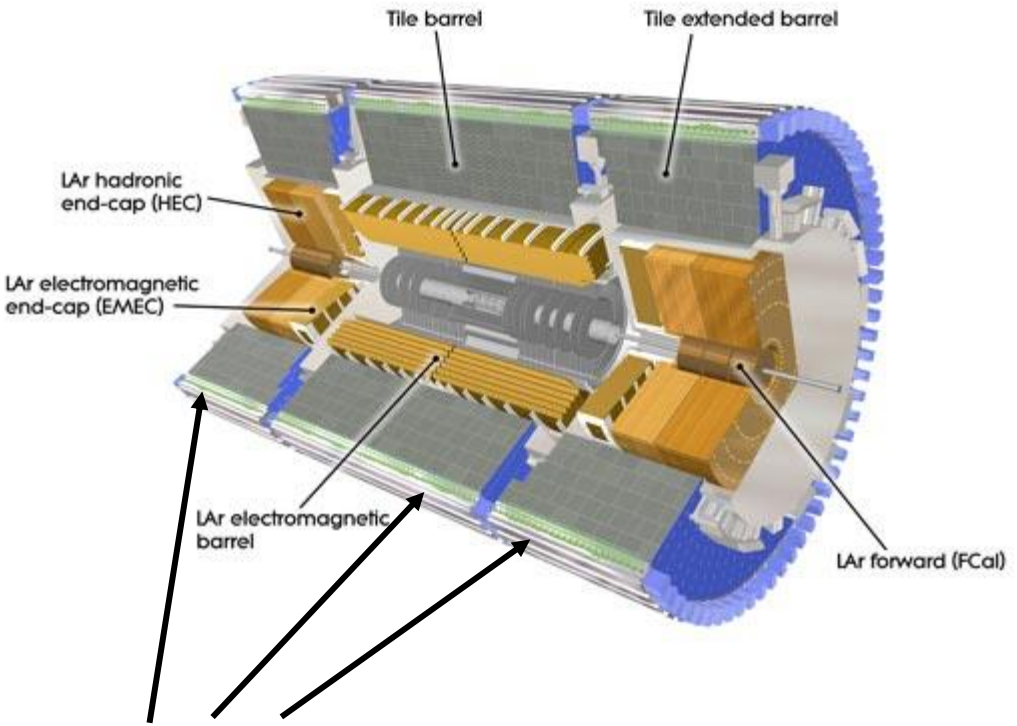
(Slide from L Levinson)

FPGAs in TileCal phase II upgrade

- The requirement for reliable calibrations demand complex on-detector logic.

- Medium number of units: about 2000 medium size FPGAs (Kintex 7) and 4000 small size FPGAs in the present planned upgrade.

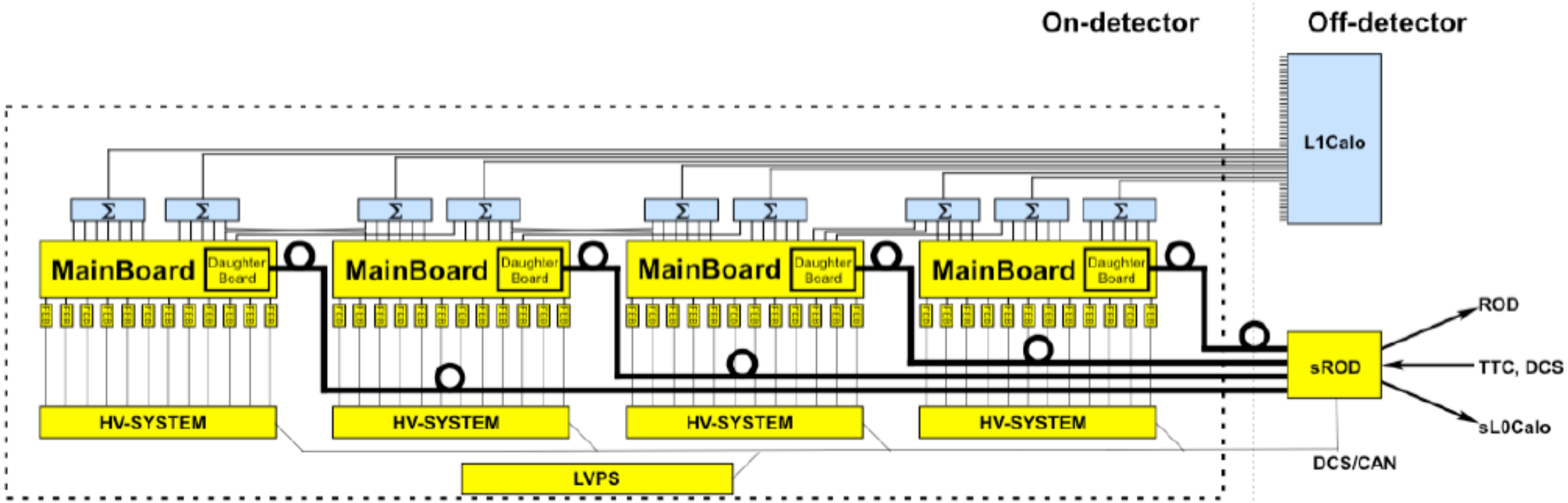
- Low level of ambient radiation



TileCal electronics located in a relatively protected area in the outermost part of the subdetector

The TileCal Demonstrator

An Phase II upgrade design of the TileCal readout augmented to fit the present system to be installed in ATLAS



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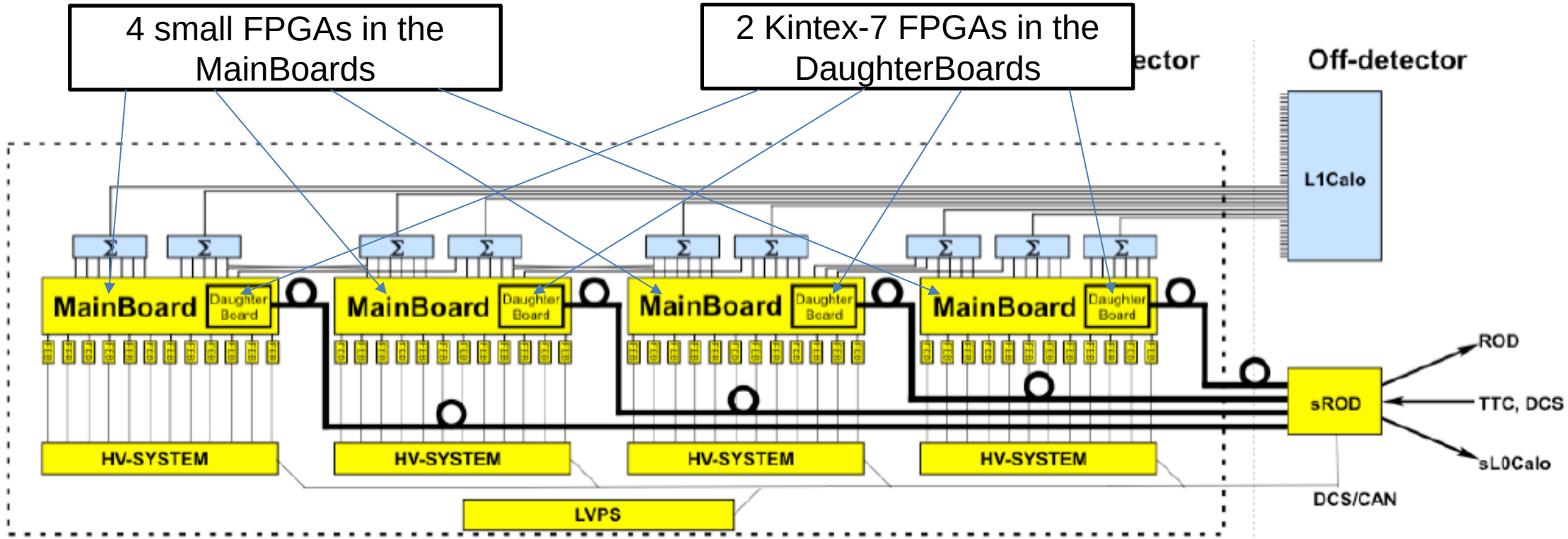
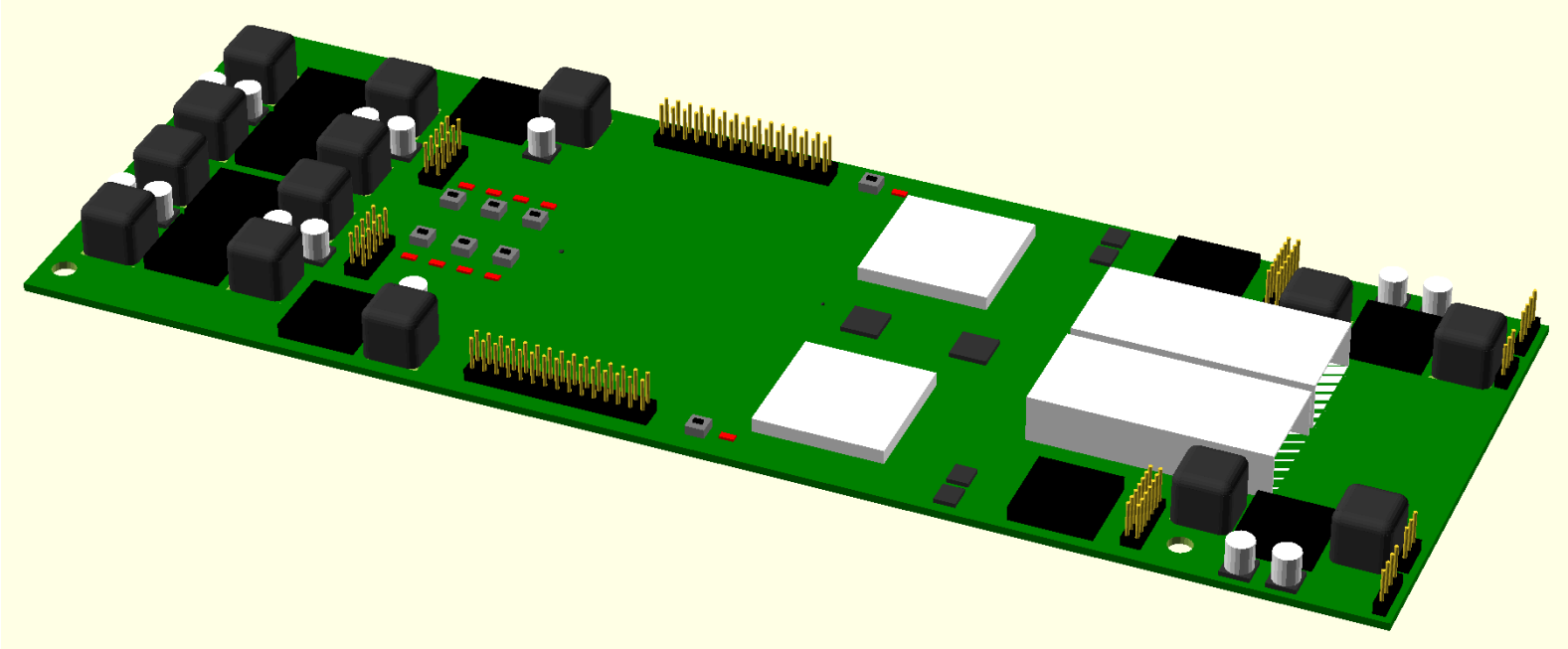


Tile reliability strategy

Each readout modules consists of two largely independent symmetrical sides.
These sides are reading out the same set of calorimeter cells.

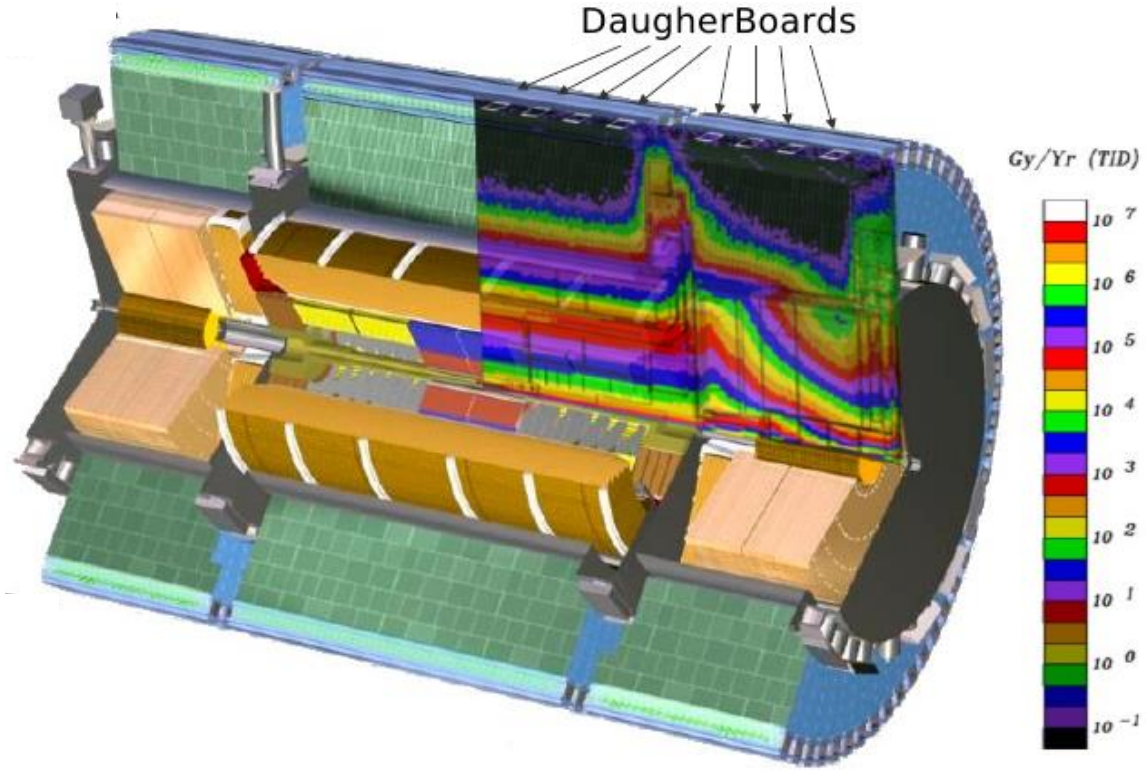


Thus, if one side fails we will not lose any events just statistical quality

All components will be tested for radiation tolerance

Radiation levels

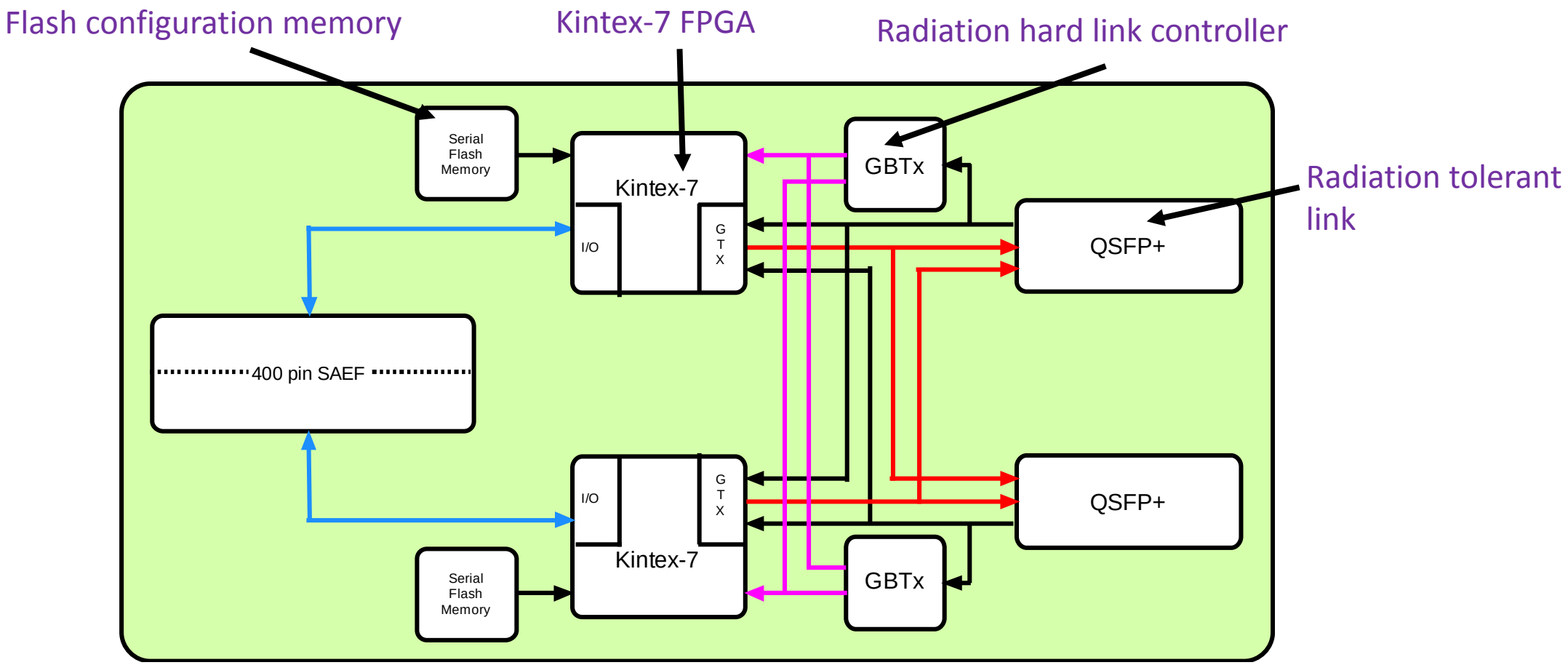
TID: < 2 Gy/year
<10^{10} p/cm^2/year



- According to the results presented by Helio Takai we should expect about 3 single bit errors per day and one double bit error per three days (the tile level is about 1 tenth of that of LAr)

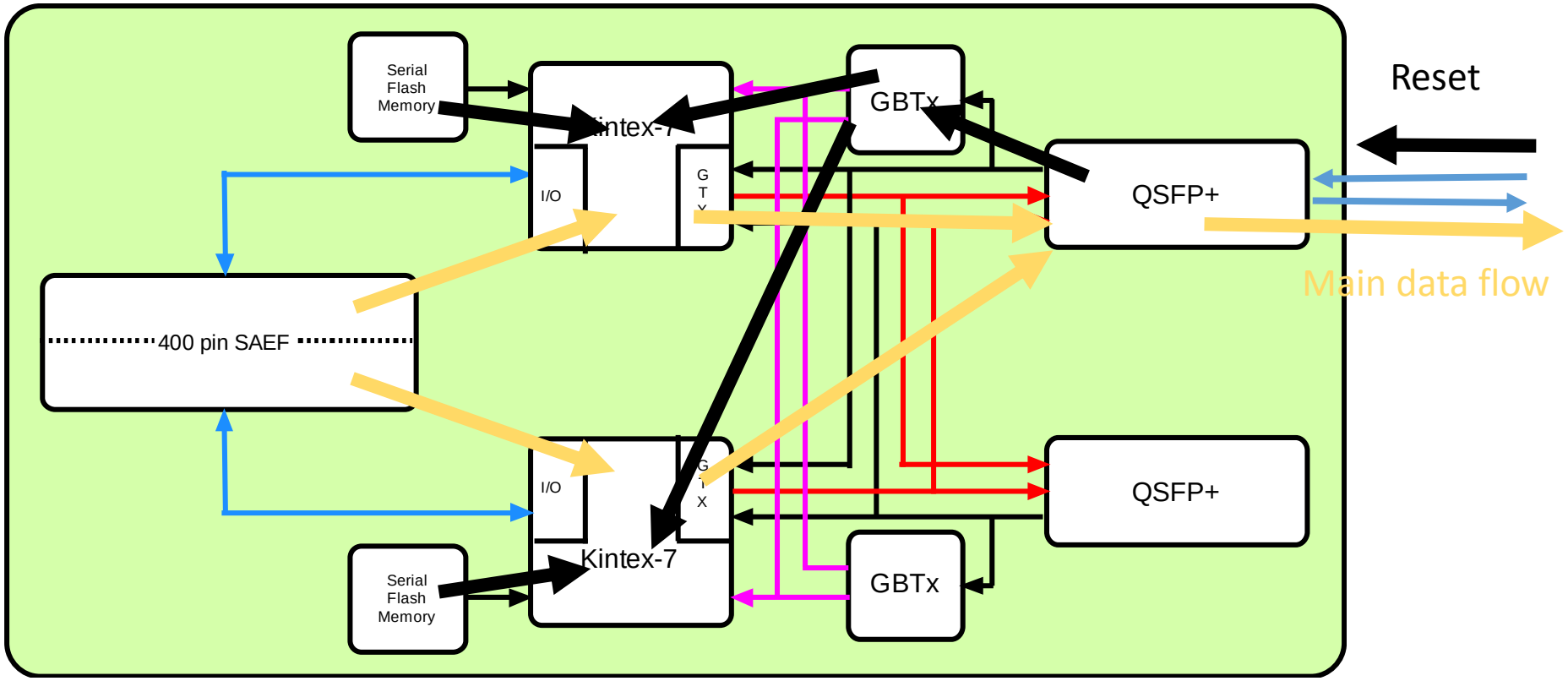
- A preliminary evaluation of radiation test made at MGH in Boston last Saturday gave an estimated 10 SEU:s per day.

DaughterBoard components

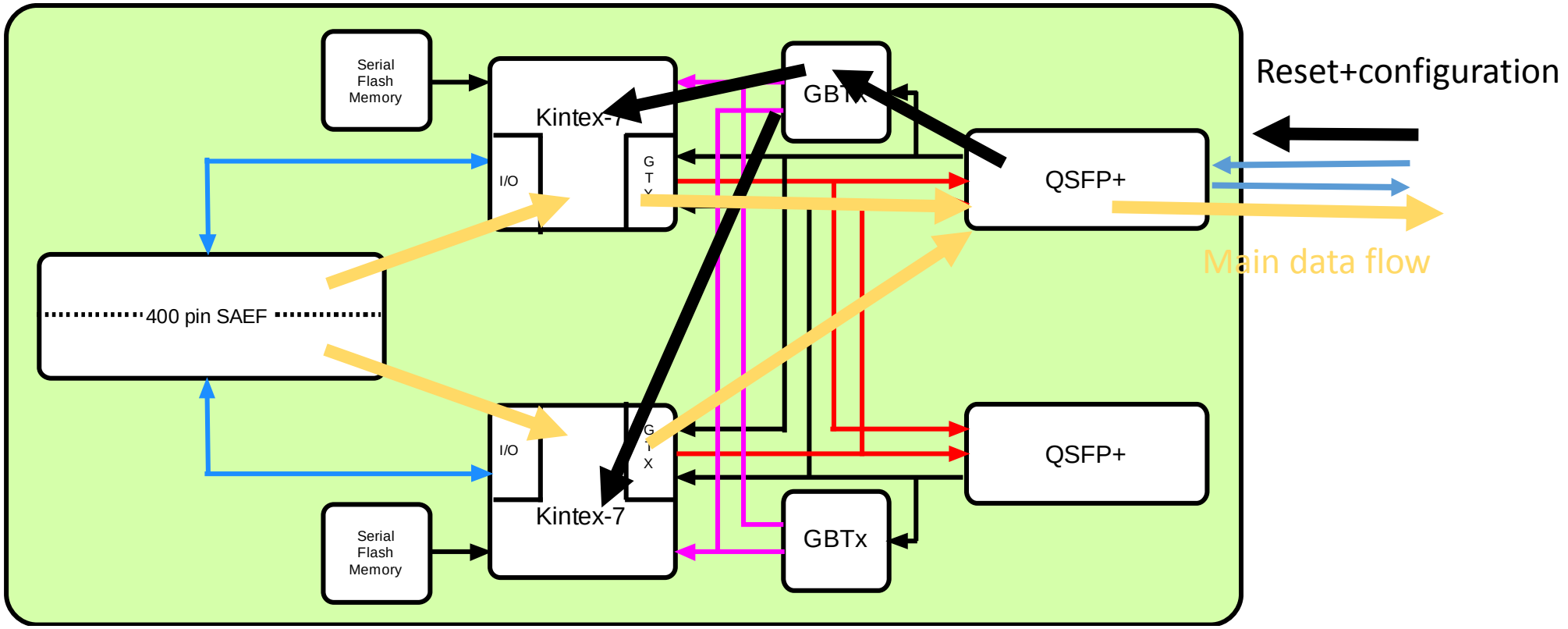


Next (final?) version to be delivered in 3 weeks

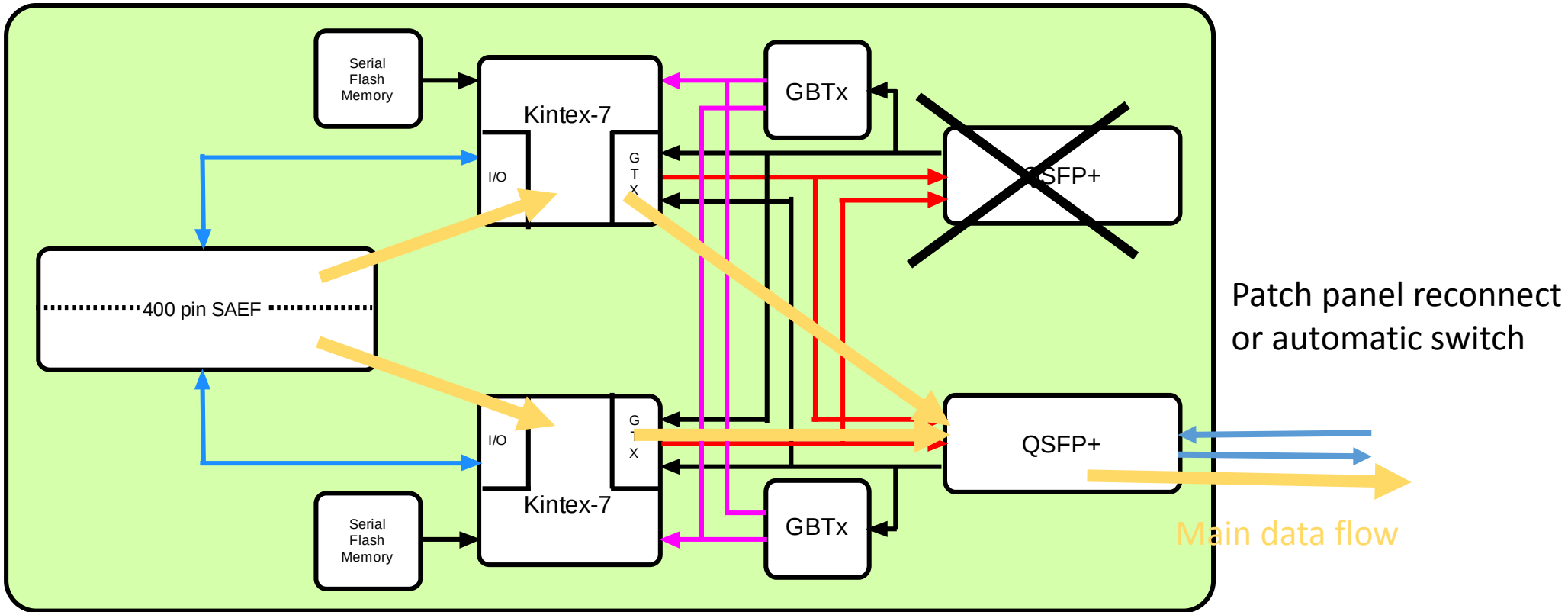
DaughterBoard configuration after reset



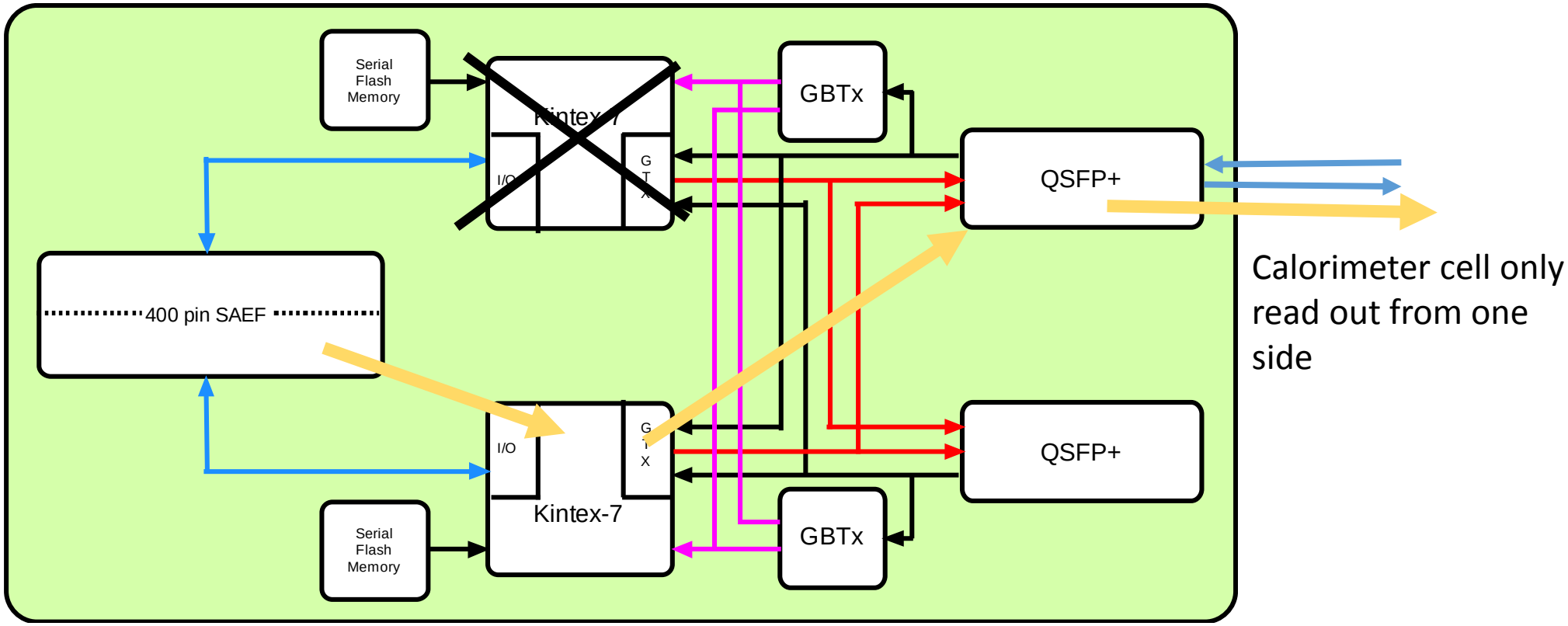
Remote Configuration



Link failure

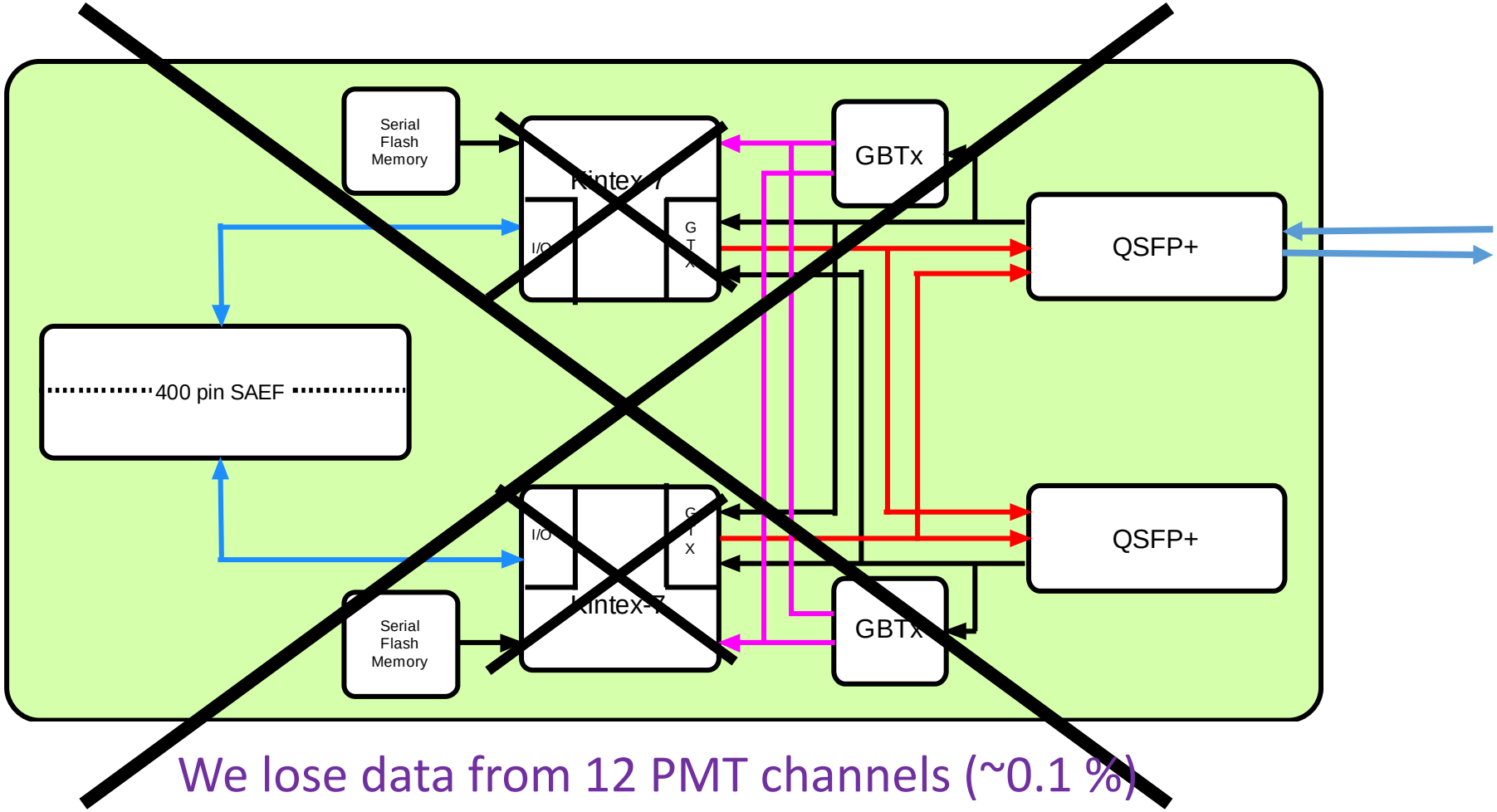


FPGA failure



Precision loss but no loss of data

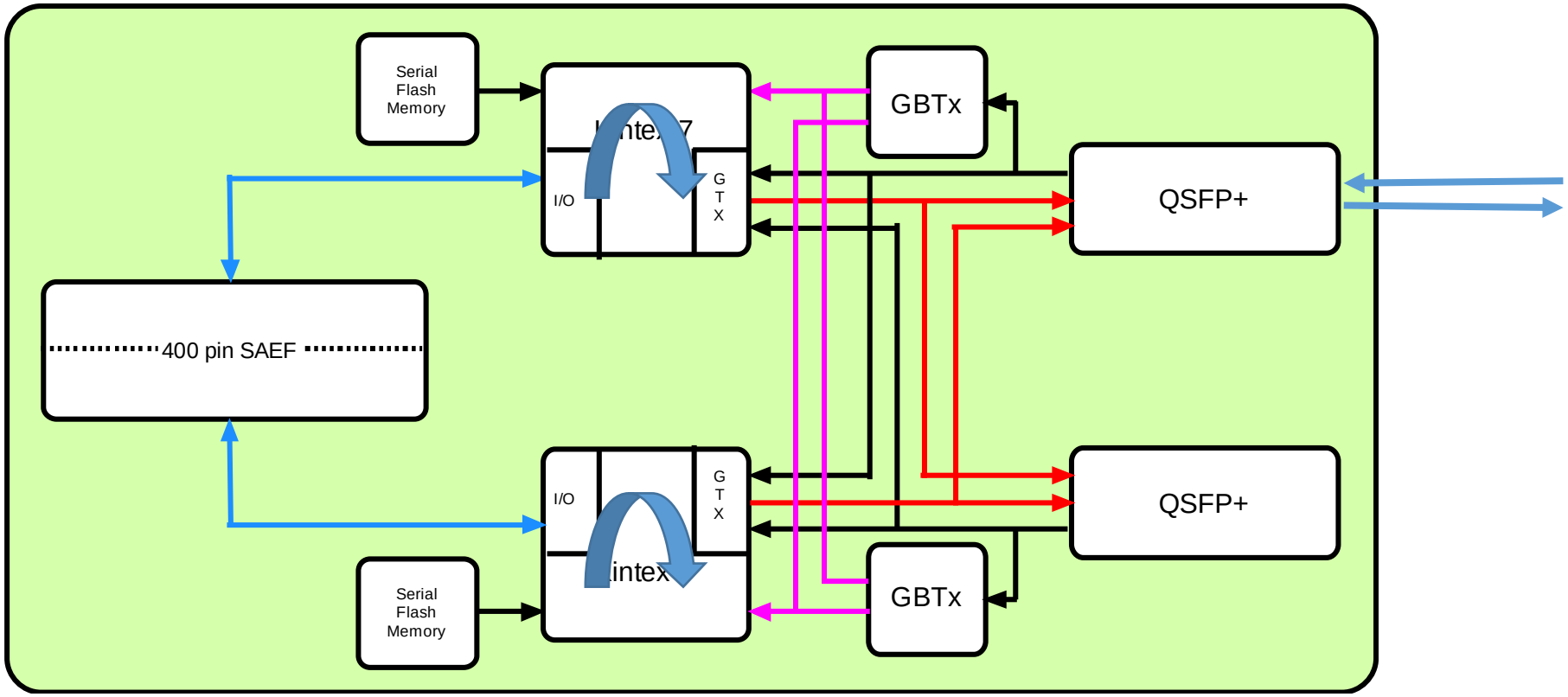
Loss of both FPGAs or both links



We lose data from 12 PMT channels (~0.1 %)

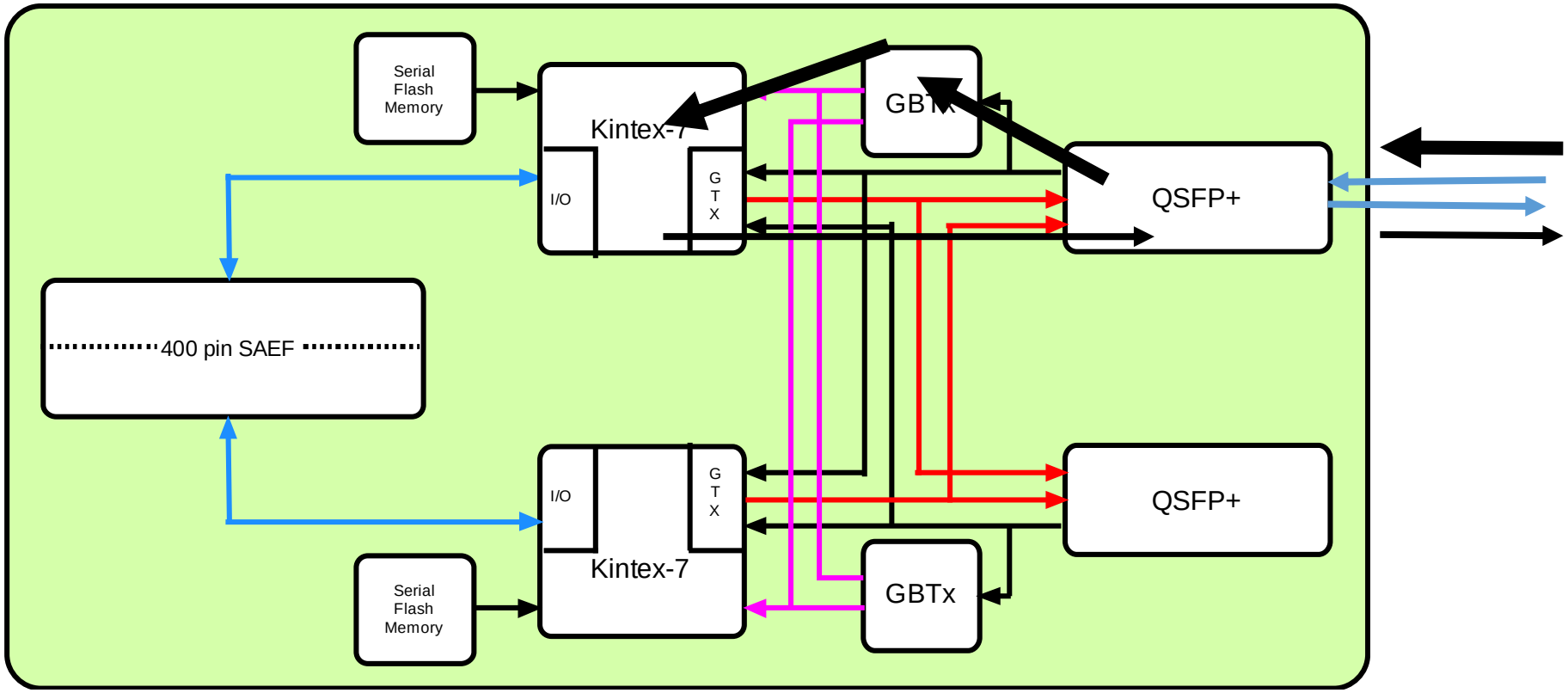
Intended FPGA error mitigation

Scrubbing of configuration memory



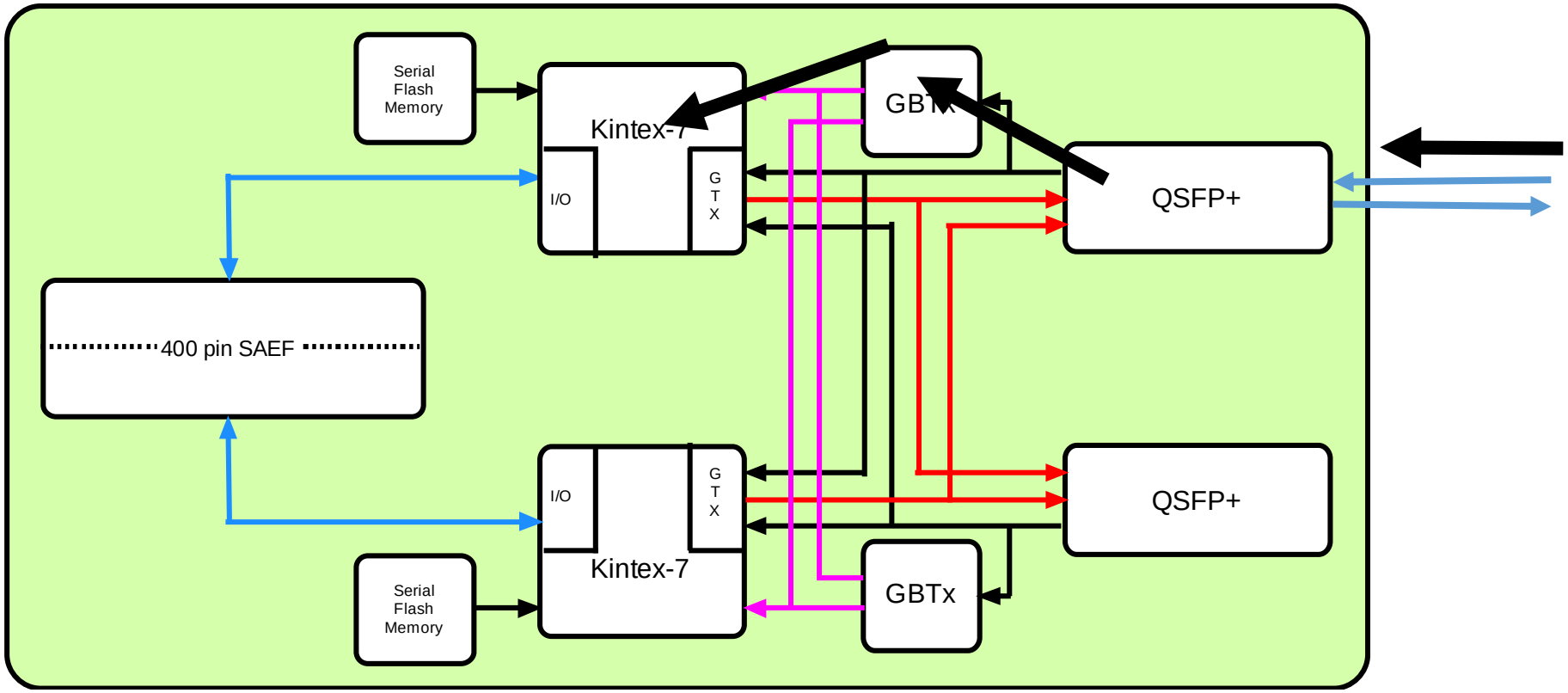
Intended FPGA error mitigation

Partial re-configuration



Intended FPGA error mitigation
Watch dog activated full re-configuration

Watch dog function: Data corruption or differences in check sums calculated on ADC data and data delivered off detector



Conclusion for the TileCal Demonstrator

- The TileCal Demonstrator development has up to now concentrated on functionality
- Implementation of FPGA error mitigation next step

Conclusion

The new hardware and error mitigation techniques allow HEP front-end electronics to follow the general trend of replacing ASICs with FPGAs in areas with moderate radiation levels