Workshop on FPGAs for High-Energy Physics

Single-Event Effects Testing
and the
Xilinx Radiation Test Consortium

presenter: Gary Swift

SWIFT ENGINEERING & RADIATION SERVICES, LLC

March 21, 2014

Overview

- SEE Testing for Space
  - Accelerated AND Accelerator-based Testing
  - Purpose
    - On-orbit rate
    - Fail signatures and design level mitigation
- XRTC (Xilinx Radiation Test Consortium)
  - Voluntary membership
  - Maximize Leveraging
  - Test Campaign Phases:
    - Static
    - Dynamic
    - Mitigation
  - Beam and/or Fault Injection Common Setup

SEE Testing's Basic Principle

SEE testing is extremely easy.

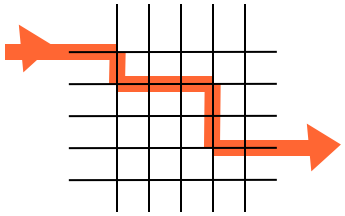
1. It's simply counting

2. Only two things to count:
   - Number of upsets
   - Total beam fluence

3. The facility counts the beam for you.

FPGAs: What bits can upset?

- Configuration Bits
  - Logical Function
  - Routing
  - User Options
- Block RAM
- User Flip-flops
- Control Registers



- × NAND
- × Ex-OR
- × Flip-Flop type
- × etc…

- × Type of I/O
- × Mode of Block RAM Access
- × Clock Manager
- × etc…

SEE Testing Is Hard

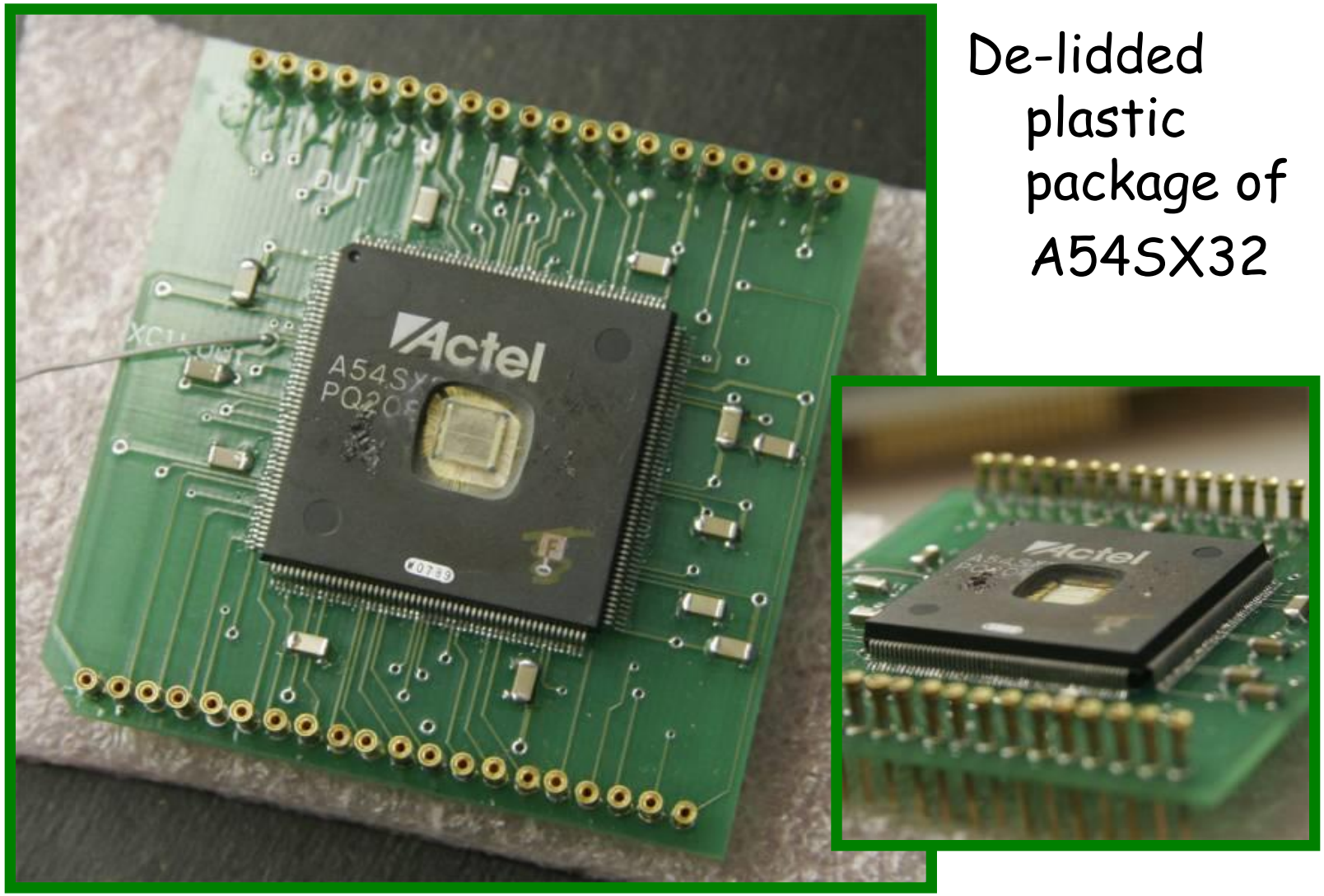
Difficult to do

High-Energy Accelerator
- Beam costs ~ $1000/hr
- Travel & shipping add extra costs
- Portable test fixtures and control systems

Test Development

Special Problems
- Part De-lidding
- In Vacuum Operation

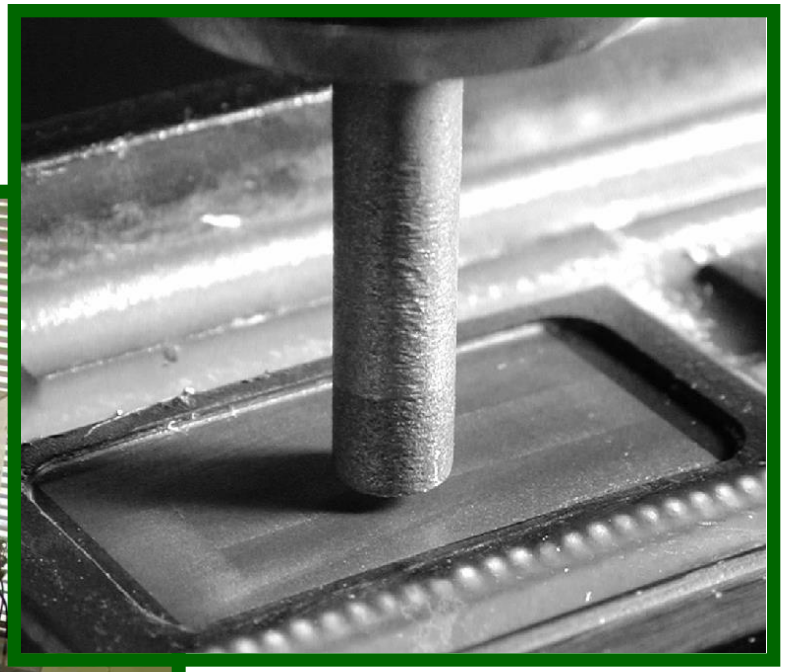
Acid Etch Plastic to Expose Die

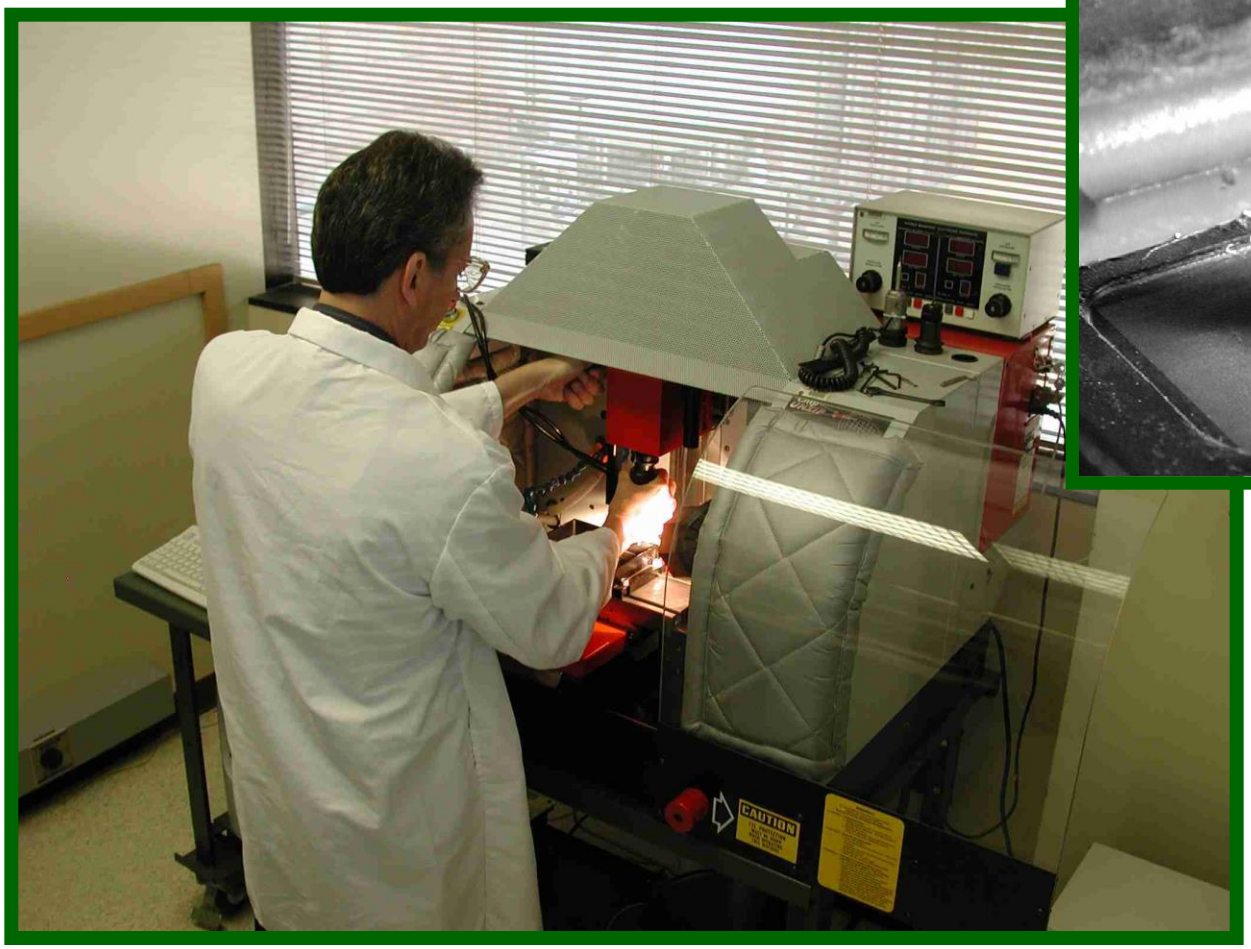


De-lidded plastic package of A54SX32

Preparation: Thinning Flip-Chip

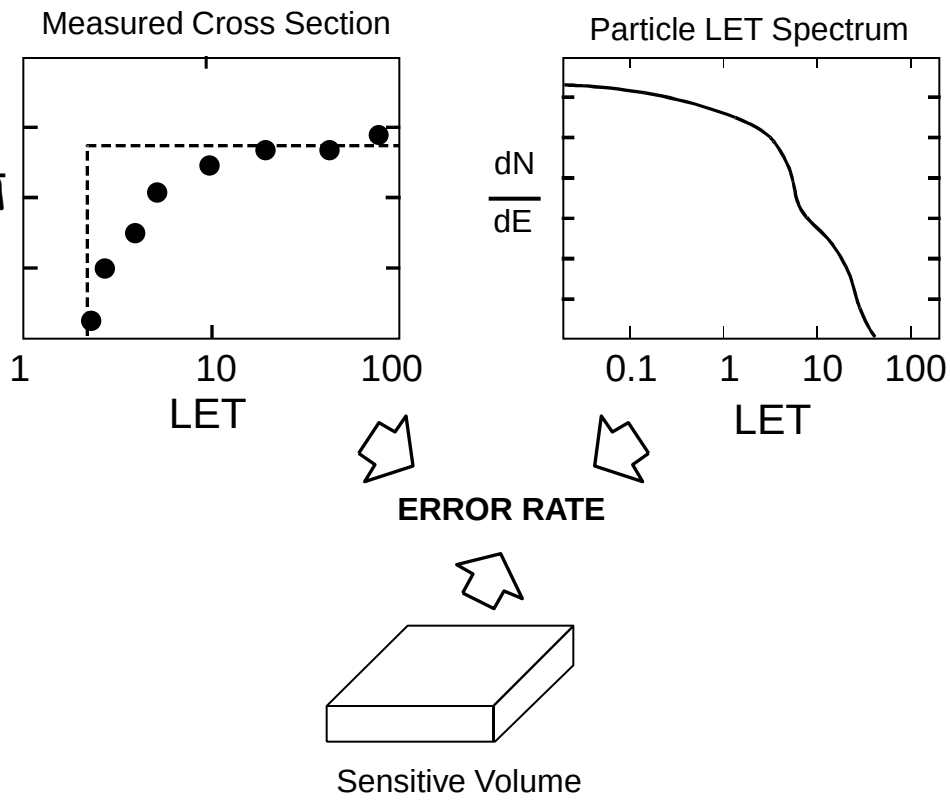
Technician thins DUT backside





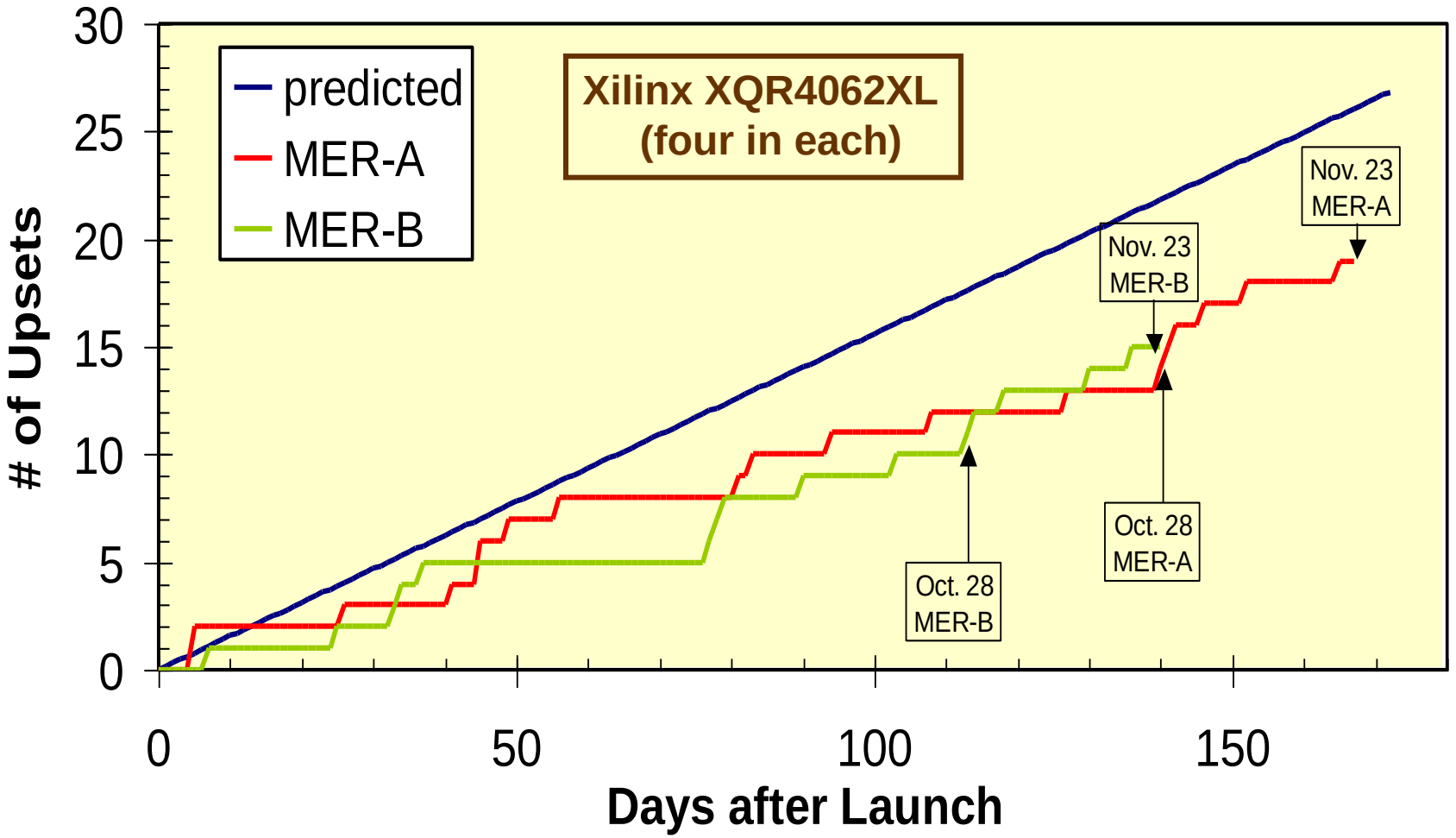
Space Upset Rates – Three Inputs

- Measure σ vs. LET
  - Testing done at high-energy accelerator
  - Cross-section determined from circuit response
- Determine Sensitive Volume
  - Requires assumptions about device construction
  - Used to determine effect of ions that strike the device at an angle
- Integrate with LET Spectrum



Prediction vs. Actual

Example: Rovers Going to Mars - Pyro Control Board



Lots of Interest ➡ Lots of Leveraging

Xilinx, Inc. and JPL started partnering on tests

JPL

XILINX®

and soon had to form the Radiation Test Consortium

THE AEROSPACE CORPORATION

Los Alamos NATIONAL LABORATORY EST. 1943

NORTHROP GRUMMAN

SEAKR Engineering

MDA

Goddard Space Flight Center NASA

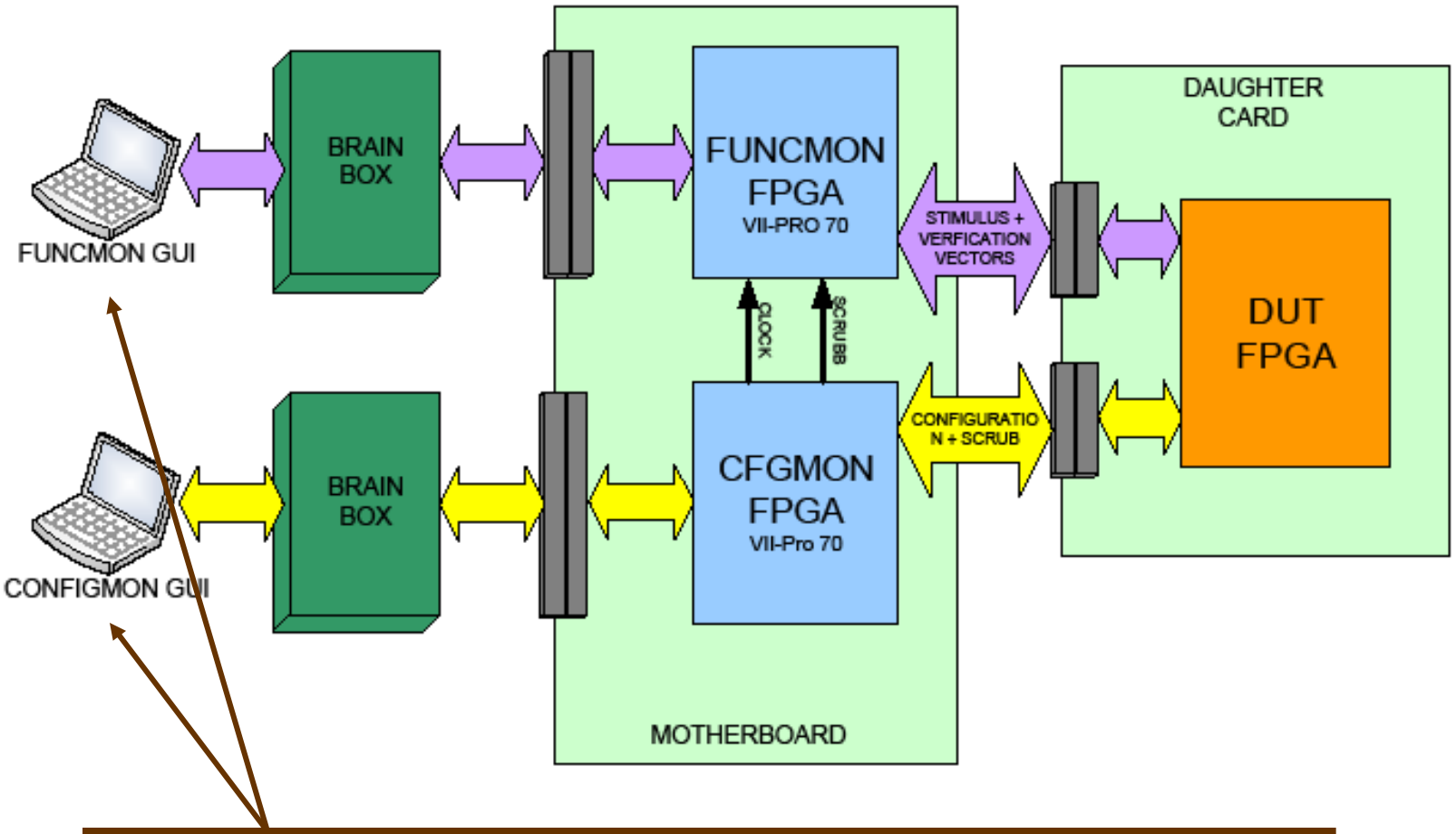
Boeing Satellite Systems

Sandia National Laboratories

BYU BRIGHAM YOUNG UNIVERSITY

NASA Langley Research Center Hampton, Virginia

XRTC Test Infrastructure



Capturing detailed strip charts allows experiment to be "re-played" for smarter signature identification and later analysis and re-analysis.

Example – Strip Chart of Irradiation

```
---------------- Log Start ----------------
Comment: Ar lo MeV/u, FX1 sn: AA4419 on board 6

Time/date, Counter0, Counter1, Counter2, Counter3, Counter4, Counter5, Co
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
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12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:43 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:44 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:44 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
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12/20/2009 3:39:44 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:44 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
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12/20/2009 3:39:44 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
12/20/2009 3:39:44 PM, 80000000, 80000000, 80000000, 80000000, 80000000,
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⋮

XRTC Motherboard History

2000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 20

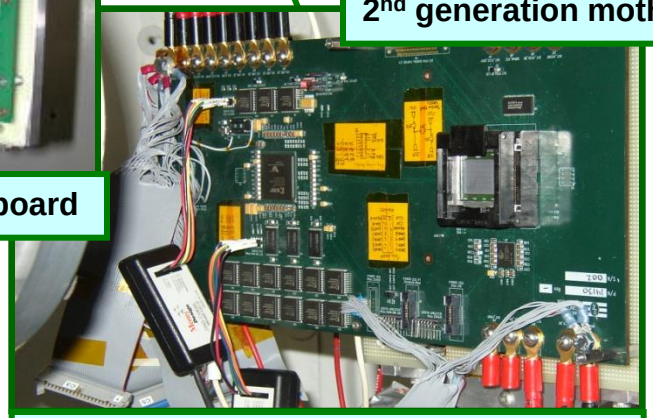
Virtex-2 | Virtex-IIpro | Virtex-4 | Virtex-5

JPL & Xilinx partner up

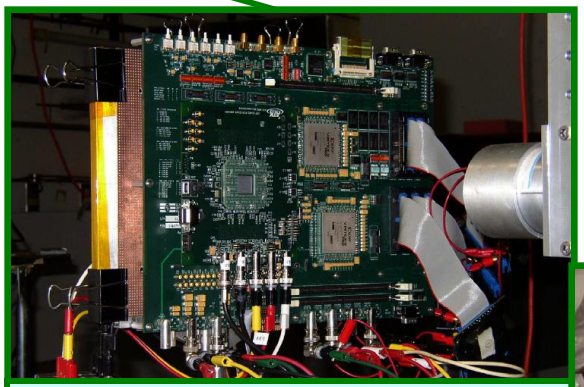
Consortium formation

1st Annual Meeting

0th generation motherboard



1st generation motherboard



2nd generation motherboard

3rd generation motherboard

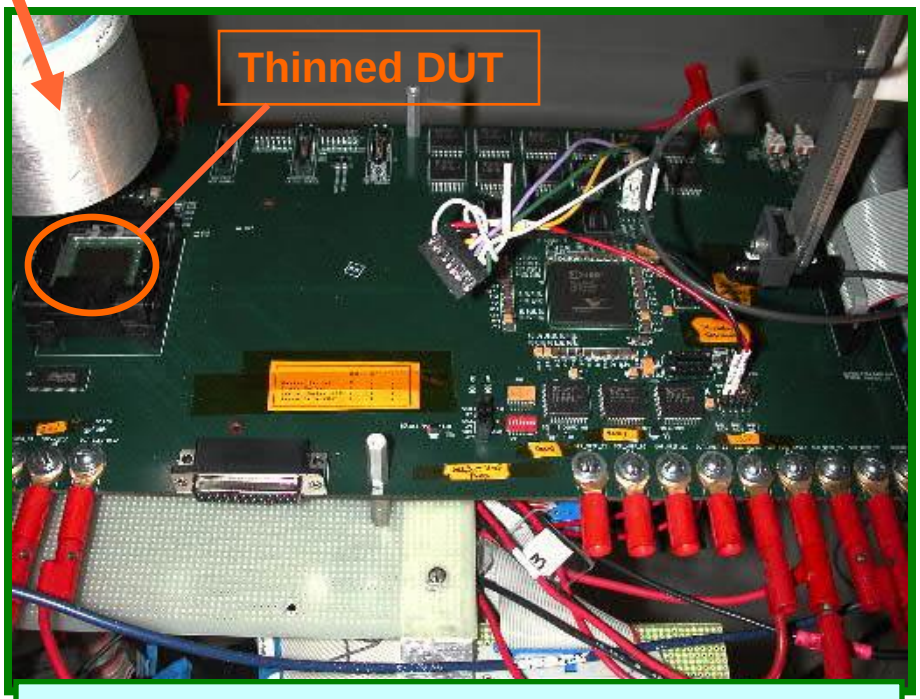
BOTH Fault Injection & Irradiation

- Dynamic Test Setup at Texas A&M Cyclotron

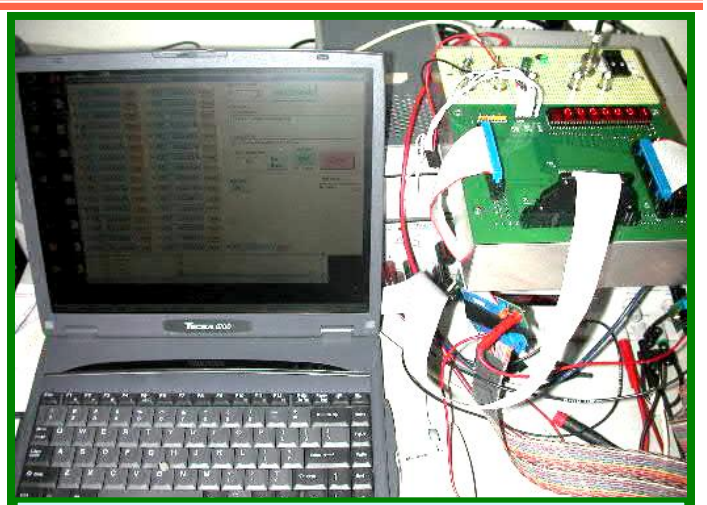
Inside target room

BEAM

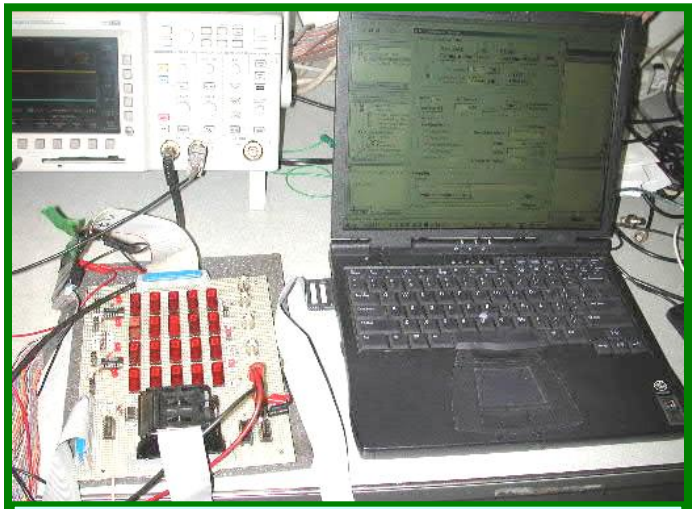
Thinned DUT



SEAKR-built DUT Board - XQR2V6000 in beam

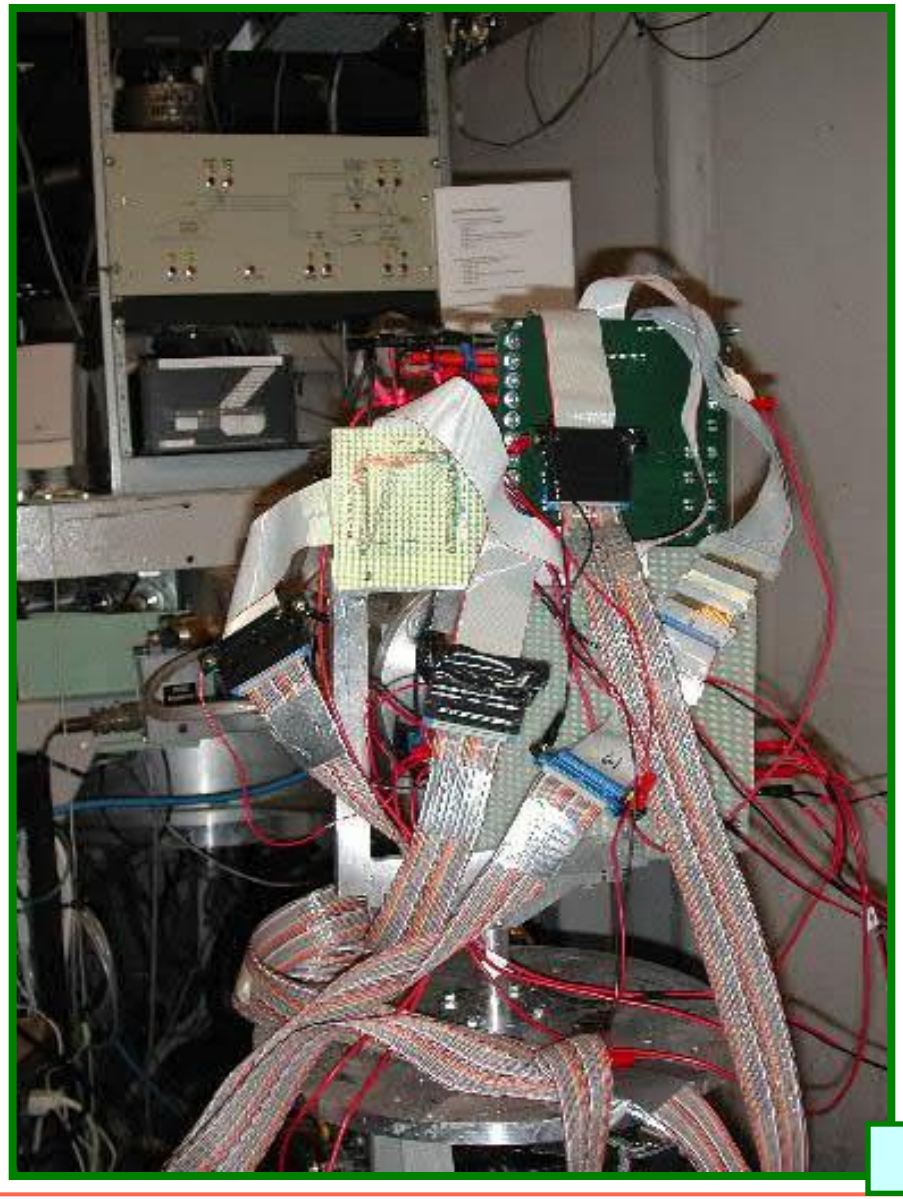


Functional Monitor/ Strip Chart



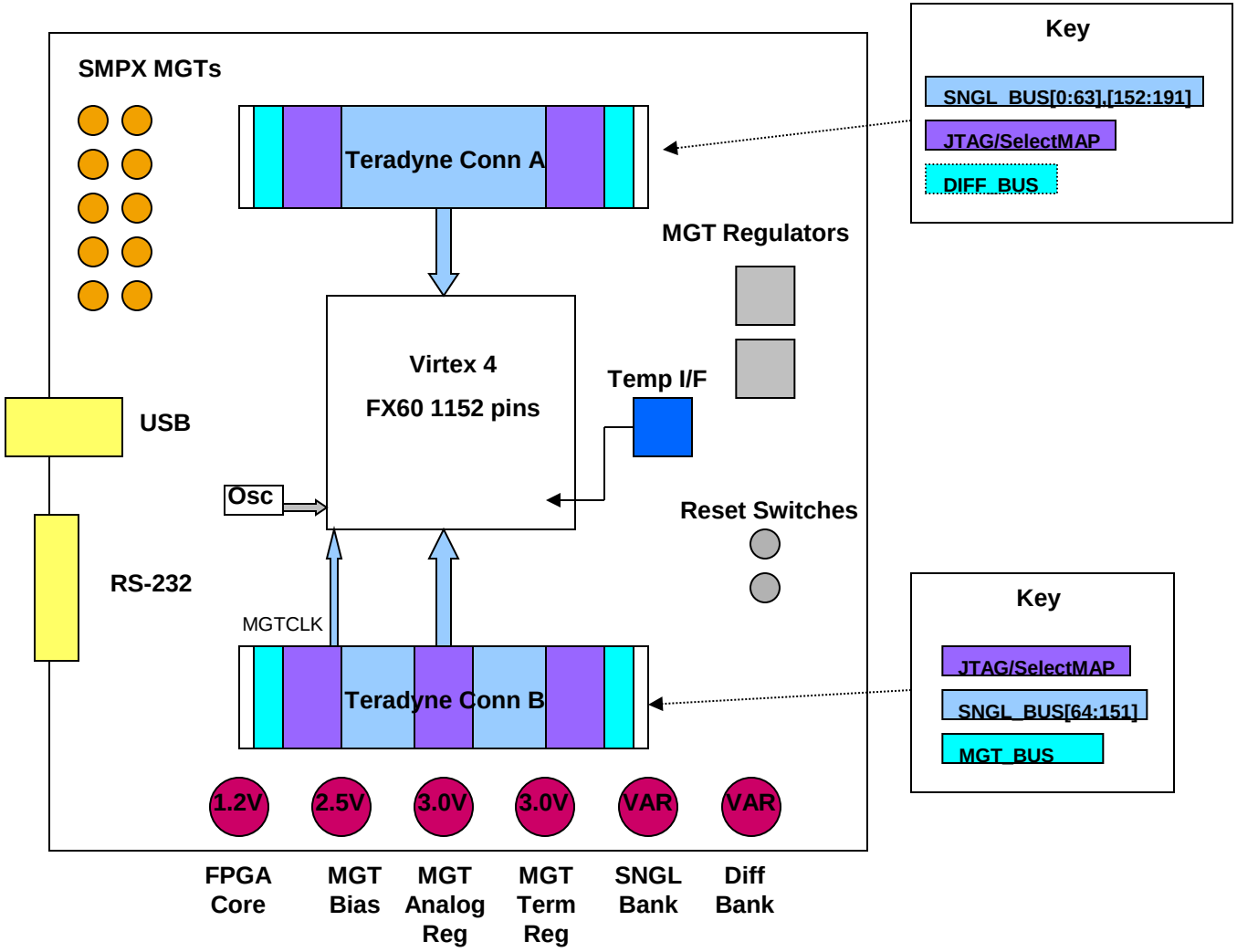
Configuration Monitor/ Strip Chart

Lots of Signals = Messy Looking

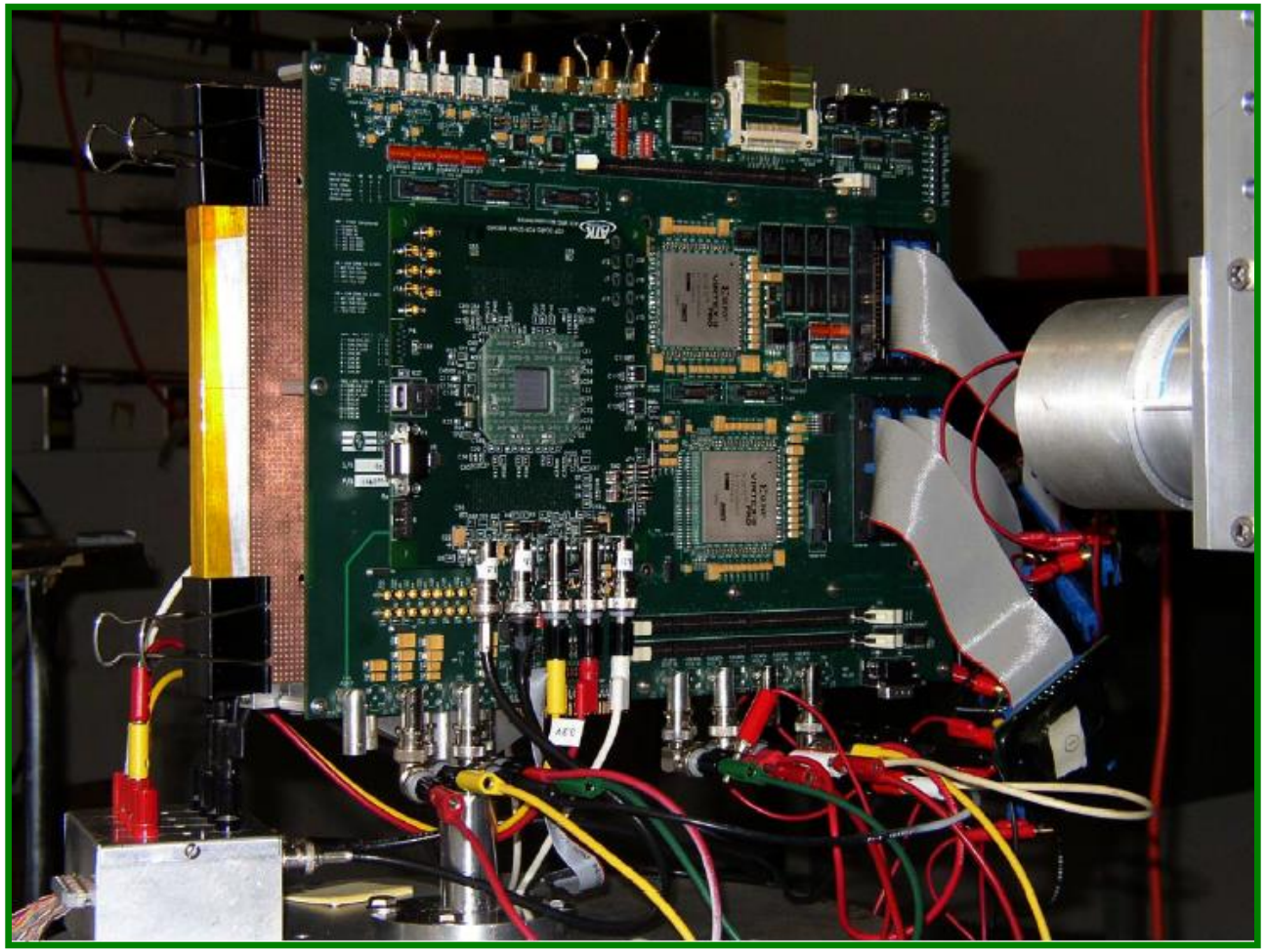


Backside

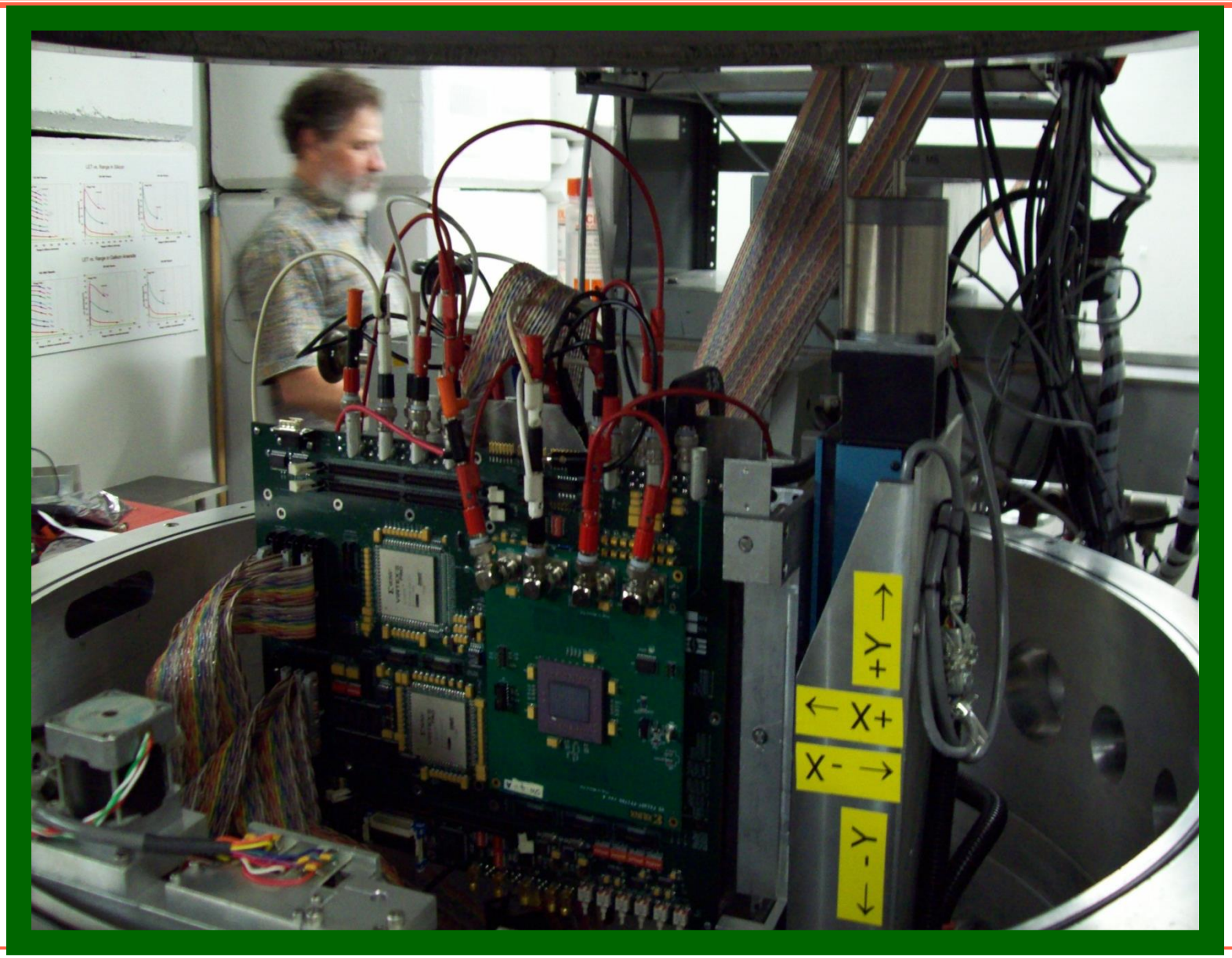
2nd Gen+ Setup – DUT Daughter Card



2nd Gen. Consortium Test Board



In-Vacuum Test at Texas A&M



Some significant events

Nov '08 - First silicon V-5QV into beam
followed by many tests, approx. monthly

May '09 - SpaceCube flies on Hubble Repair Mission
with the first V-4's in space

Nov '09 - First XRTC space experiment launched
with first V-4QV in space (& SpaceCube again)

July '10 - Official V-5QV Product Announcement (at NSREC)
plus shipping engineering samples to EA customers

May '11 - 2nd XRTC space experiment launched
with first V-5QV (ES) in space

July '11 - Official V-5QV Release Announcement (at NSREC)
plus shipping flight parts

Nov '11 - First production V-5QV launched

Feb '12 - 10th XRTC Annual Meeting

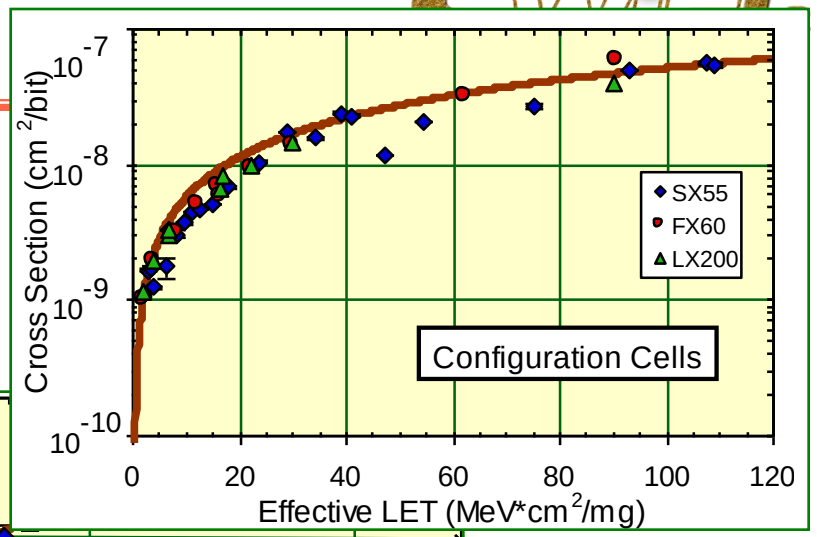
XRTC Mission: Beam Testing

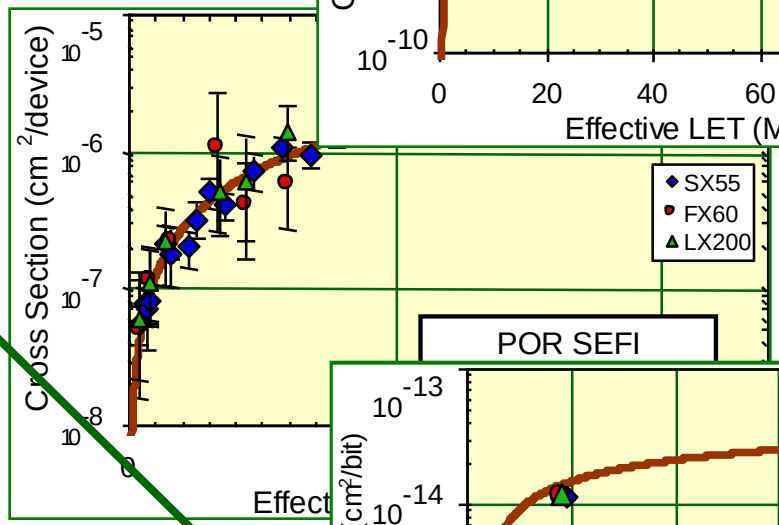
- Feb '09 thru Jan '10 = 451 hrs of beam
- Feb '10 thru Jan '11 = 552 hrs of beam
- Feb' 11 thru Dec '11 Tests = 392 hrs of beam
- Main Proton Test Campaign:
  - UCD, Nov 2011 — 40
  - UCD, Jan 2012 — 40
  - UCD, June 2012 — 28
  - UCD, October 2012 — 16
  - UCD, November 2012 — 45
  - UCD, December 2012 — 48
- "Cleanup" Heavy Ion Tests:
  - LBL, April 2012 — 16
  - LBL, May 2012 — 16
  - LBL, August 2012 — 16
  - TAM, August 2012 (BYU/SEAKR) — 12
  - TAM, Sept. 2012 — 94

Total 371 beam hrs

XRTC Mission: Test Results

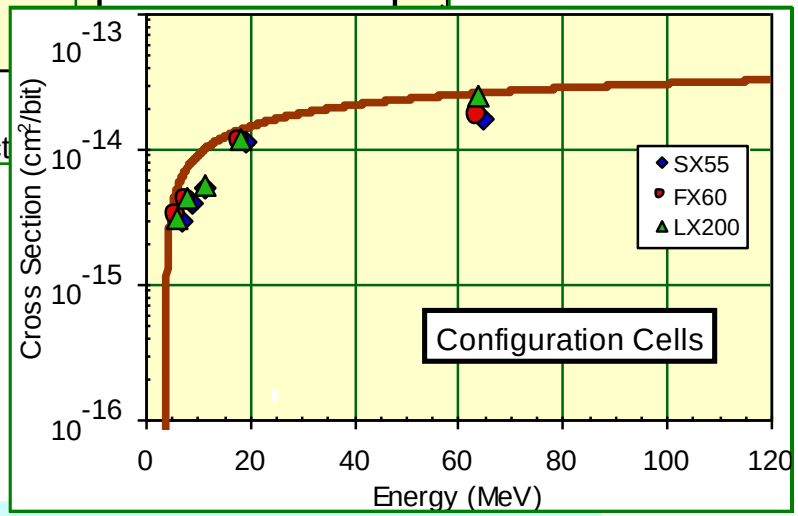
- Static Results on Virtex- 4QV
  - -- Config cells
  - -- User BRAM & FFs
  - -- Functional Upsets
  - - (aka SEFIs)
- - Both heavy ions & proton





Virtex-5QV

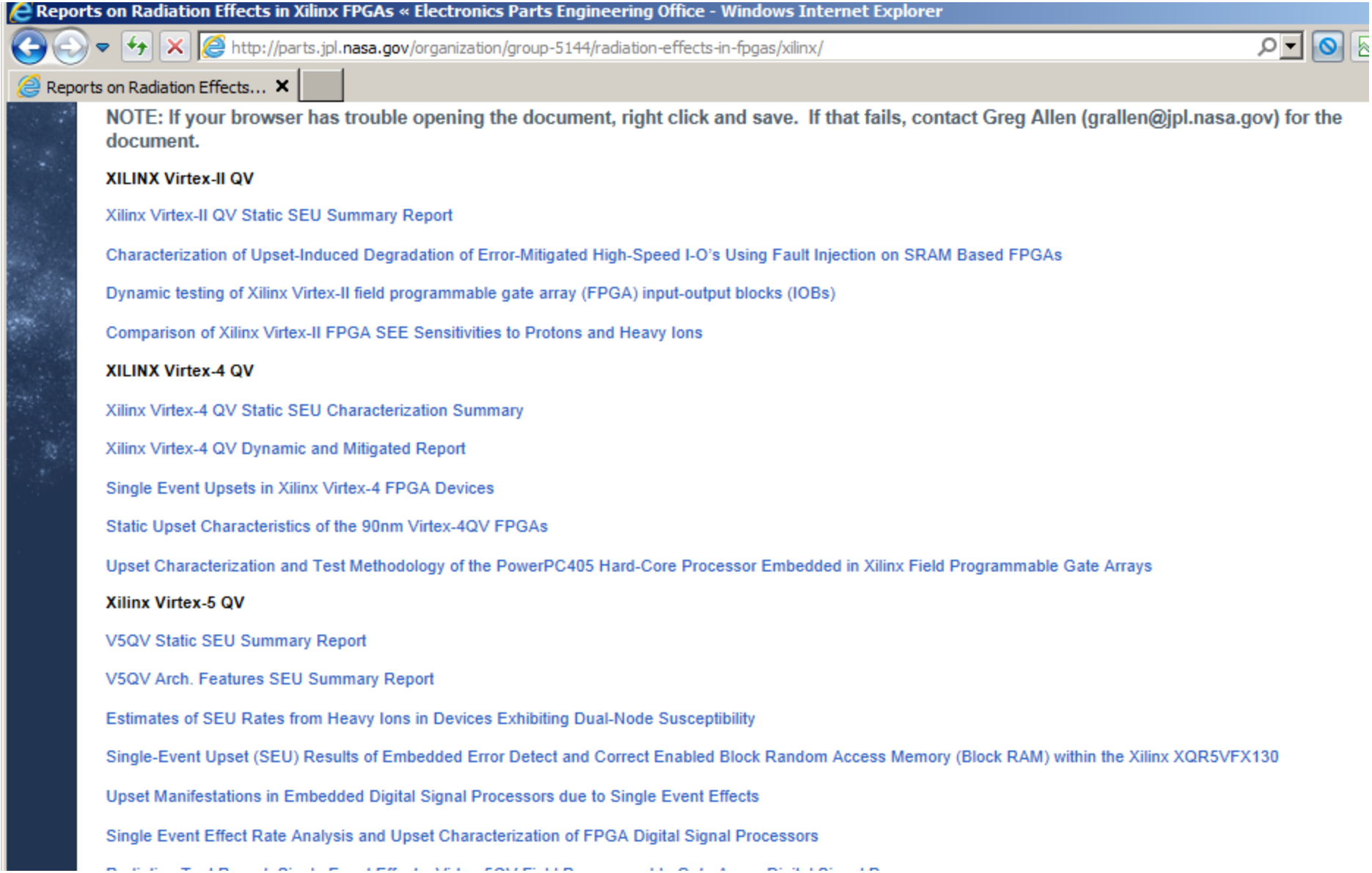
- Static Report
  - -Release 3 May 2013
- Architectural Features Report
  - -Release 2 Aug. 2013



- Reports hosted on JPL website:

http://parts.jpl.nasa.gov/organization/group-5144/radiation-effects-in-fpgas/xilinx/

XRTC Test Reports



XRTC Annual Meeting – 2.5 Days

Day Two	Thursday March 1, 2012		
Session/Time		**Presentation**	**Presenter**
8:00a		***Continental Breakfast***	
B. Virtex-5QV Rad Test Results & Plans (cont'd)			
8	**8:30a**	Overview of the Static & Architecture Reports	Gary Swift (Xilinx)
9	**9:00a**	DSPs: Overview and Update	Roberto Monreal (SWRI)
10	**9:20a**	SET Filters & User Flip-Flops	Gary Swift (Xilinx), collab: Boeing, JPL
11	**9:50a**	Review of "Raw" MGT Testing & Results	Roberto Monreal (SWRI)
12	**10:10a**	I/O Beam Results: LVCMOS, Reg. & Unreg	Gary Swift (Xilinx), ack: Boeing
10:30a		***BREAK***	
13	**10:50a**	MGTs: Running RapidIO in Beam	David Lee (Sandia), ack: Boeing
14	**11:10p**	MGTs: Running the Aurora Protocol in Beam	Prof. Mike Wirthlin (BYU)
15	**11:40a**	V-5QV Perspective on Half-Latches	Gary Swift (Xilinx)
16	**11:50p**	Clocking Test Results: DCMs & PLLs	Greg Allen (JPL)
17	**12:10p**	I/O Features: DCI, IOSERDES, & IODELAY	Gary Swift (Xilinx), ack: Boeing
18	**12:30p**	Beam Test Results: BRAM FIFO Update	Scott Arlo Anderson (SEAKR)
12:40a		***LUNCH & Solution Center Tours***	
D. Upset Mitigation and IP			
1	**1:30p**	Update on IP Support for Space FPGAs	Ron Digiuseppe (Xilinx)
2	**1:50p**	Plans for a Virtex-5QV DRAM Interface IP	Brian Daellenbach (Northwest Logic)
3	**2:10p**	Update on Xilinx' TMRTool	Carl Carmichael (Xilinx)
4	**2:30p**	Update on LEON-FT & openLEON Testing	Mark Learn (Sandia)
5	**2:50p**	S/W-based Fault Injection and Design Analysis	Lee Lerner (Luna Innovations)
3:10p		***BREAK & New Motherboard/BrainBox Demos***	
6	**3:30p**	XAPP588's Reference External Cfg Manager	YC Wang (Xilinx)
7	**3:50p**	Sandia's Internal Configuration Manager	David Lee (Sandia)
8	**4:10p**	SEAKR's Hybrid Configuration Manager	Scott Arlo Anderson (SEAKR)
9	**4:30p**	Plans for a Reference Internal Config Manager	YC Wang (Xilinx)
10	**4:50p**	First Beam Results: Virtex4 + Precision HiRel	Jeff Kaady (Mentor)
11	**5:10p**	Upset Detection & Mitigation with Software	Nathan Rollins (BYU)
12	**5:30p**	Virtex-4QV Updates and Thoughts	Gary Swift (Xilinx)
5:40p		***Wrap up***	

Basics of Upset Mitigation

- Redundancy -

  Extra information (bits) prevents all upsets from yielding system errors.

- Scrubbing required –

  Accumulation of errors rapidly kills mitigation effectiveness.

- Effective –

  Most spacecraft now fly large arrays of upset-soft memories with few or no errors.

  Typically, uncorrectable errors are detectable.

Basics of Upset Mitigation - cont'd

- Common sense says -

  At some point, upsets will occur too rapidly and the mitigation will be "overwhelmed."

- In fact, Edmonds approx. equation says –

  There's not really a "cliff."

  The relationships are known; the error rate:

  (1) increases with the square of upset rate

  (2) decreases linearly with faster scrub rates

  (3) is directly proportional to EDAC word size†

† EDAC word size = data bits + check bits ; EDAC=error detection and correction

Basics of Upset Mitigation - Examples

- 32 data bits + 7 check bits -

  Cassini Solid State Recorders with 2+ Gb DRAM array is working well, in spite of architecture “flaw.”

- 128 data bits + 9 check bits –

  This hidden EDAC word inside IBM Luna-C 16Mb DRAMs used on RAD6000 boards on many missions requires external accesses to prevent accumulation of upsets.

- 64 data bits + 16 check bits –

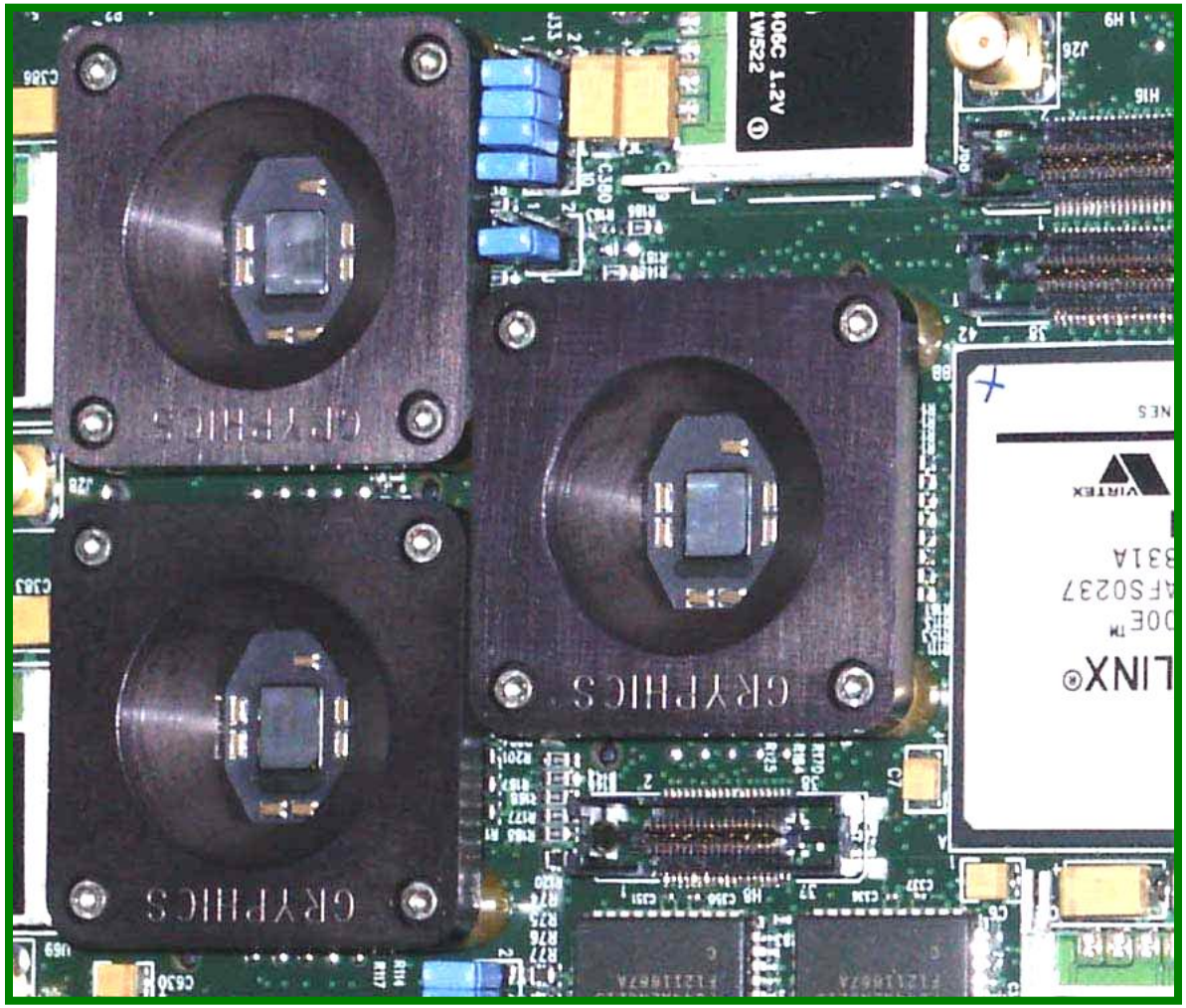
  A specially design cyclical parity scheme on the RAD750 board corrects up to 4 upsets, if confined to a nibble, allowing correct operation with a bad DRAM chip.

If U is the underlying upset rate, then the EDAC word error rate is approximately:

$$0.5 \times \frac{T_{scrub}}{N_{EDAC}} U^2$$

Mitigation – Chip-Level TMR

Maxwell's SCS750 prototype at the Texas A&M Cyclotron Facility:



Upsets by Processor

Run	uP-A	uP-B	uP-C
47.1	67	82	82
47.2	20	20	15
47.3	63	66	62
47.4	22	18	19
47.5	113	157	131
47.6	27	32	23
47.7	45	56	37

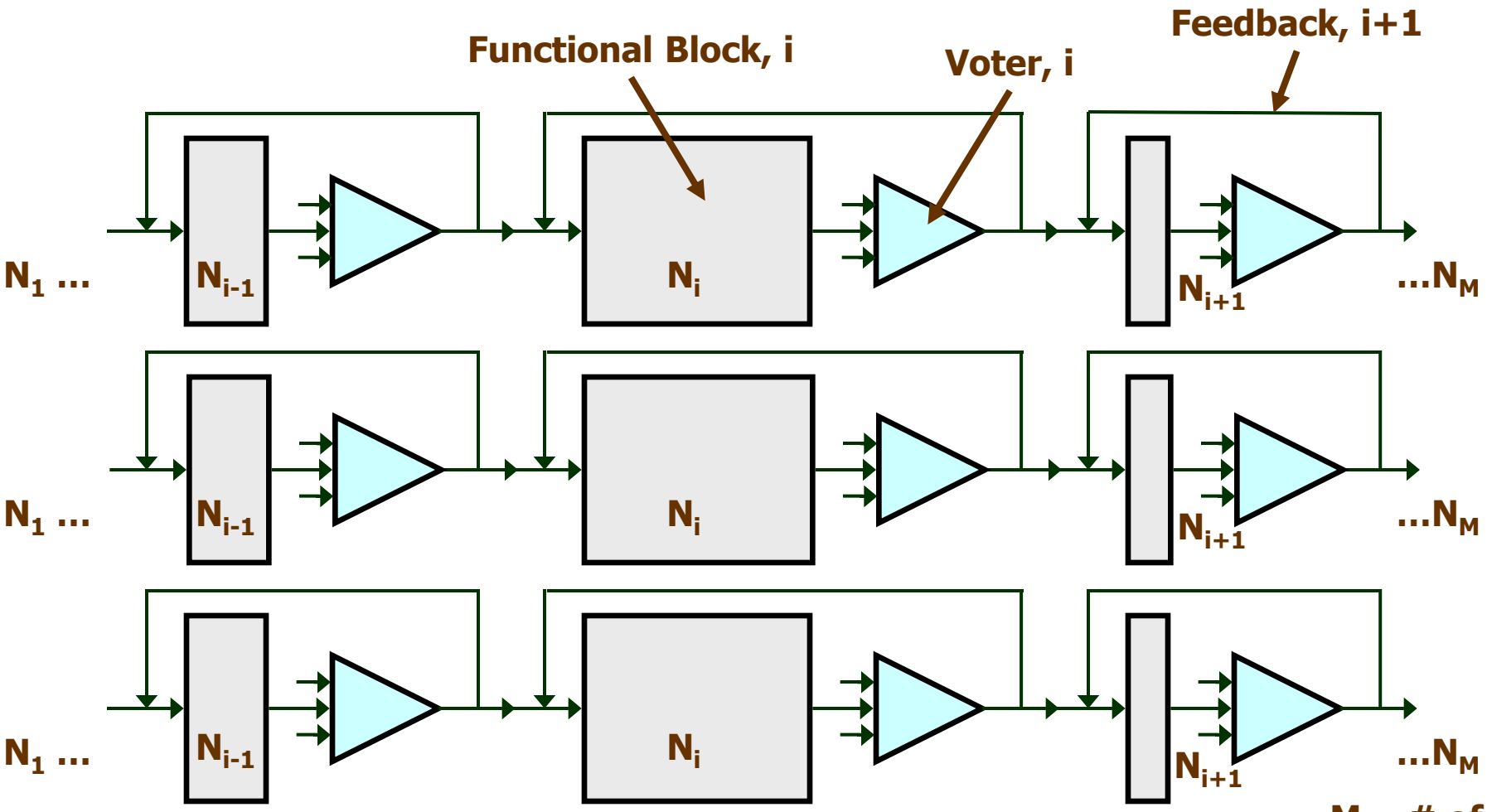
Quite Acceptable Uniformity

TMR Basics

- TMR = triple-module redundancy
  - Three independent “legs” or domains performing identical functions
  - Voters are inserted – typically at feedback points
  - Voters are triplicated also
    - they are *not* a single point of failure

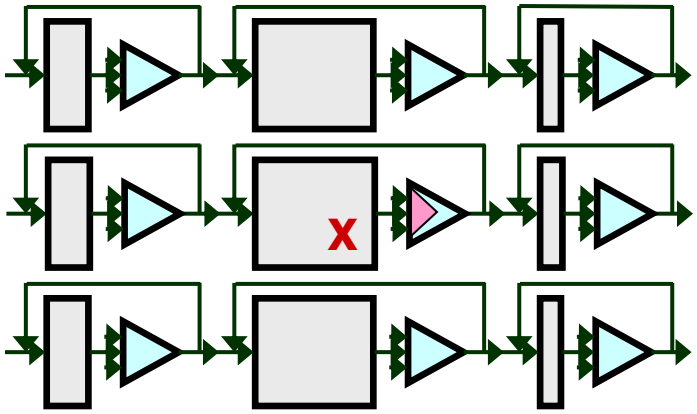
- Error-free operation with any *single* upset
  - Two upsets might cause system failure
  - Scrubbing is again required to reduce the chance of co-resident upsets.

Model of TMR System

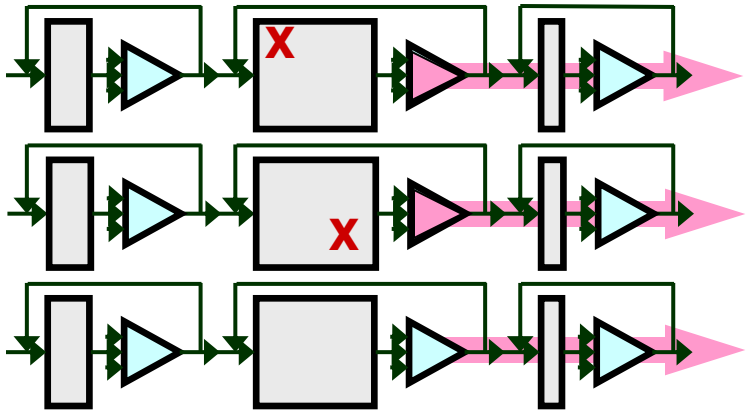


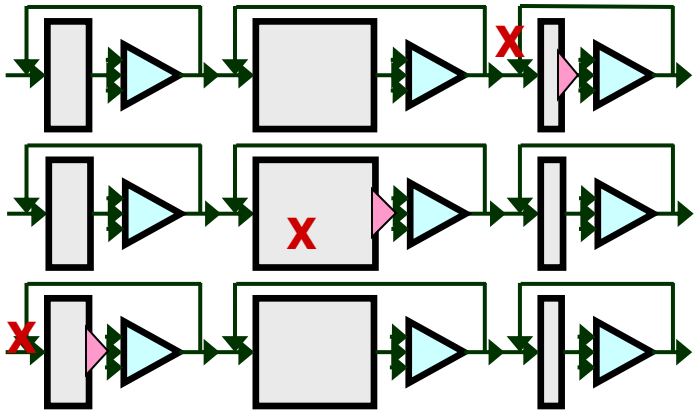
Feedback from the voters corrects state errors inside blocks

TMR stops error propagation



Single upsets cannot cause errors





Even multiple upsets *may* not cause errors

Error propagation requires upsets in two parallel modules.

Edmonds TMR Equation – small r approx.

$$R \approx 3M T_C (\mathcal{M}_2 r)^2$$

- R: System Error Rate
- M: Total Modules
- T_C: Scrub Time
- $\mathcal{M}_2$: "Fitting" Parameter
- r: Underlying Upset Rate

Edmonds TMR Equation – small r approx.

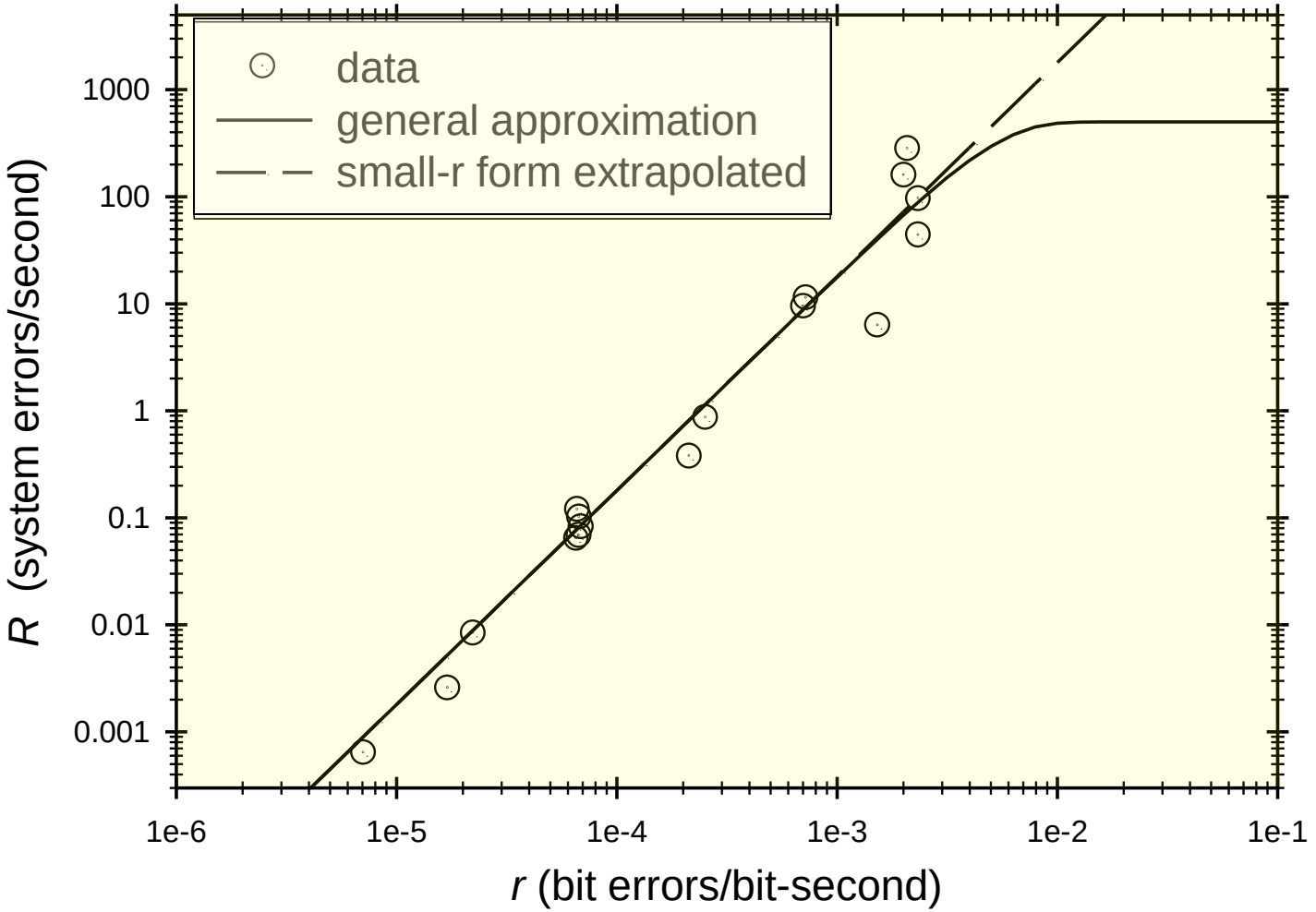
$$R \approx 3M T_C (\mathcal{M}_2 r)^2$$

- R: System Error Rate
- M: Total Modules
- T_C: Scrub Time
- r: Underlying Upset Rate

Parameter is really the second moment of the distribution of N's. This is a "cousin" of the standard deviation.

$$\mathcal{M}_2 \equiv \left[\frac{1}{M} \sum_{i=1}^{M} N_i^2 \right]^{1/2},$$

Example Application - BRAM Scrubber



Given parameters: T=2 ms, M=48000 | **Fit parameter:** M2=M3=M4= 250

In Review …

- New Edmonds Equation for TMR is
  - General (for TMR-ed systems)
  - Powerful
    - Works over many orders-of-magnitude
  - Based on moments which are
    - Statistically meaningful
    - Of rapidly diminishing importance so only one (or two) adjustable parameters are enough
    - Calculable, in theory anyway; in practice, probably not.
  - Useful
    - In predicting system error rates in space
    - In designing appropriate in-beam testing
      - Consortium uses “three-flux” test for all mitigated experiments using spacing of an order of magnitude or more

The End

Thank you!

Any questions?