Scrubbing Approaches for Kintex-7 FPGAs

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Xilinx Kintex7

- Commercially available FPGA
  - 28 nm, low power programmable logic
  - High-speed serial transceivers (MGT)
  - High density (logic and memory)
- Built-In Configuration Scrubbing
  - Support for Configuration Readback and Self-Repair
  - Auto detect and repair single-bit upsets within a frame
  - SEU Mitigation IP for correcting multiple-bit upsets
- Proven mitigation techniques
  - Single-Event Upset Mitigation (SEM) IP
  - Configuration scrubbing
  - Triple Modular Redundancy (TMR)
  - Fault tolerant Serial I/O State machines
  - BRAM ECC Protection
- Demonstrated success with previous FPGA generations in space
  - Virtex, Virtex-II, Virtex-IV, Virtex 5QV

Kintex7 325T

- 407,600 User FFs
- 326,080 logic cells
- 840 DSP Slices
- 445 Block RAM Memory
  - 16.4 Mb
- 16 12.5 Gb/s Transceivers

LAr Upset Rate Estimation

	Timepix	V-4VQ(1)	V-4VQ(2)	Simple
CRAM	1.87×10^{-6}	2.04×10^{-6}	1.82×10^{-6}	1.96×10^{-6}
BRAM	1.67×10^{-6}	1.82×10^{-6}	1.63×10^{-6}	1.75×10^{-6}

($bit^{-1}fb^{-1}$)

[1]obtained by multiplying the measure cross section by the fluence of particles above 20 MeV ($2.84x10^{8}$ $cm^{-2}fb^{-1}$)

- Phase 2 will integrate 2 fb^{-1} in 10 h (5.56E-5 fb^{-1}/s) - 3000 fb^{-1} for the integrated run
  - CRAM: 1.01E-10 upsets/bit/s
  - BRAM: 9.06E-11 BRAM upsets/bit/s
- Estimate accuracy: ± 50%
- Overall upset rate will depend on device
  - Larger devices have more CRAM and BRAM bits

Series 7 FPGA Configuration Data

- Device configuration organized as “Frames”
  - Smallest unit of configuration and readback
    - Individual frames can be configured (partial reconfiguration)
    - Individual frames can be read (readback)
  - 101 words x 32 bits/word = 3232 bits/frame
- Frames organized into different “Blocks”
  - Block 0: Logic/Routing Configuration Data (22546 frames)
  - Block 1: BlockRAM configuration/contents (5774 frames)
- Number of frames in bitstream depends on device size
  - XC7K-325 Device
    - Block 0: 22546 frames (72.9 Mb)
    - Block 1: 5774 frames (18.7 Mb)

Scrubbing Configuration Data

- Frames can be “scrubbed” during device operation
  - Writing individual configuration frames overwrites previous data
    - Replaces “bad” data in the presence of upsets
    - Writes “same” data when no presence of upsets
  - Scrubbing involves continuous reading/writing of configuration data
- Block 0 Frames usual
  - Scrubbed – Contains logic/interconnect configuration
- Block 1 Frames
  - Not scrubbed – data protected with BRAM ECC

Configuration Data Protection

- Each Frame contains SECDED ECC Code
  - Single word of 32 bits (1 of the 101 frame words)
  - Provides single-bit correction and double bit detection
    - Identifies the location of the single-bit upset
    - Identifies presence of double bit upset
    - Double-error detection can be masked with >2 upsets in frame
- Entire bitstream checked with global CRC
  - Detects failure of individual ECC words (masked ECC)
  - Suggests full reconfiguration if global CRC error detected
- Internal FrameECC Block
  - Dedicated block for ECC computation and error correction
  - Computes ECC of last “readback” frame
    - Compares computed ECC with internal frame ECC word
    - Provides status (OK, Single bit error, double bit error)

Internal Scrubber

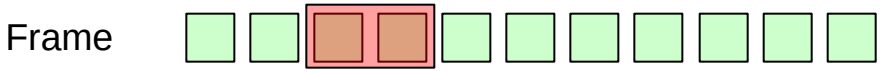
- Series 7 Devices contain internal “scrubber”
  - Continuously reads frames and computes ECC
  - Repairs *single-bit* frame errors
  - Stops on double-bit frame errors
  - Must be enabled with user option (Halt, Correct, Correct and Continue)
- External circuitry must respond to >2 bit frame errors
  - JTAG, SelectMap, ICAP, etc.
  - Requires external configuration memory circuitry

Understanding Multi-Bit Upsets

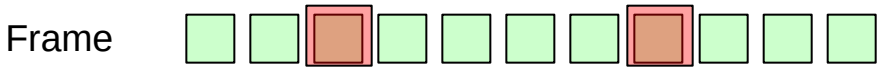
- Analyze frequency of multi-bit upsets within a configuration frame in radiation test data
  - Estimate rate at which *external* scrubbing needed
- Test Procedure
  - Power device and configure with test design
  - Apply predetermined radiation beam fluence
  - Readback device configuration bitstream
  - Compare readback bitstream to golden bitstream
    - Identify differences in Configuration Memory (CRAM)
    - Identify differences in Block Memory (BRAM)
    - Identify differences in user Flip Flops
  - Identify multiple upsets within a frame

Multi-Bit Upset Analysis

- Identify adjacent frame upsets (Intra-Frame Upset)



- Ignore non-adjacent upsets (coincident MBU)



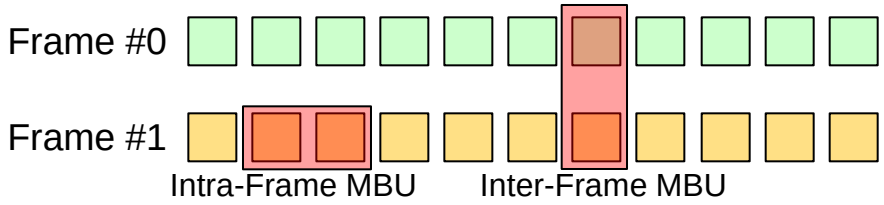
Upsets/event	Frequency
1	90.1%
2	7.5%
3	1.4%
4	.60%
5	.26%
6+	.16%

**results based on 2012 LANSCE neutron test (normal incidence)*

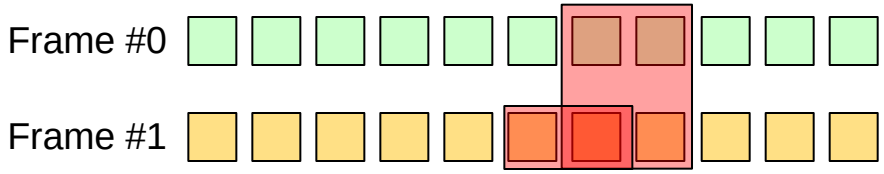
- 90.1% of events result in single-bit frame upset
  - Can be repaired with internal scrubber
- 9.9% of events result in multi-bit frame upset
  - External scrubbing required on 9.9% of events
- *MBU results highly dependent on angle of incidence (results to follow)*

Inter-Frame Upsets

- Configuration bits interleaved with adjacent frames to reduce intra-frame upsets
  - Upsets in same bit of adjacent frame
- Does not affect scrubber
  - Two single-bit upsets in adjacent frames can be repaired



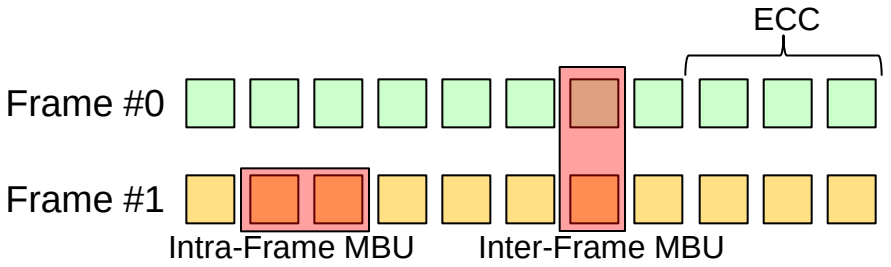
- Larger upset events may occur (Both inter and intra upsets)

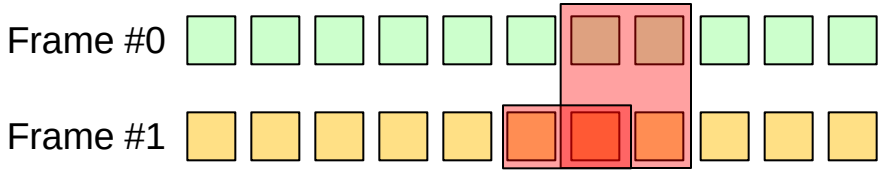


Inter-Frame MBUs

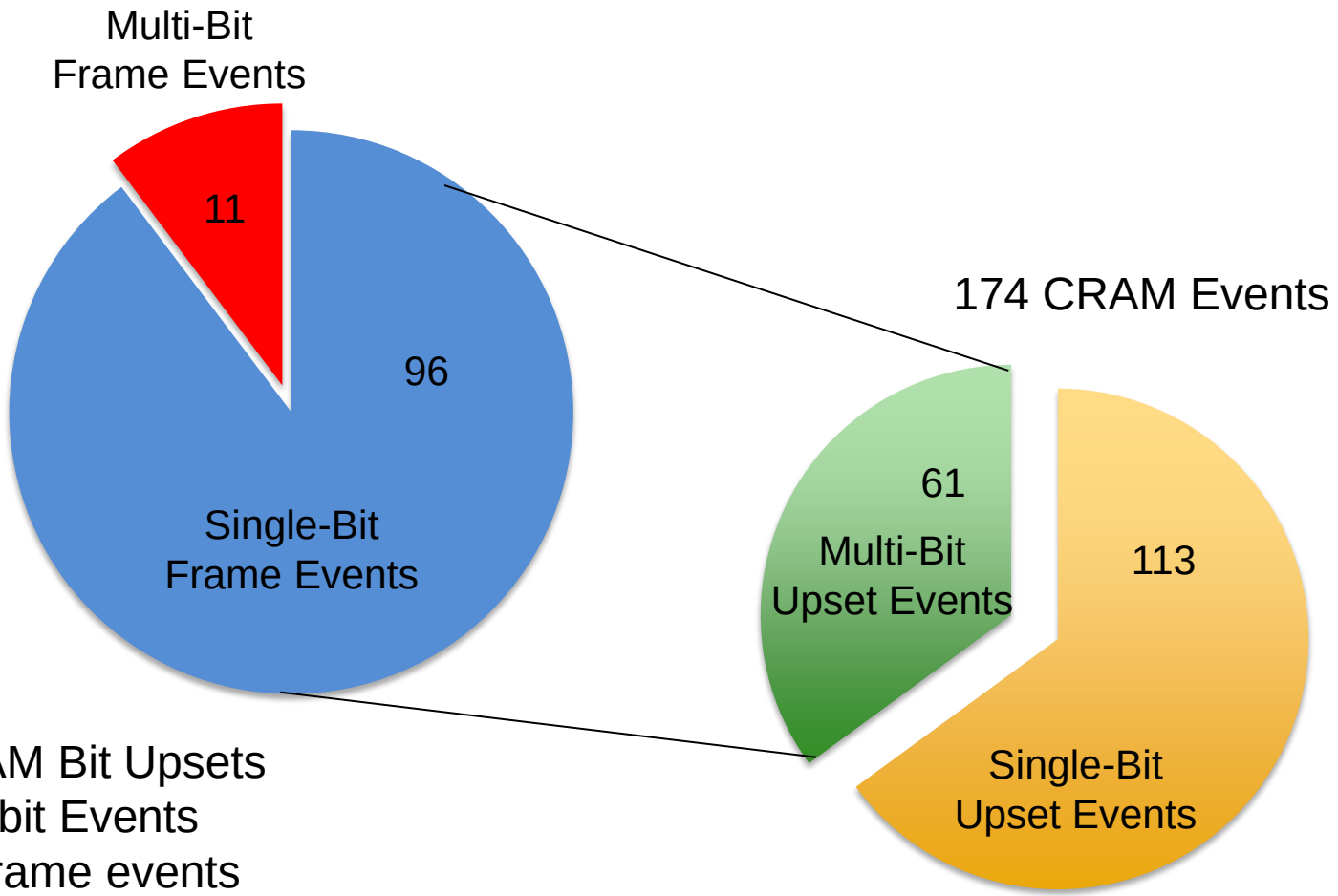
Inter-Frame MBUs

Upsets/event	Frequency
1	65.0%
2	26.8%
3	2.9%
4	3.5%
5	.61%
6+	1.3%





10 Hour CRAM Upset Estimates



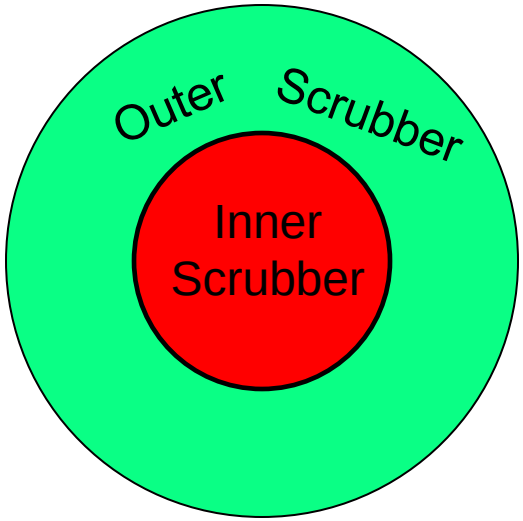
264 Total CRAM Bit Upsets

- 113 Single-bit Events
- 96 Single-frame events
- 11 Multi-frame events (56 bits)

Dual Configuration Scrubbing Approach

- Configuration Scrubbing Constraints
  - Must repair single and multiple-bit upsets quickly
  - Minimize external circuitry (avoid radiation hardened scrubbing HW)
- Multi-level Scrubbing Architecture

Inner Scrubber
- Uses internal Kintex7 Post CRC scrubber
- Scans full bitstream
  - repairs single-bit upsets
  - Detects multi-bit upsets
- Full bitstream CRC check
- *Repair 91% upsets*



Outer Scrubber
- JTAG Configuration Port
- Monitors state of inner scrubber
- Repairs multi-bit upsets
- Logs upset activity
- *Repair 9% upsets (slower)*

Multi-level scrubber currently validated at September, 2013 LANSCE test

JTAG External Scrubber

- SEU Information over JTAG (FPGA->Host)
  - Single event information
    - Specific location of upset (Frame #, Word #, Bit #)
    - Repaired internally with FrameECC
  - Multi-Bit information
    - Double bit upset detection (send Frame #)
    - Global CRC error
- Repair Configuration over JTAG (Host -> FPGA)
  - Single frame configuration (multi-bit upset)
  - Full device configuration (global CRC Error)
- Dual Scrubber tested in radiation beam
  - TSL, Sweden (w/INFN)
  - LANSCE, Los Alamos, CA

Summary

- Extensive testing of Kintex-7 FPGA
  - Static Cross Section Estimations
    - CRAM, BRAM, Flip-Flops
    - Multi-Bit Upsets (MBU)
  - Single-Event Latch up Testing
- Mitigation Strategy Identified
  - Kintex-7 Scrubber developed and validated
  - BL-TMR for logic mitigation
- Future Work
  - Validation of BL-TMR mitigation approach
  - Testing of Multi-GigaBit Transceivers (MGT)