Workshop on FPGAs for High-Energy Physics
- CERN -

Proton irradiation test of an Altera SRAM-based FPGA for the possible usage in the readout electronics of the LHCb experiment

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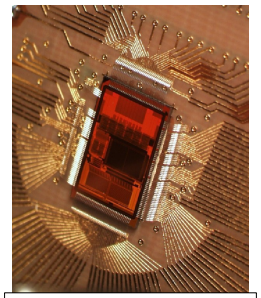
Introduction

- The LHCb upgrade
  - 40MHz readout and flexible software trigger
  - Increase luminosity → 2 x 10^{33}cm^{-2}s^{-1}
  - Current readout chips need upgrade



OTIS chip

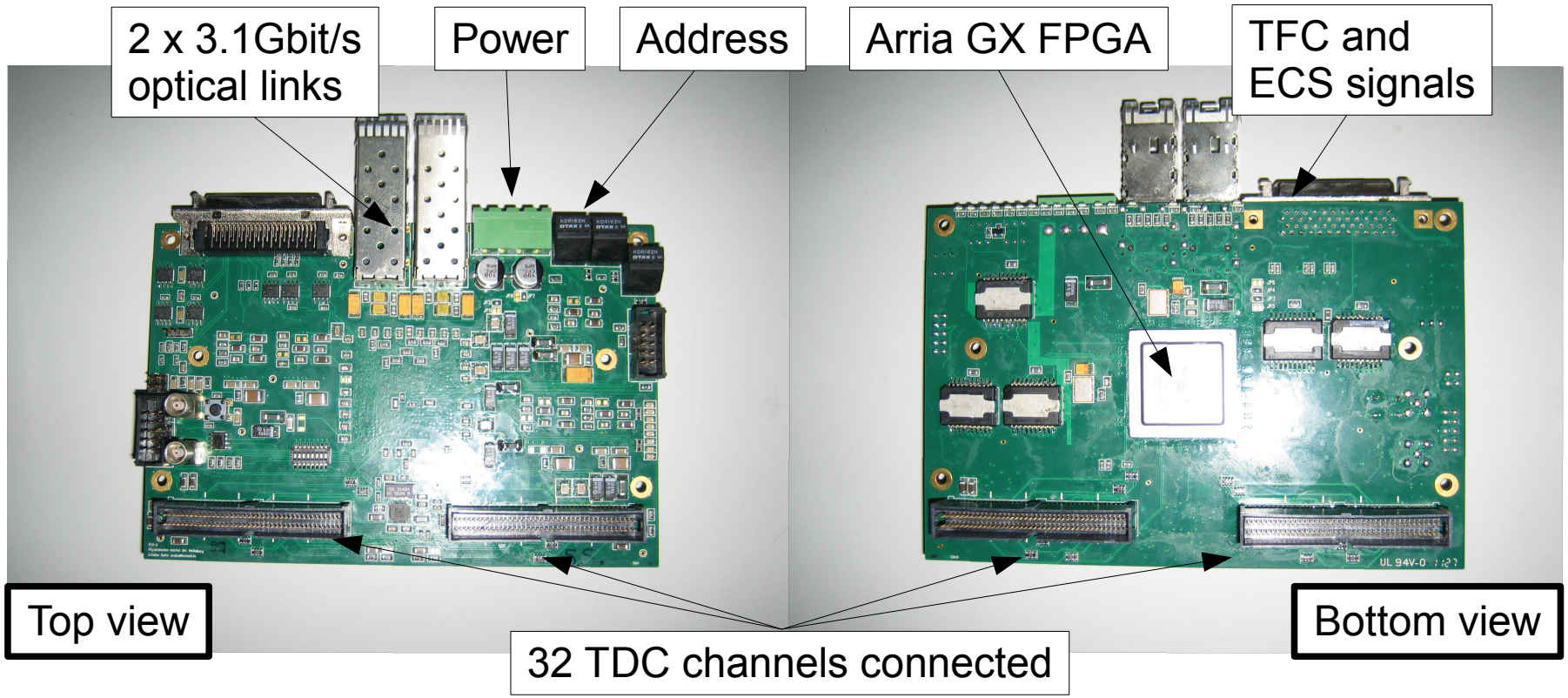
- Possible solution for regions with lower rad. levels:
  - Modern SRAM-based FPGAs with high bandwidth transceivers

Total expected dose for LHCb main tracker area (outer boundary)

	Current situation	Upgrade situation
Total dose	3 krad	29 krad
1MeV neutron	4 x 10^{11}	4 x 10^{12}

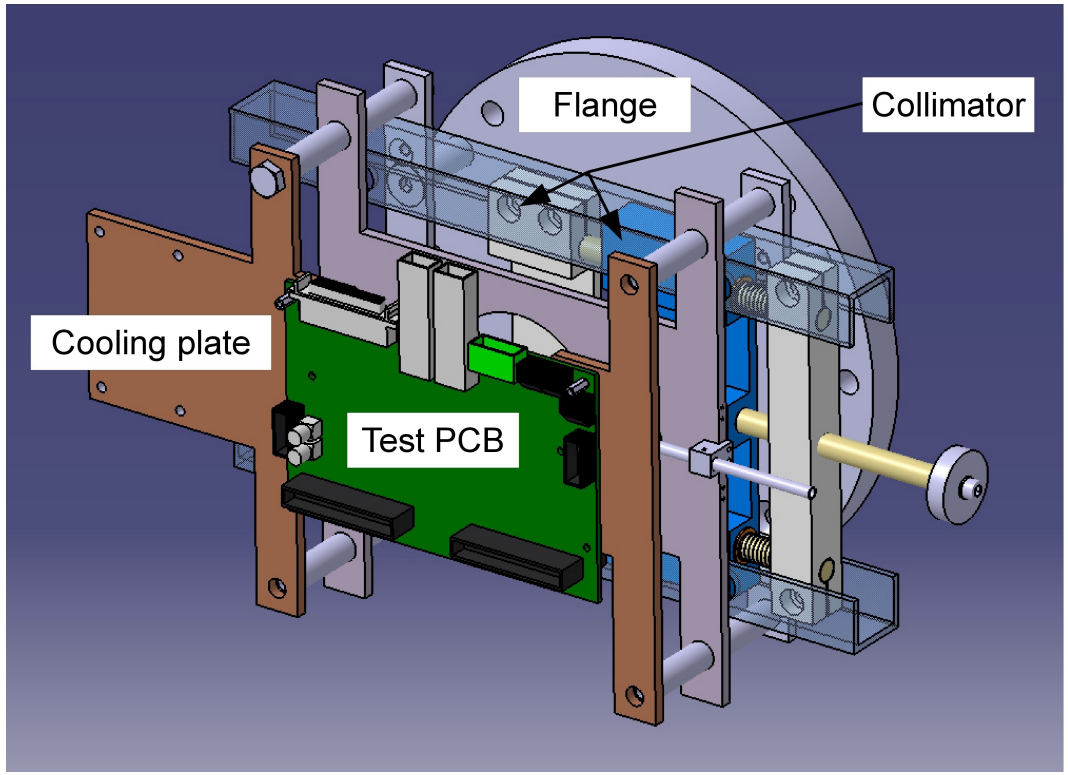
FPGA irradiation test board

- Arria GX – EP1AGX35DF780I6 (90nm)
- FPGA used as TDC and Gbit/s trans. (2 x 3.125GBit/s)
- Test board pin-compatible with existing Front-end electronics of the LHCb Outer Tracker detector



Irradiation Setup

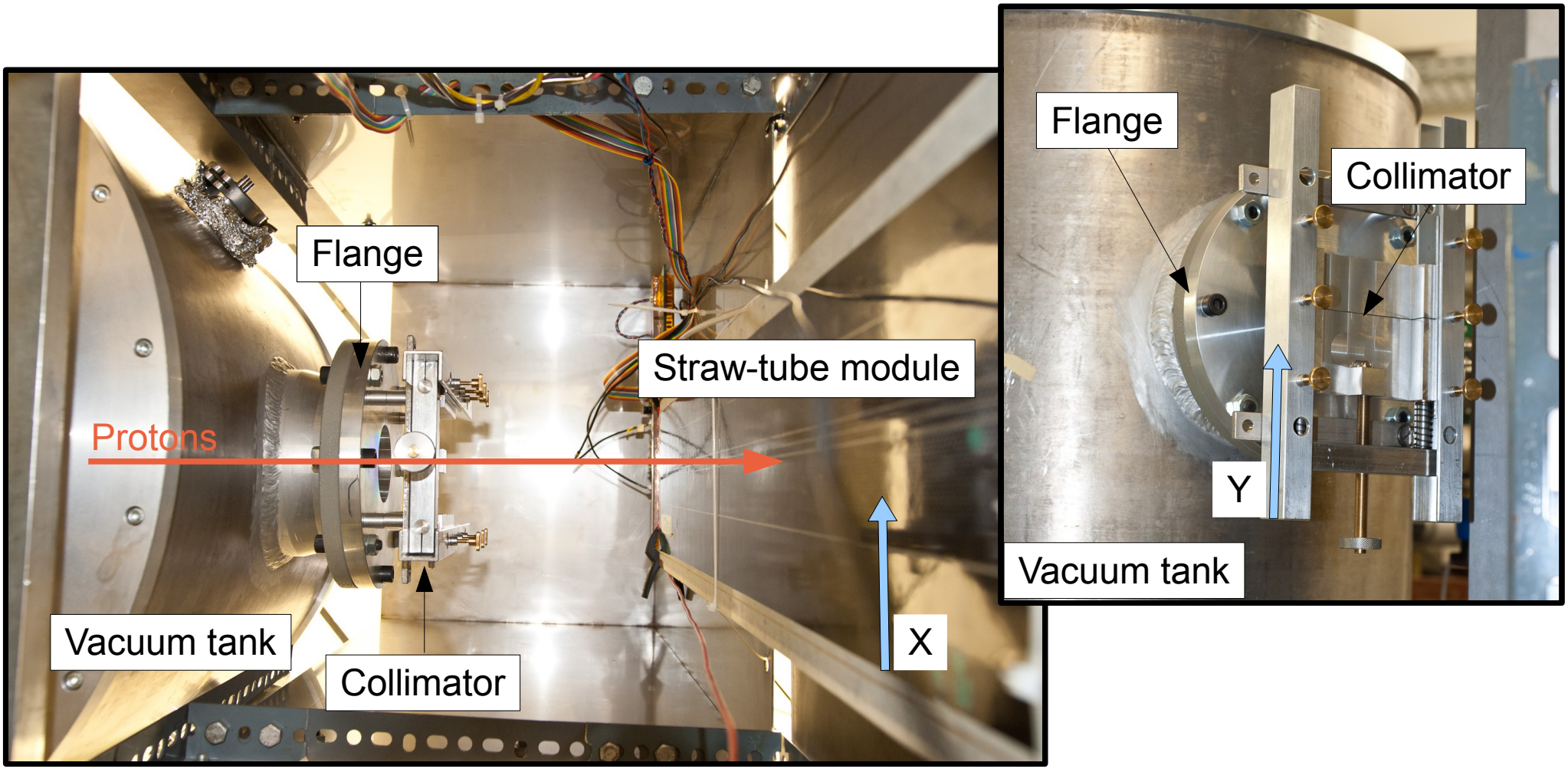
- Two test boards irradiated with **22 MeV protons***
- Each FPGA irradiated in several irr. cycles
  - Proton flux:
    2×10^7 protons*Hz/cm^2 - 6×10^9 protons*Hz/cm^2
  - Dose per irr. cycle:
    4.5 krad(Si) – 5 Mrad(Si)
- TID: up to 7 and 31 Mrad(Si)
- For precise dosimetry to measure beam profile



* Average energy deposit in Si of FPGA: 4.7MeV

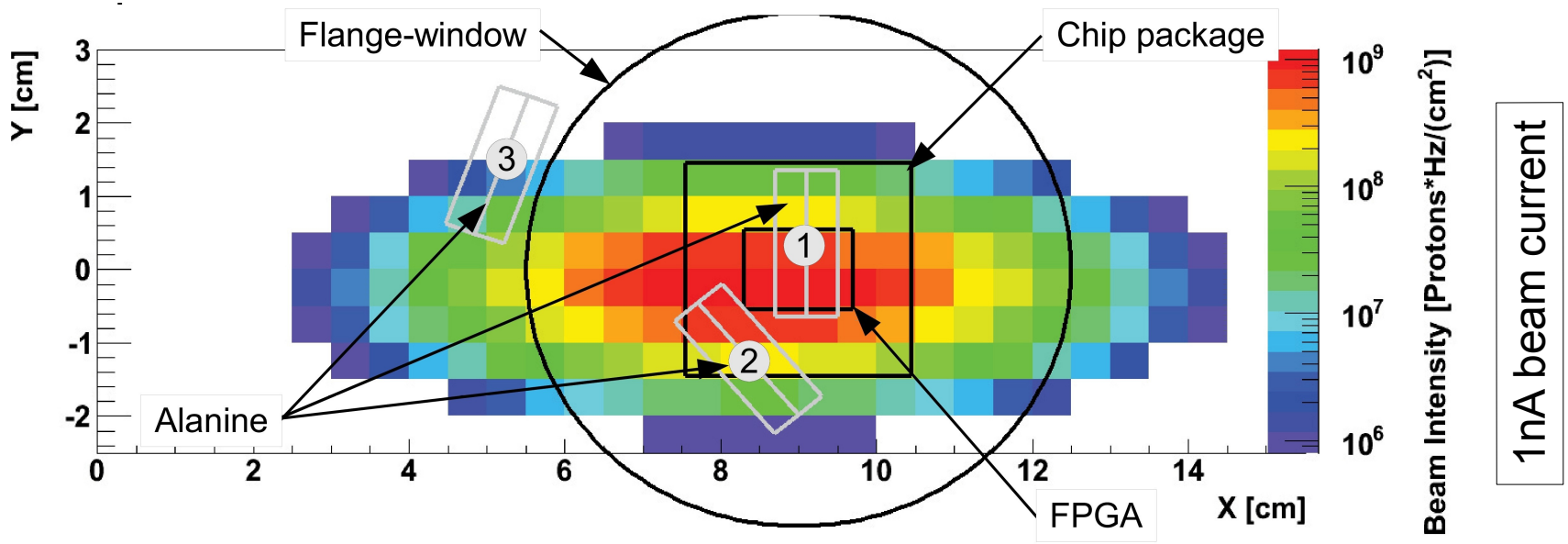
Setup: Beam Profile Measurement

- Used straw-tube module with 1 layer of 32 straws (Ø=0.5cm)
- Perpenticular to the straws used a collimator



Dose determination

- Expected dose from measured beam profile:



- Cross-check with dosimeters:

	Meas. Dose [Mrad]	Calc. Dose Alanine [Mrad]
Position 1	~0 / 0.070	0.06 / 0.06
Position 2	0.15 / 0.25	0.12 / 0.32
Position 3	8.2 / 12.2(max)	7.9 / 14.0

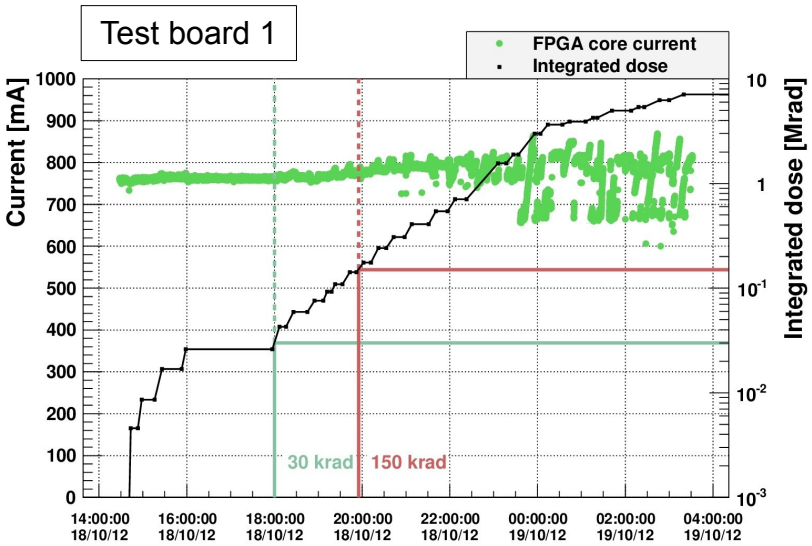
Calc. Dose FPGA:

31.2 Mrad

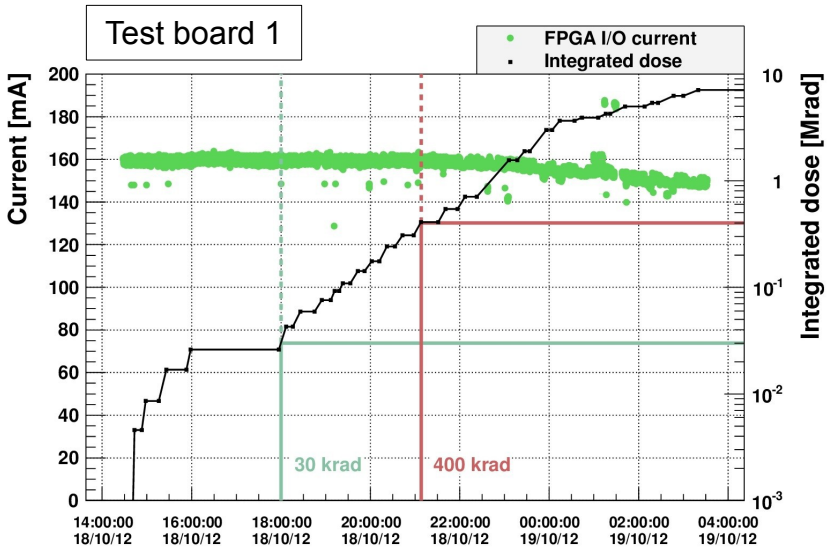
Reasonable agreement between expectations and measurements

FPGA currents

- The electric currents of different voltages of the FPGA were monitored



FPGA Core current rises after 150 krad(Si) and reaches 107% after 7 Mrad(Si).

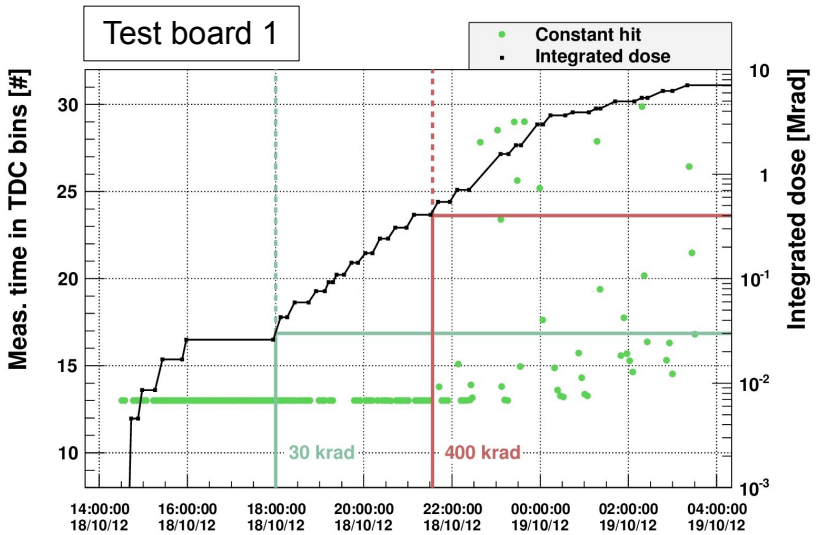


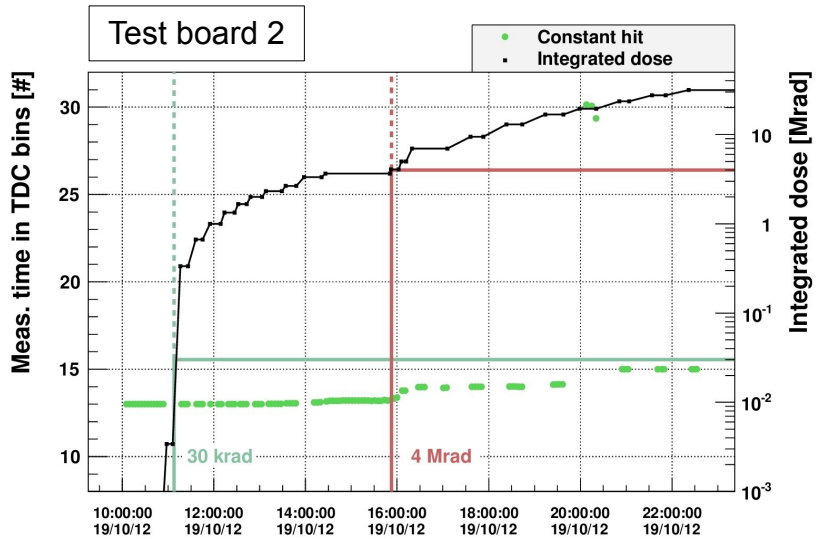
FPGA I/O current starts to drop after 400 krad(Si) and reaches 94% at 7 Mrad(Si).

All permanent current changes are between 5% - 20% and begin after 150 krad(Si).

Stability of Implemented TDC

- 32 channel FPGA-based TDC was tested
  - TDC bin size: 790 ps
  - TDC design uses fast counters + fine timing with phase shifted clocks
- To test TDC: Measure time of constant delayed signal

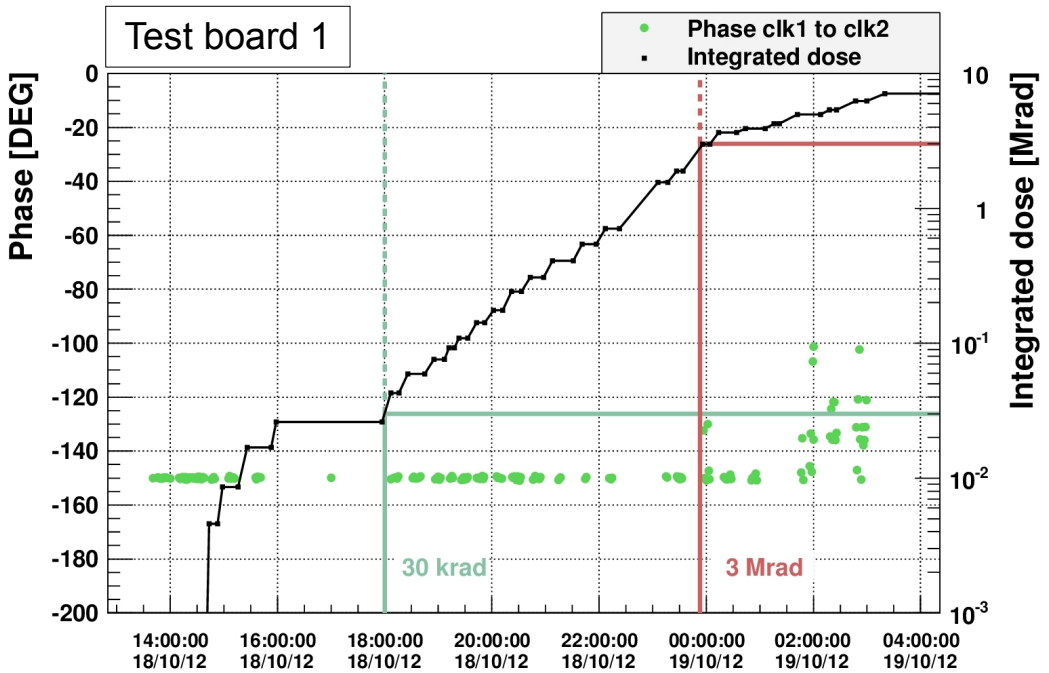




- Wrong time measurement after a TID of 400 krad(Si)
- Shifted time measurement after a TID of 4 Mrad(Si)

PLL stability

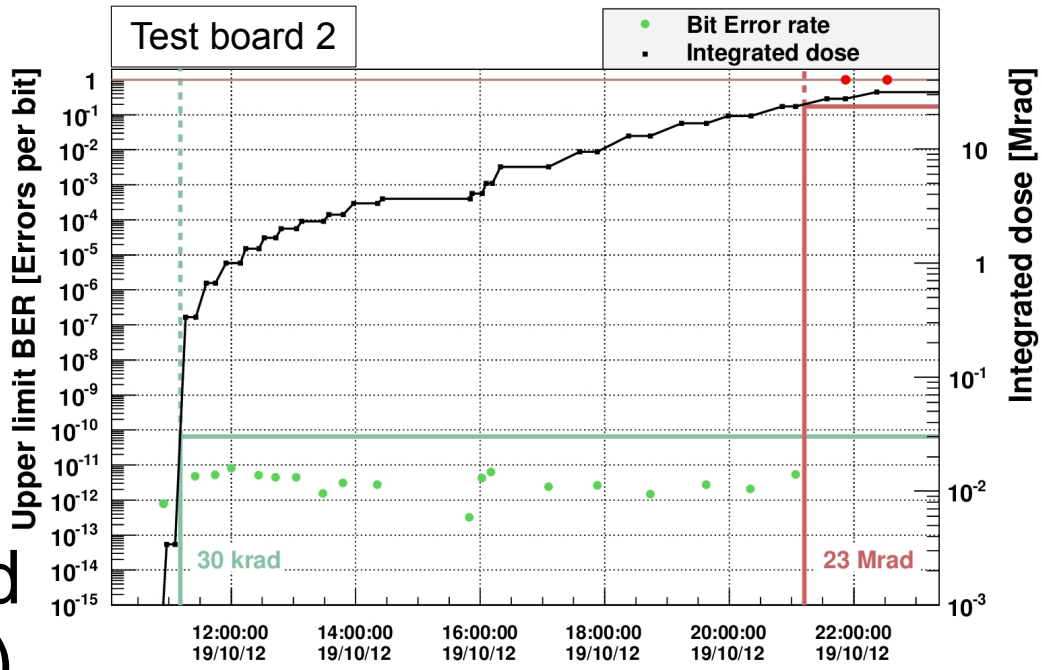
- PLL stability crucial for TDC design
- 3 PLL clock signals monitored with a 1 GHz oscilloscope
- The 3 frequencies did not changed
- The phase between clk1 and clk2 shows a shift from -150° to larger values after 3 Mrad(Si)



FPGA Gbit/s Transceiver Tests 1/2

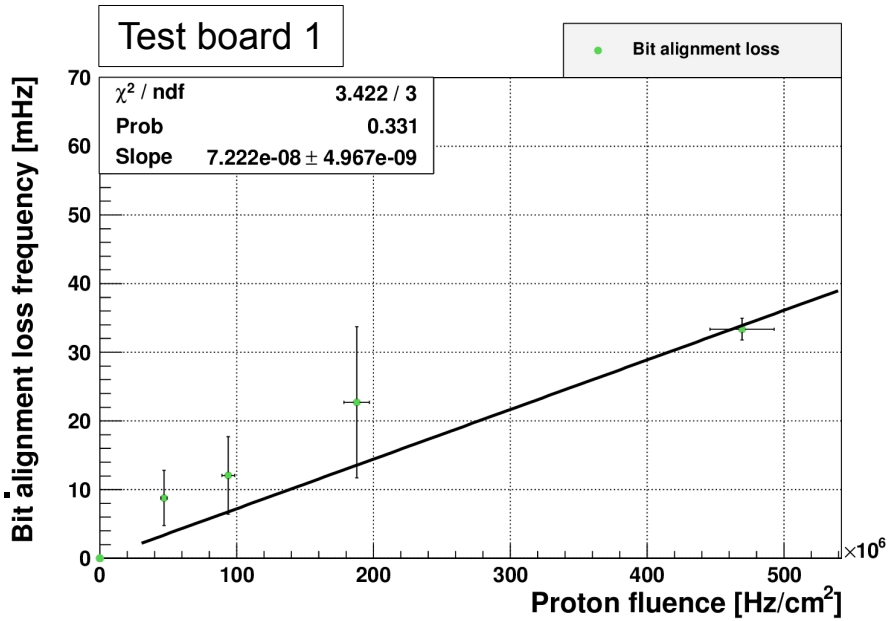
- 1. Gbit link: Loop back → BERT (PRNG data)
- 2. Gbit link: TDC data transmission to a StratixIV FPGA

- Between the irradiation cycles (no irradiation):
  - No bit error found
  - BER upper limit 10^{-12} - 10^{-11} errors per bit due to meas. time
  - Both links stopped after 23Mrad(Si)



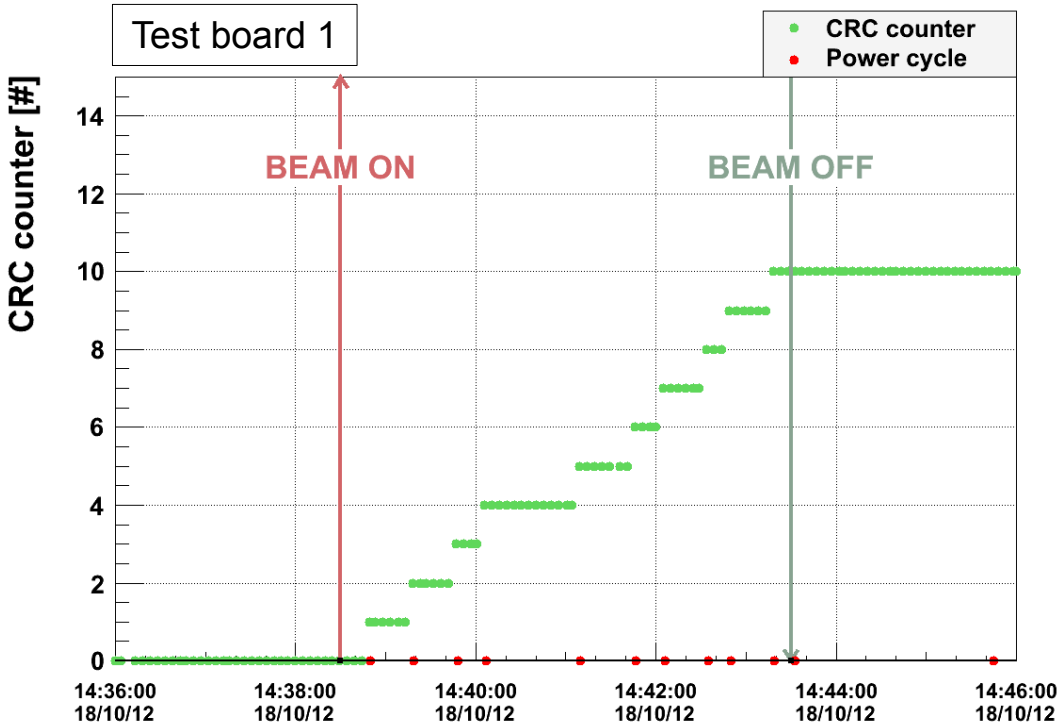
FPGA Gbit/s Transceiver Tests 2/2

- During the irradiation two types of errors found
  1. Loss of bit alignment
     - Recovered by sending next bit alignment word
     - Cross section:
       (1.3±0.5) x10^{-10}cm²/GBit tra.
  2. De-synchronization of transmitter and receiver
     - Needed reprogramming of the FPGA
     - Cross section:
       (8±4) x10^{-11}cm²/GBit transceiver



FPGA configuration registers

- Used cyclic redundancy checker tool from Altera
- For an irradiation intensity 54000 times the expected one, one error every (28 ± 3) seconds was found
- Proton flux:
  2.3 x10^{7} protons*Hz*cm^{-2}
- Cross section:
  (1.6±0.2) x$10^{-9}$$cm^2$/FPGA
- Scale to upgrade:
  Expected CRC every:
  1.5Msec per single FPGA



Summary

- After LHCb upgrade electronics at the outer boundary of the main tracker has to sustain ~30krad(Si).
- 2 Arria GX FPGAs have been tested with 22 MeV protons up to a TID of 7Mrad(Si) and 31Mrad(Si).
- The FPGA sustained the expected TID of 30 krad(Si) without measurable degradation.
- The expected rate of FPGA firmware errors and resets for the Gbit transceivers seem to be manageable for the expected upgrade condition.
- An additional irradiation test with (50-200)MeV protons is foreseen in the near future to verify the SEU results.