FPGAs in the CMS HCAL electronics

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FPGAs in CMS HCAL

We use FPGAs both in the Front-End Electronics (FEE) mounted on the detector and in the Back-End electronics (BEE) located in the counting rooms.

Existing system: produced in 2004 circa.

Upgraded system: in steps between 2014 and 2019.

	Existing	**Upgrade**
Expected TID on FEE	2 Gy	14 Gy (1.4 krad)
Expected 1 MeV-equivalent neutron fluence on FEE	1×10^{11} / cm^2	7×10^{11} / cm^2
Front-End	Actel antifuse (for control only)	Microesemi flash-based (control and data)
Back-End	Xilinx and Altera	Xilinx
Number of FPGA types	2 (FEE) + ~8 (BEE)	~5 (FEE) + 5 (BEE)
Number of developers	1 (FEE) + ~4 (BEE)	~6 (FEE) + 4 (BEE)

FPGAs in the FEE

Existing system: Actel antifuse with hand-made TMR

- no radiation effects observed
- problems for lack of reprogrammability

Upgrade: we are considering Microsemi Flash-based FPGAs. Major advantage is that the configuration is SEU-immune.

1) ProASIC3L:

- logic, PLL, RAM, ROM, etc
- Fmax ~300MHz
- no serdes

2) igloo2 : has also 5 Gbps serdes

Grade of the FPGAs

Microsemi sells non rad-tol FPGAs and Rad-Tol FPGAs.

We have heard that:

- they are manufactured in the same factories
- the Rad-Tol production lots are tested for radiation.

We buy non rad-tol FPGAs and hope for the best…

Tests on Microsemi ProASIC3L

There are good publications. The most complete is:

- C. Poivey et al, “Radiation Characterization of Microsemi ProASIC3 Flash FPGA Family”, proceedings of IEEE Radiation Effects Data Workshop (REDW 2011)

→ no SEL, no SEU on configuration, calculation of various cross-sections, timing degradation starts at 200 Gy, failure around 500 Gy…

In one scenario we want to interface the ProASIC3L to the Cern GBTX → need the ability to receive SLVS (a differential signal similar to LVDS but with smaller amplitude).

SLVS inputs are not in the FPGA specs, and obviously were not tested under radiation.

We have shown that ProASIC3L can receive SLVS, and this is true also under radiation. Publication:

- A Belloni et al, “Radiation tolerance of an SLVS receiver based on commercial components”, Journal of Instrumentation (JINST 2014)

Tests on Microsemi igloo2

On-going tests by Univ. of Minnosota with 230 MeV protons:

- failure after 2×10^{12} protons (~ 1000 Gy);
- no SEU seen on a TMR-type shift-register
- no SET seen;
- PLL : observed 400 SEUs over a fluence of 10^{11} protons/cm^2 (or maybe 2×10^{12}…)

→ cross section < 400/ 10^{11} p/cm^2 = 4×10^{-9} cm^2

The PLL always re-locked within 34 us.

Results are satisfactory for our application.

We plan to test also the embedded 5Gbps serdes.

Use of igloo2

We are going to test the igloo2 serdes for data readout from the FEE, and for the control of the FEE.

Major issue: how to drive the reference clock ?

Two options:

1) synchronous with the accelerator: need a rad-tol jitter cleaner
2) from a local oscillator: need for padding logic

Reprogramming the Microsemi flash-based FPGAs

Advantage: reprogramming the FPGA after a certain TID will improve the timing characteristics.

Disadvantage: reprogramming during an irradiation has a small chance to burn the FPGA (SEGR). This is related to the charge-pump voltage converter used to increase the voltage internally.

→ Obvious solution in HEP experiments: reprogram only when there is no beam

Mitigation techniques

- TMR inside the FPGA (preferably automatic, see next slides)
- Could also triplicate the most critical IOs
- Redundancy at the system level

Organization of our FPGA designs

- mostly in verilog
- version number on each FPGA
- Compilation often based on the vendor GUI, in a few cases it is entirely script-based
- store on the CMS SVN server all source files, constraint files and the files needed to reproduce the compilation (project file or scripts).

→ This organization allows easier:

- re-use
- cross-check
- partitioning of a design between different developers

Export limitations from U.S.A. [“ITAR”]

The following items are designated as defense articles:

microelectronic circuits that meet or exceed the following characteristics:

1. total dose of 5×10^{5} Rads (Si);
2. dose rate upset threshold of 5×10^{8} Rads (Si)/sec;
3. neutron dose of 1×10^{14} n/cm2 (1 MeV equivalent);
4. single event upset rate of 1×10^{-10} errors/bit-day or less, for the CREME96 geosynchronous orbit, Solar Minimum Environment;
5. Single event latch-up free and having a dose rate latch-up threshold of 5×10^{8} Rads(Si).

Consequences (1)

- CERN used to have a license for a synthesizer that can do automatic TMR (Precision Hi-Rel from Mentor Graphics)

- The license has been cancelled as a consequence of ITAR

- CERN still has license for Synplify Premium which can also do some TMR although less effective [see https://indico.cern.ch/event/164326/material/slides/3?contribId=7]

Consequences (2)

If we publish results of radiation tests on a commercial device and the results meet the ITAR characteristics, we may no longer be able to buy that device ☹

We have a list of FPGA irradiation results accessible only by CERN members:

https://twiki.cern.ch/twiki/bin/view/FPGARadTol/InformationOfInterest

If you need other commercial components to put in your PCB, a similar list exists:

https://twiki.cern.ch/twiki/bin/viewauth/Main/TulliosPreferredPartList