FPGA For High Energy Physics Workshop—LHCb Inputs

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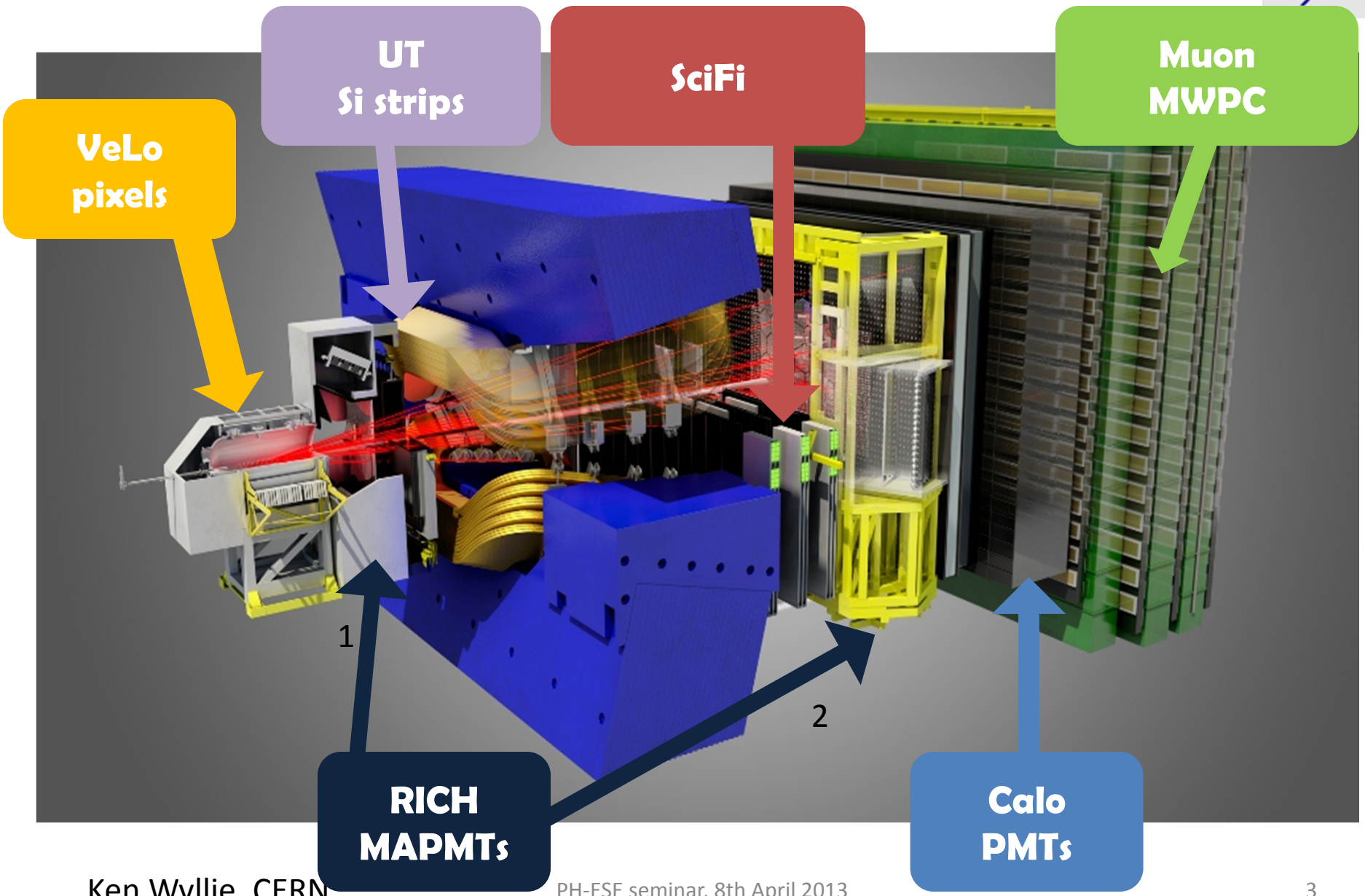
This slide package contains materials from Ken Wyllie, Steve Wotton, Tomasz Skwarnicki, Antonio Pellegrino, and Wilco Vink.

Topics

- First … some context
  - Overall LHCb Detector Snapshot
  - CERN IP Blocks and generic LHCb detector architecture
- General FPGA considerations
- Some specific detector examples: RICH, SciFi, and UT
  - Key FPGA-relevant requirements and considerations
  - Specific options in consideration
  - Status
- Rad-Tolerant FPGA path finding options

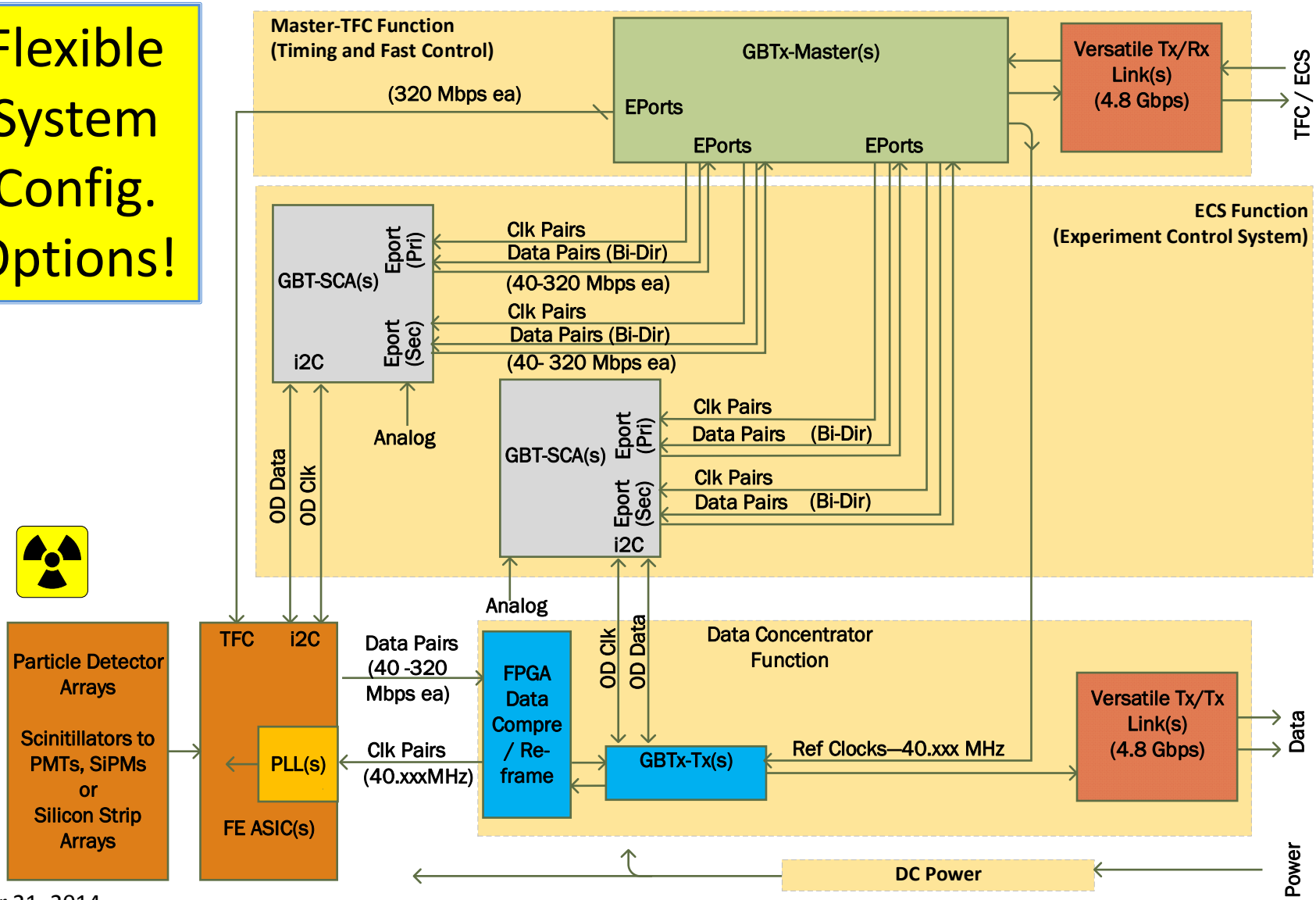
I'm the facilitator, so dialog is encouraged and welcomed!

LHCb Future


UT
Si strips
SciFi
Muon
MWPC
VeLo
pixels
1
2
RICH
MAPMTs
Calo
PMTs

Generic LHCb Detector Architecture

Flexible System Config. Options!



CERN Developed IP Blocks

- Communications IP tailored for deployment in the cavern radiation environments
  - 130 nm CMOS proven for >> 300 Krad TID
- Three primary components address remote control interfaces as well as high-speed optical SERDES data transfer
  - GBTx
    - Bi-directional SERDES at 5 Gbps interface with the counting room
    - Multiple channel elink ports for interface with detectors
      - 40 → 320 Mbps data rates
    - Built-in Clock recovery and jitter cleaner via on-board crystal osc.
      - 40.xxx MHz reference clock extraction, phase adjustment, and distribution
  - Versatile Tx/Rx Link
    - Optical layer linking front-end to back-end up to 300 m distant
    - Pluggable module (similar to SFP+)
    - Bi-directional @ 5 Gbps
  - GBT-SCA
    - Control via elinks
    - Multiple interface options: JTAG, i2C, parallel, memory bus, analog mux + ADC

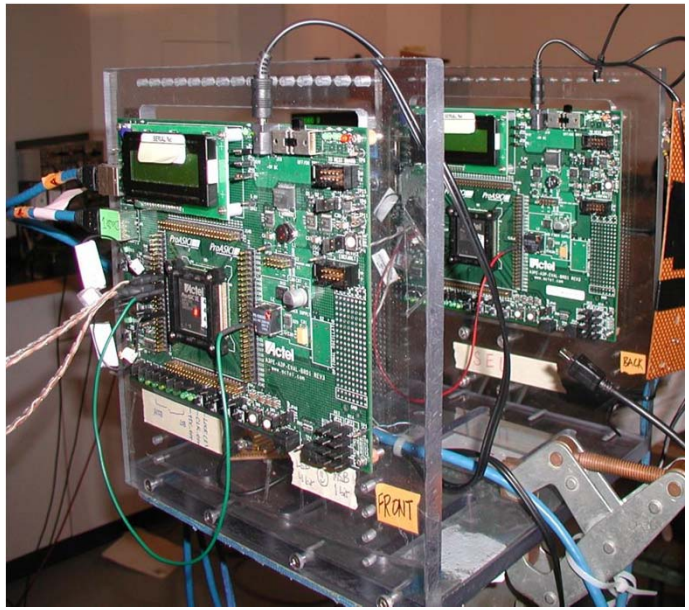
FPGAs in front-end

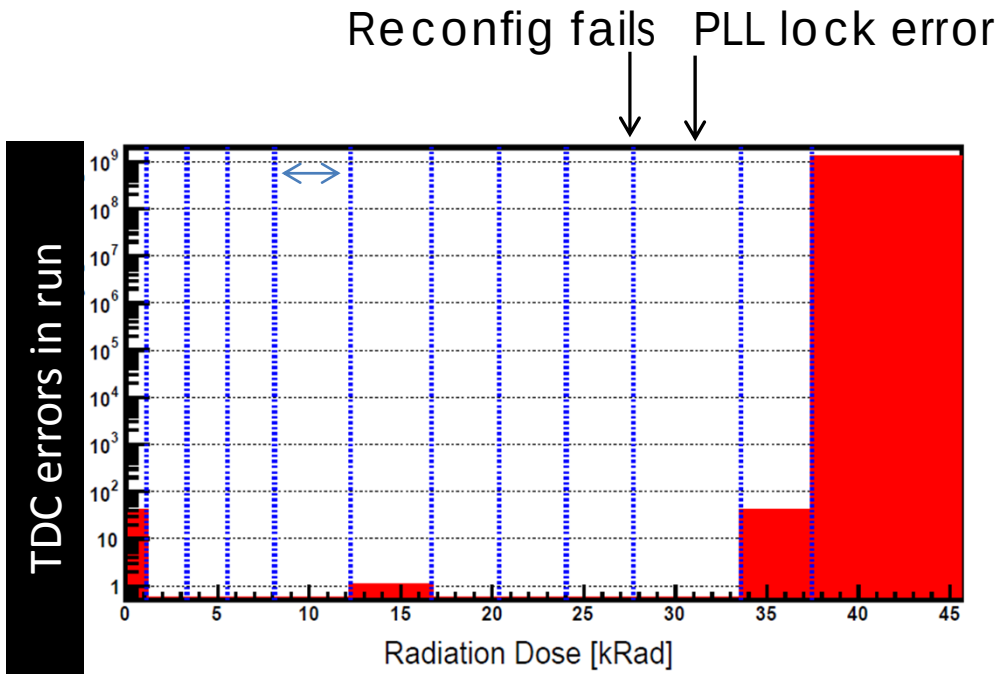
Big advantage: re-programmability
=> tune algorithms
=> scale system

Example Microsemi ProASIC3 irradiation tests from SciFi early R&D efforts

Good past experience with flash FPGAs (ACTEL/MICROSEMI)

Irradiation program with full TDC[1] code, 320MHz from internal PLL





[1] SciFi early R&D outer tracker option, but since eliminated.

FPGA Options Summary

	TID limit	Configuration Tolerant to SEUs	SEUs in functional blocks	Notes
MicroSemi ProAsic Flash	20-40 krad (very dependent on dose rate & refresh conditions/annealing)	Yes	Use TMR, embedded blocks should be tests (eg PLLs)	Already tested
MicroSemi SmartFusion2 Flash	?	Yes	Use TMR, embedded blocks should be tested (eg PLLs)	Very new and not tested much
AntiFuse	? (but higher than Flash. PINT was tested good to 150 krad)	Yes	Use TMR, embedded blocks should be tested (eg PLLs)	One shot only!
SRAM FPGA	100s krad	No: needs scrubbing	Use TMR, embedded blocks should be tested (eg PLLs)	Needs careful testing & scrubbing implementation

Some General FPGA Considerations

- Need reprogrammable option
  - Supports dynamic requirements development
  - Addresses system complexity risks
- Power
  - Voltage rails
    - Sub 1.2V rails are below on-board reference for some LDO linear regulator rad-hard options
  - Total consumption—especially relevant for many 100's of FPGAs
- Overall product lifetime
  - Desired product life > 10 years
- On-board SERDES, while attractive, is not without potential performance burdens
  - FPGA-based PLL clock recovery typically not crystal-based which results in higher inherent jitter clock outputs
  - SEU performance of PLL and SERDES blocks needs careful test evaluation
    - Overall TID and SEU capability
    - Bit error rates

Some General FPGA Considerations-Cont'd

- SRAM-based FPGAs can be more prone to configuration memory upsets
  - Scrubbing is used in ALICE (local flash device stores reference)
  - Some new FPGAs have automatic procedure for correction
    - Kintex7, with external flash
  - Scrubbing has to be tested against expected SEU rate
- Vendors sell 'rad-tol' FPGAs, but they are expensive
  - 'rad-tol' = sample-tested, costly MIL grade package
  - Commercial equivalent chip is often not the same as rad-tol
- Need to define robust methods to program the FPGAs in situ using the CERN IP communications blocks
- Need suitable rad-tolerant flash memory solution for SRAM-based options

RICH: Key Requirements and Status Summary

- Key FPGA Functionality: Processes 64-channel Multi-Anode PMT outputs
  - Latch results, zero suppress, format GBTX frames, housekeeping/configuration
- Radiation Environment: 23 Krad/year x 10 years
- Some Key Considerations:
  - Need reprogrammable option to support dynamic requirements development
  - Costs (eg Spartan-6 adequate for performance)
    - 2,000 smaller + 400 larger FPGAs, but dependent upon selected device density
  - Power conversion voltage rails and total power
  - Good product lifetime
- Practical options: SRAM-based FPGAs
- Status: Evaluating device options

SciFi (Scintillating Fibers): Key Requirements and Status Summary

- Key FPGA Functions: Processes data from PACIFIC ASICs
  - TDC, zero suppress, data compression, format GBTX frames, housekeeping/configuration
- Radiation Environment: 30 Krad total over 10 years
- Some Key Considerations:
  - Need reprogrammable option to support dynamic requirements development
  - Data compression algorithm needs lots of logic resources
    - Microsemi SF2/IG2 attractive option for resources + internal SERDES, but greater resources available in SRAM-based FPGAs has some potential advantage
  - Good product lifetime
  - Total 5,760 Microsemi IG2/SF2 FPGAs estimated
- Practical options: Microsemi SF2
- Status: Evaluating specific device options

UT(Upstream Tracker): Key Requirements and Status Summary

- Key Functionality: Collects silicon strip detector data via 4,192 custom FE ASICs
  - Data concentrator design trade in-work
    - Use FPGAs to re-pack data (reduces # optical channels) versus parse data in counting room
    - Additional constraint is routing >12,000 SLVS data line pairs operating at 320 Mbps to more distant locations to lower the radiation exposure
  - Separate FPGAs planned for housekeeping/configuration/local failsafes
- Radiation environment design trades in-work
  - Desire < 30 Krad total over 10 years, but requires finding available volumes >1.5-2.0 meters distant from the beam pipe
  - Volumes adjacent to detector planes require 200- 300 Krad TID over 10 years
- Some key considerations:
  - Need reprogrammable option to support dynamic requirements development
  - Generally need lots of combinatorial logic and memory resources for data repack
  - High performance, noise tolerant SLVS compatible differential receivers
  - Good product lifetime
- Practical options: ProASIC3, IG2/SF2, SRAM-based FPGAs
- Status: Evaluating electronics location and interconnect options

UT Dose Curves

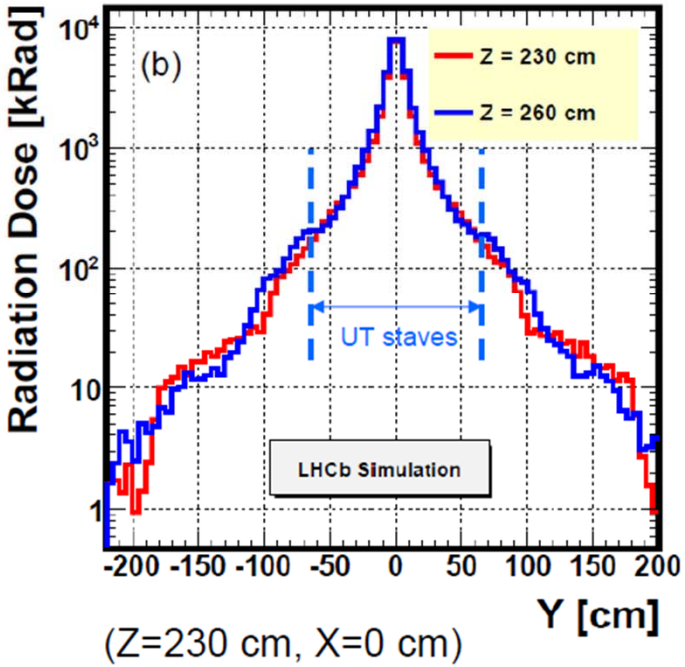
Expected total dose

TDR: These studies imply that all the components in the region near the beam pipe need to be irradiated up to 40 MRad to validate their ability to sustain performance; this includes a safety factor of four. In addition, the electronics located near the detector box needs to be checked with a radiation level of the order of 100 kRad.

Simulations by Matthias Karacson (50 fb^{-1}): Jan 20, 2014 Talk
https://indico.cern.ch/event/292452/contribution/5/material/slides/0.pdf
Warning: plots have finite bin size effects that require corrections for the innermost parts and no safety factors

Note: Still Need Radiation Design Factor Applied!

10 MRad
1 MRad
100 kRad



(Z=230 cm, X=0 cm)

40 MRad for the innermost sensor
(3.3 cm from the beam) includes a factor of 2 safety in normalization of simulations.

Another factor of 2 was a correction for the finite binning.

SALT chips
5cm to the beam: **30 MRad**

FPGA Irradiation Test Path Finding Summary

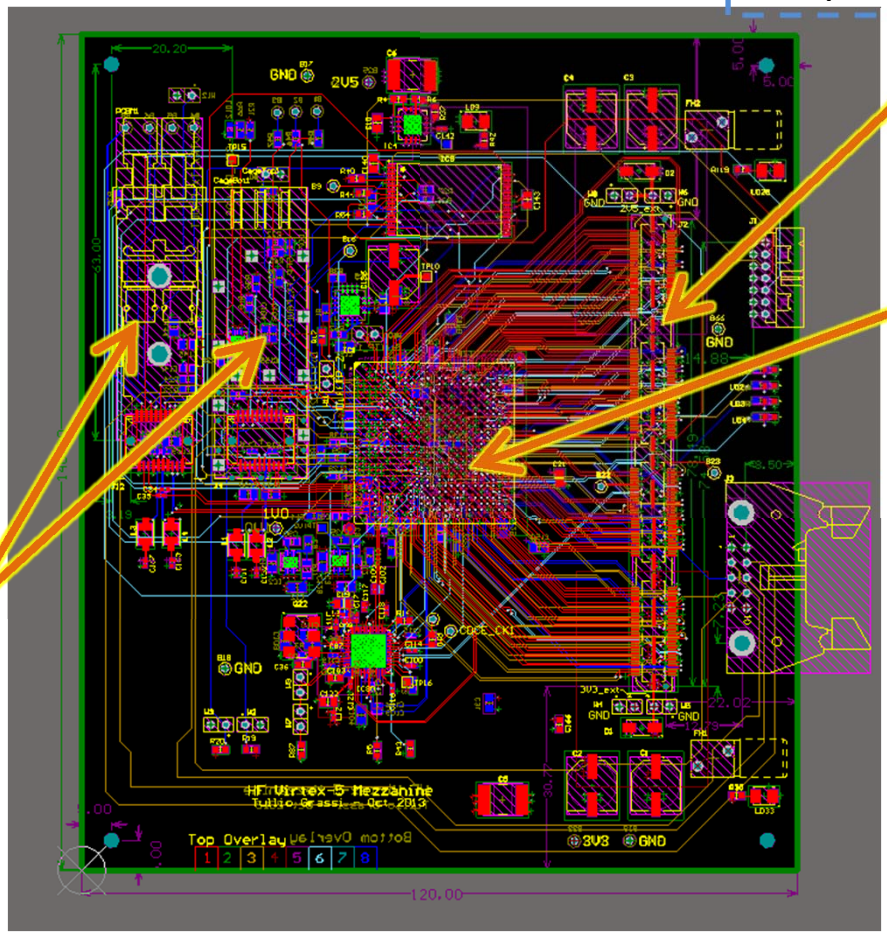
- Microsemi has promised results on IG2/SF2
  - Product updates and tests on-going
  - May be OK for < 100KRad?
  - SERDES and PLL SEU and TID performance needs confirmation
- Xilinx Virtex 5 is a desirable and proven solution, but space grade option too costly
- UT to build FPGA radiation test path finder for tests in CY2014 if dictated by design trade results
  - Still working to complete trade study that will drive final requirements
  - < 30 KRad solution could include either Microsemi ProASIC3 or IG2/SF2 options
  - 200 - 300 KRad most likely option is SRAM-based such as Kintex7
- CMS designing Igloo2-based rad-tolerant mezzanine card
- SciFi not planning specific FPGA irradiation tests, but willing to collaborate
- RICH groups still working test and validation plans, but baseline solution is SRAM-based FPGAs

Backup

CMS Igloo2 FPGA Mezzanine In-Work

Planned Igloo2-based Rad-Tolerant FPGA Mezzanine card for CMS ngCCM is potential option for LHCb

Mezzanine Card Connector: Supports I/O Expansion (80 diff pairs)



Soon-to-be Igloo2 FGPA with built-in SERDES

SERDES SFP+ Sockets: Can accommodate commercial or Versatile components

Board Outline: 120 x 140 mm