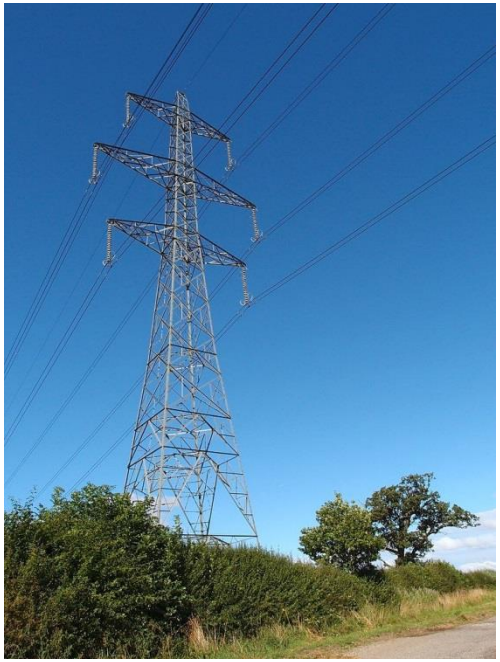


Powering Schemes

for vertexing and tracking detectors

Peter W Phillips

STFC Rutherford Appleton Laboratory

VERTEX 2014, Macha Lake, 15-19 September 2014

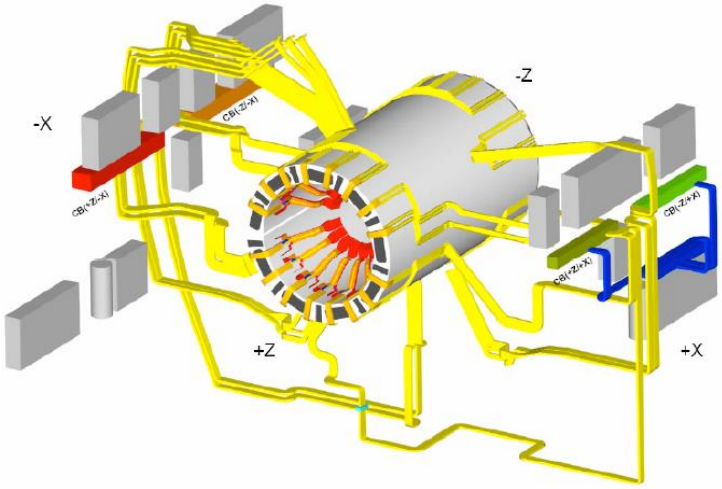
Outline

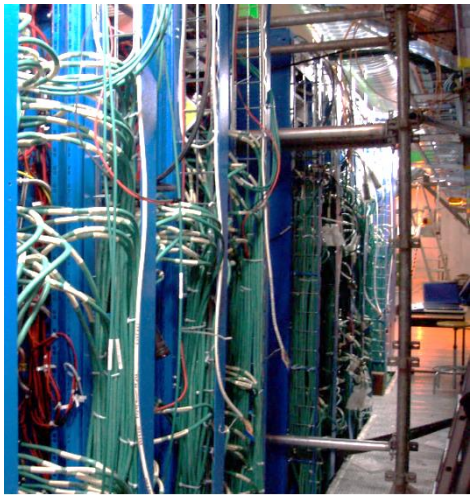
- Motivations for Change
- Serial Powering
- DC-DC Point of Load Converters
  - Buck Converter
  - Packaging Options
  - Switched Capacitor
- Power Pulsing
- HV Multiplexing
- Conclusions

Example: ATLAS SCT (Silicon Strips)

- 4088 Detector Modules
- **Independent Powering**
  - 4088 cable chains
  - 22 PS racks *in service caverns*
  - 4 crates / rack
  - (up to) 48 LV and 48 HV channels / crate
- Longest cable run
  - ~130m copper cable (3 gauges)
  - ~2m copper/kapton (endcap) or aluminium/kapton (barrel) power tapes
  - Voltage limiter in line to block spikes due to sudden drops in load
- Typical overall efficiency ~40%

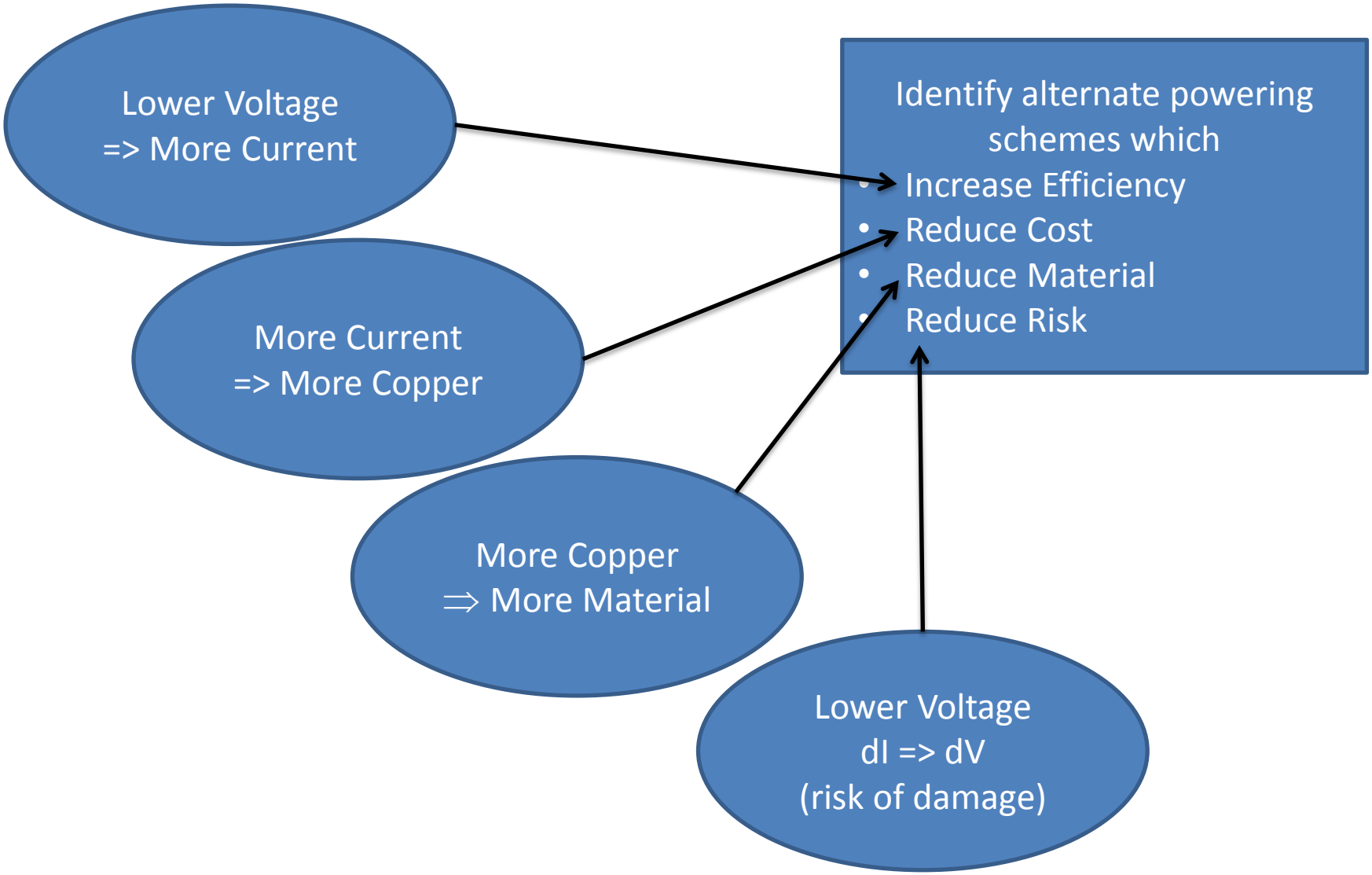
Example: CMS Silicon Strip Tracker



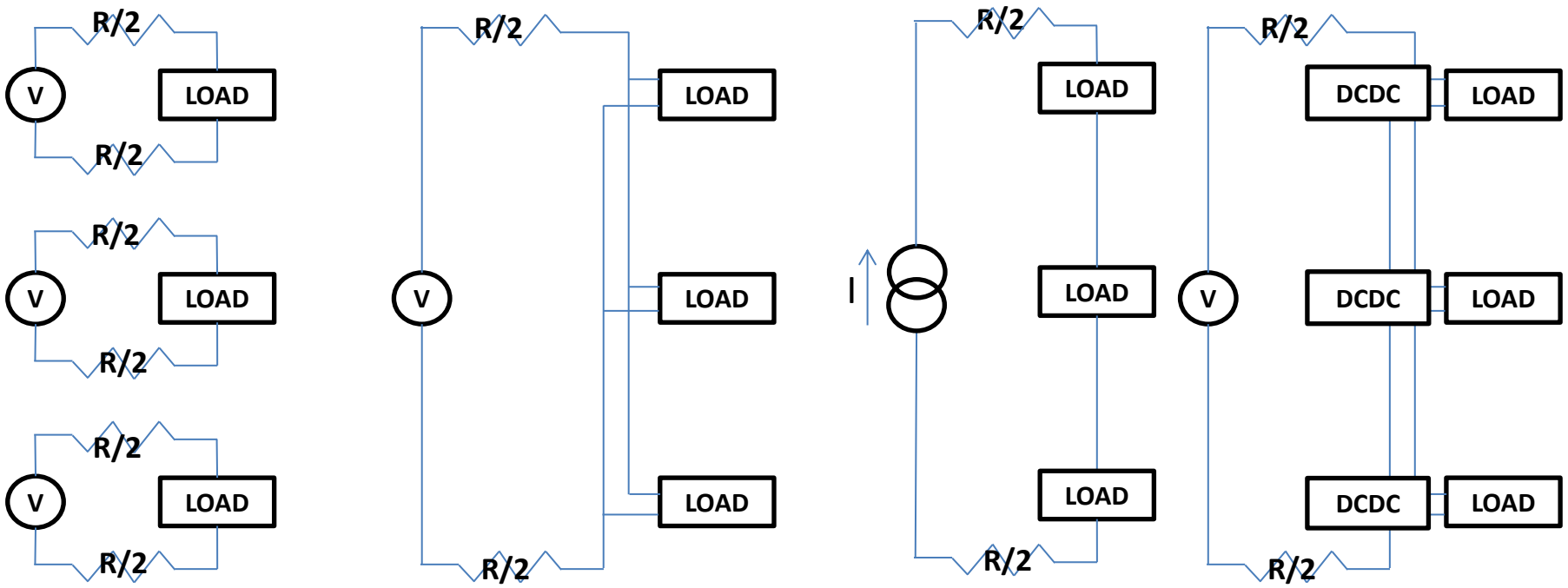


- 15000 Detector Modules
- **Parallel Powering**
  - 1944 “detector power groups”
  - 29 racks in **main cavern**
  - (up to) 6 crates per rack
  - CAEN EASY system for “hostile environments”
    - Magnetic field tolerant
    - Radiation tolerant
- Typical cable run
  - 40m copper + 6m aluminium
- Typical overall efficiency ~40%

Motivations for Change



Powering Schemes and Cables



Independent Powering | Parallel Powering | Serial Powering | DC-DC Powering

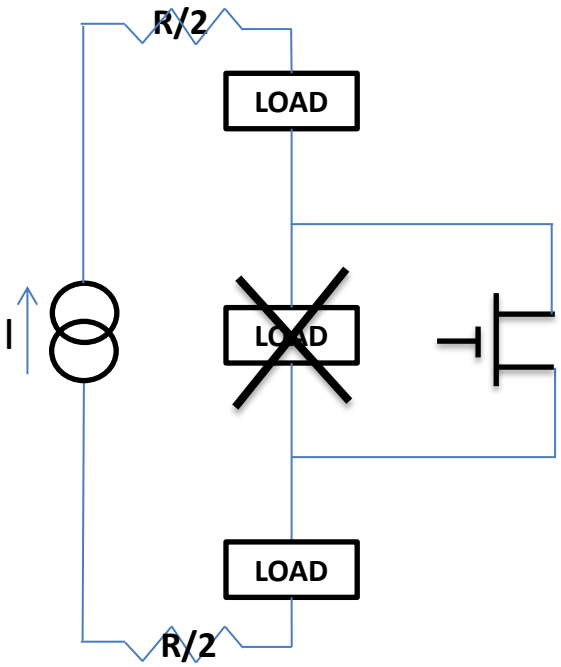
Losses in off-detector cabling of total resistance R for n loads drawing current I:

$P = nI^2R$ $P = n^2I^2R$ $P = I^2R$ $P = n^2I^2R / r^2$

where ratio r = Vin/Vout

Serial Powering and DC-DC Point of Load conversion offer more efficient cable usage than Independent or Parallel Powering. *Total system efficiency will be lower as this depends upon the efficiencies of bulk supplies, DC-DC converters, shunts etc. which are neglected here.*

Serial Powering

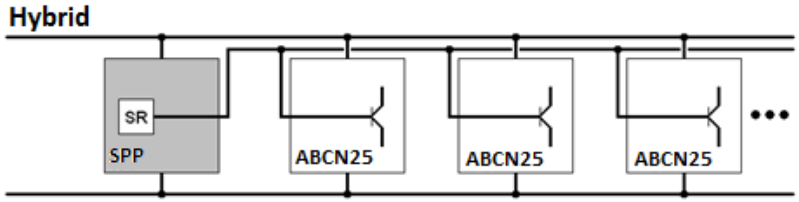


- Elements of a serially powered system
  - Current Source
  - Shunt regulator / transistor
  - AC or opto-coupling of control signals
  - Protection circuit & Bypass shunt
    - Shunt current past faulty device in response to over-voltage condition or under DCS control
- Current must be sufficient to cover the peak demand of the biggest load in the chain
  - Best suited to chains of identical devices
  - Not ideally suited to disk geometries (but possible)
- Intrinsically low mass, needs little if any extra space
  - Can be useful for tracking detectors, especially pixels (where power density highest and space most limited)

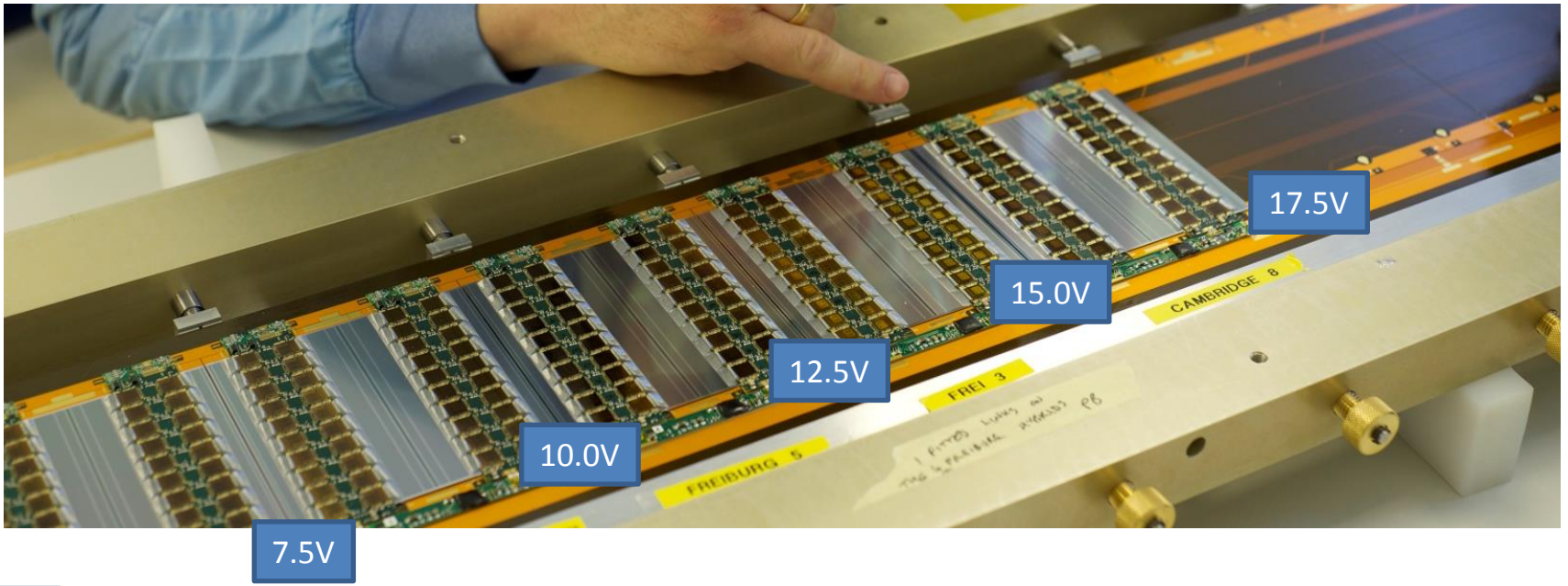
Example: ATLAS ITk Strip Stave with SPP

- Distributed SP Architecture
  - Shunt transistors within ABCN25 FE ASIC, 20 per hybrid
  - One control block per hybrid (op-amp) or module (SPP)
- Three short (4 module) prototypes built
  - Good results in “Chain of Modules” Configuration
- One long (12 module) prototype part-loaded (7 modules)
  - With integrated protection from SPP chip

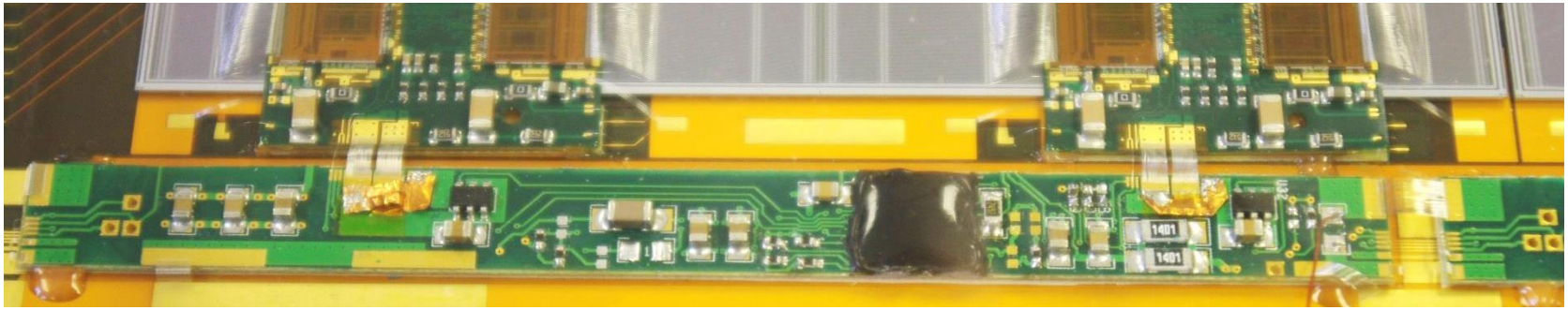
Further Example in Backup



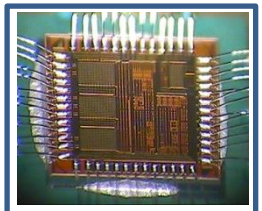
Distributed SP Architecture (within the hybrid)



Example: ATLAS ITk Strip Stave with SPP



- Serial Power and Protection (SPP) Chip
  - Shunt Regulation
  - Over Voltage Protection
  - Bypass under DCS control



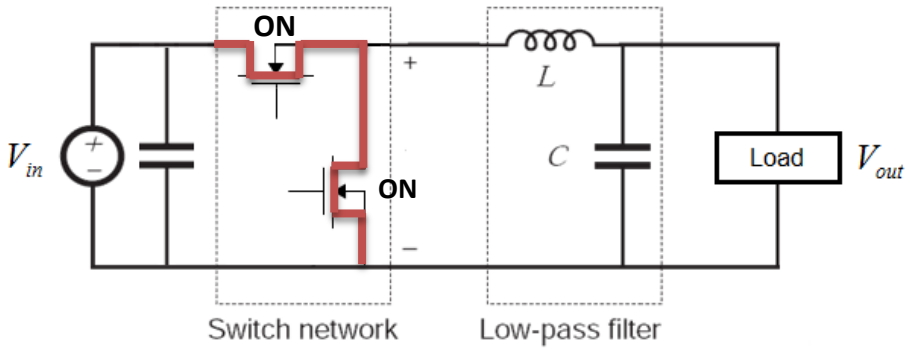
SPP Chip

- Designed for 2A @ 1.5V
  - PCB adds commercial FETs to handle 10A @ 2.5V
  - Component count for phase 2 much lower
- Strip Stave with SPP has unfortunately been something of a development exercise
  - Powering PCB made for wrong polarity
  - Corrected by copper foil straps rather than respin due to limited SPP availability

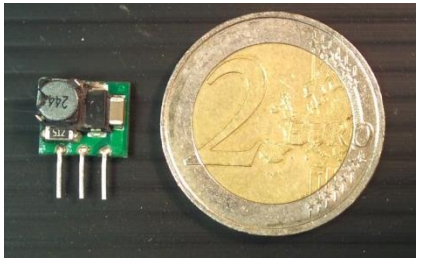
- Developed working startup procedure
  - Ramp in small steps
  - Enable desired modules
  - Ramp some more
- Analogue results mixed
  - ENC good
  - DTN shows progression along stave
- SPP will work better in a 1.5V, 2A system
  - Present test is perhaps unfair

- **Also Pixel SPP (PSPP) for ATLAS Pixels**
  - Adds I2C control bus & ADC
  - System studies with FE chips to follow

DC-DC Synchronous Buck Converter



Output voltage is regulated by adjustment of the duty cycle of the two switch transistors

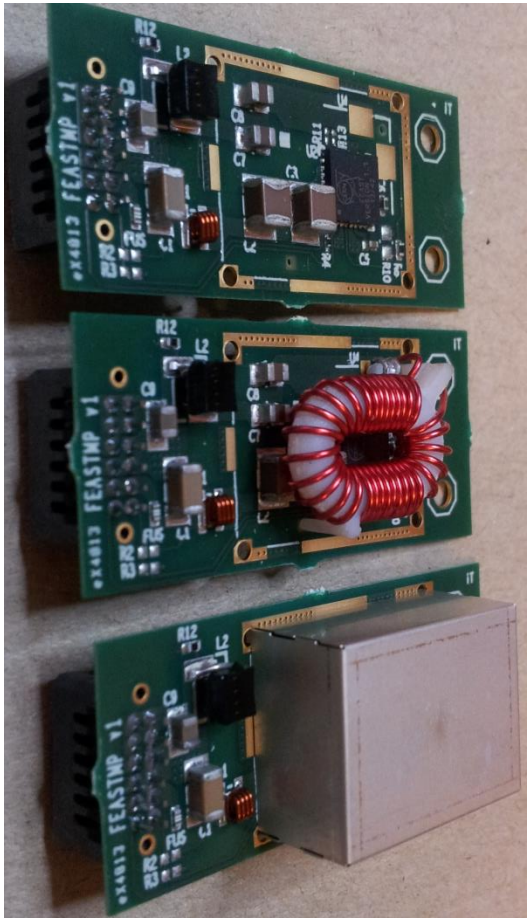


Typical Commercial Buck Converter:
Input 24V, Output 5V 1A, 90% efficiency

- Why not COTS?
  - readily available
  - cheap & efficient
  - small and reliable
- BUT
  - ferrite-cored inductors
    - may not be used in magnetic fields
  - not radiation hard
    - may not be used in many experimental environments
- We need custom converters
  - air-cored inductors
  - radiation hardened ASIC
  - *for tracker applications: low mass design*

Buck Converters for HL-LHC Phase 1

- An initial production of 1000 FEASTMP modules, a converter ASIC **for Phase 1 upgrades**, has been completed by CERN
  - FEAST2 ASIC follows on from AMIS5 prototype in same, commercial 0.35um technology
- FEASTMP DC-DC converter Module
  - 127um thick tinned copper shield
  - Custom 430nH oval air-cored inductor
  - Vin 5V to 12V (min Vin = Vout+2V)
  - Vout 1.2V to 5V, 4A max
  - EMC compliant with conductive noise requirements of CISPR11 Class B
  - TID above 200Mrad, displacement damage up to 7e14 1MeV neutrons/cm^2
  - Magnetic field tolerance > 40,000 Gauss
  - Area 37.57mm by 16.94mm
- The converter is quite large and massive
  - Meets needs of (most) Phase 1 customers

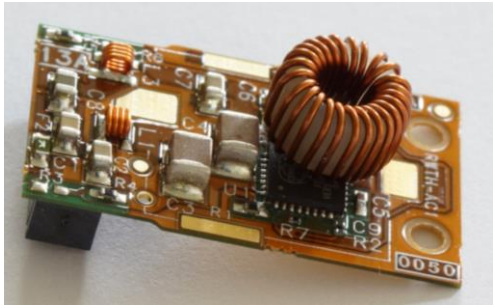


Example: CMS Pixel Upgrade

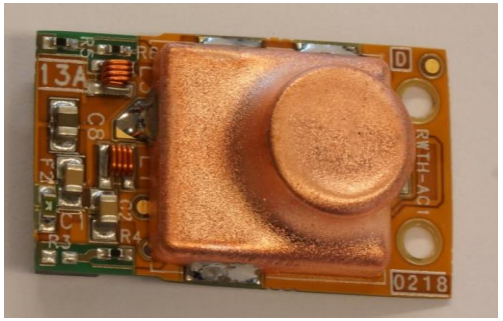
See "CMS Pixel Detector Phase-1 Upgrade", Wolfram Erdmann, Tuesday of this workshop

- For installation in 2016-17 Extended Technical Stop
  - x1.9 increase in channel count
    - x1.9 increase in power consumption
  - Must use existing cable plant
- Use DC-DC converters with FEAST2
  - Toroidal 430nH air-cored inductor
  - Converters located 2.2m away from modules
  - 13 converter pairs (analogue, digital) per bus board
    - Each converter pair serves 1 - 4 pixel modules
  - I_{out} < 3A per converter
- No noise increase due to use of DC-DC converters

Efficiency Plots in Backup

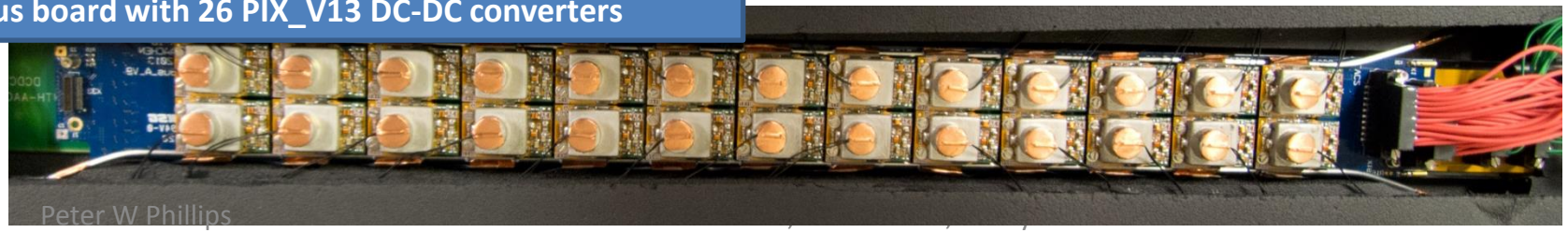


PIX_V13: 2.8cm x 1.7cm x 0.8cm; 3.0g



Shield: 0.3mm plastic, 48µm copper

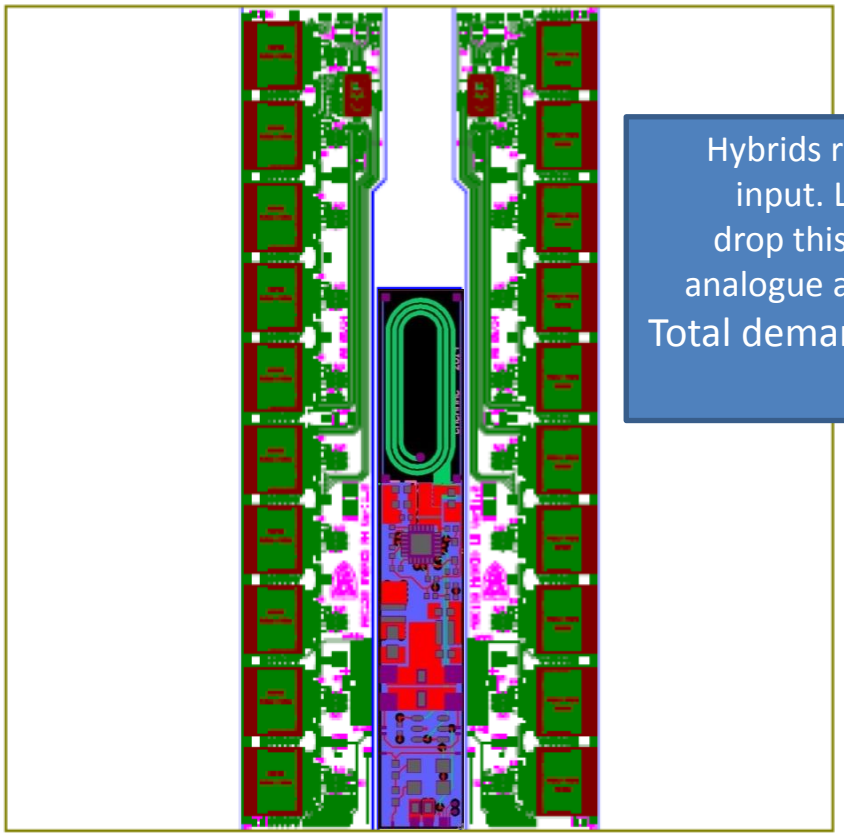
Bus board with 26 PIX_V13 DC-DC converters



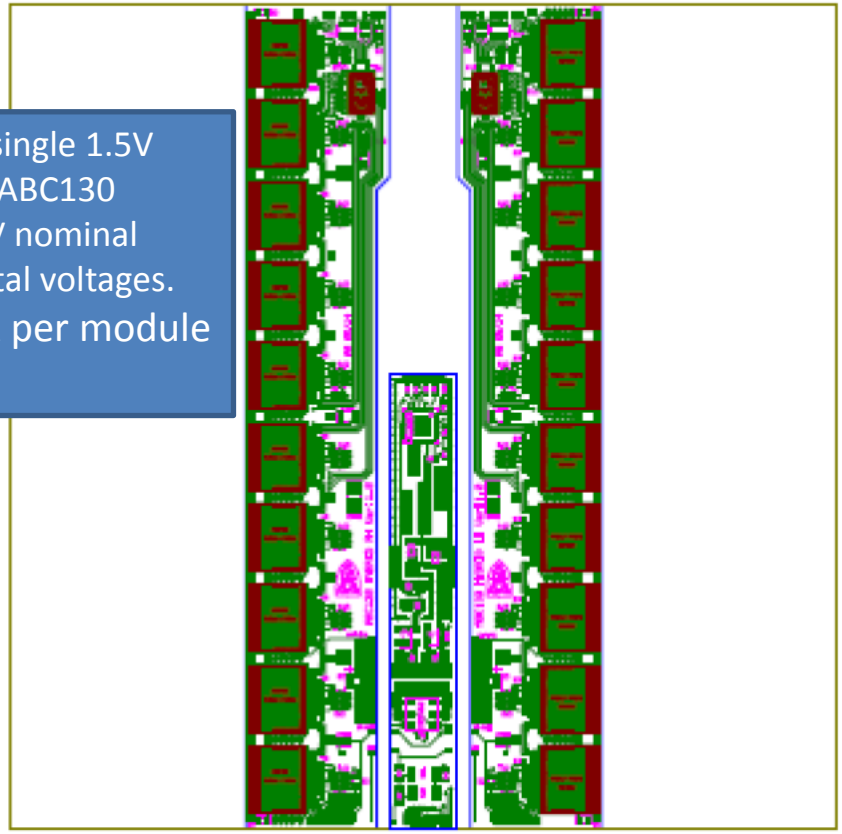
Buck Converters for HL-LHC Phase 2

- FEAST2 in I3T80 technology does not meet the Phase 2 specification in terms of its susceptibility to displacement damage
  - Failure of on-chip linear regulators at >5e14 n/cm2
  - Excessive bandgap shift => change of output voltage
- Plan move to the similar I3T25 process
  - Access to different p-channel LDMOS transistor
- Test structure with linear regulator
  - functional at >>5e14 n/cm2
- Test structure with new bandgap
  - submission this month, results early 2015
- Possible additions to FEASTxx (subject to experimental request & CERN approval)
  - Trimming of reference voltage to have smaller spread of output voltage
  - Bus control option based upon I2C or similar protocol
- Otherwise FEASTxx chip will be the same as FEAST2
  - Electrical performance identical
- Experiments can use FEAST2 during R&D and move to the new chip once it becomes available
  - but before production ;-)
- ***For tracking detectors, different form factors with lower material are of particular interest***

Packaging for ATLAS ITk Strip Stave



Hybrids require single 1.5V input. LDOs in ABC130 drop this to 1.2V nominal analogue and digital voltages.
Total demand <2A per module



Yale Planar Coil Converter (64 x 10)

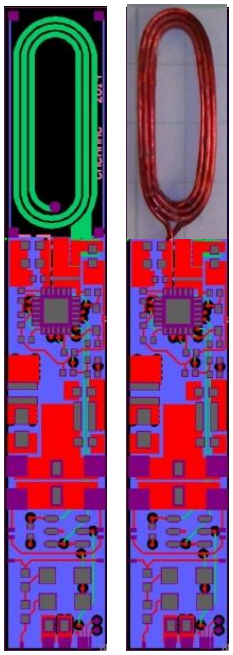
Both include HV filter components

Liverpool "Abracon" Converter (54 x 8)

Packaging for ATLAS ITk Strip Stave

ATLAS ITk Strips is prototyping a series of DC-DC PoL converters which may be mounted directly on the sensor.

- Bottom layer must be hermetic electrostatic shield (blind vias etc)
- Present devices use the LTC3605 chip but we will soon move to FEAST2.
- To maintain clearances during insertion it is important height < 5mm.



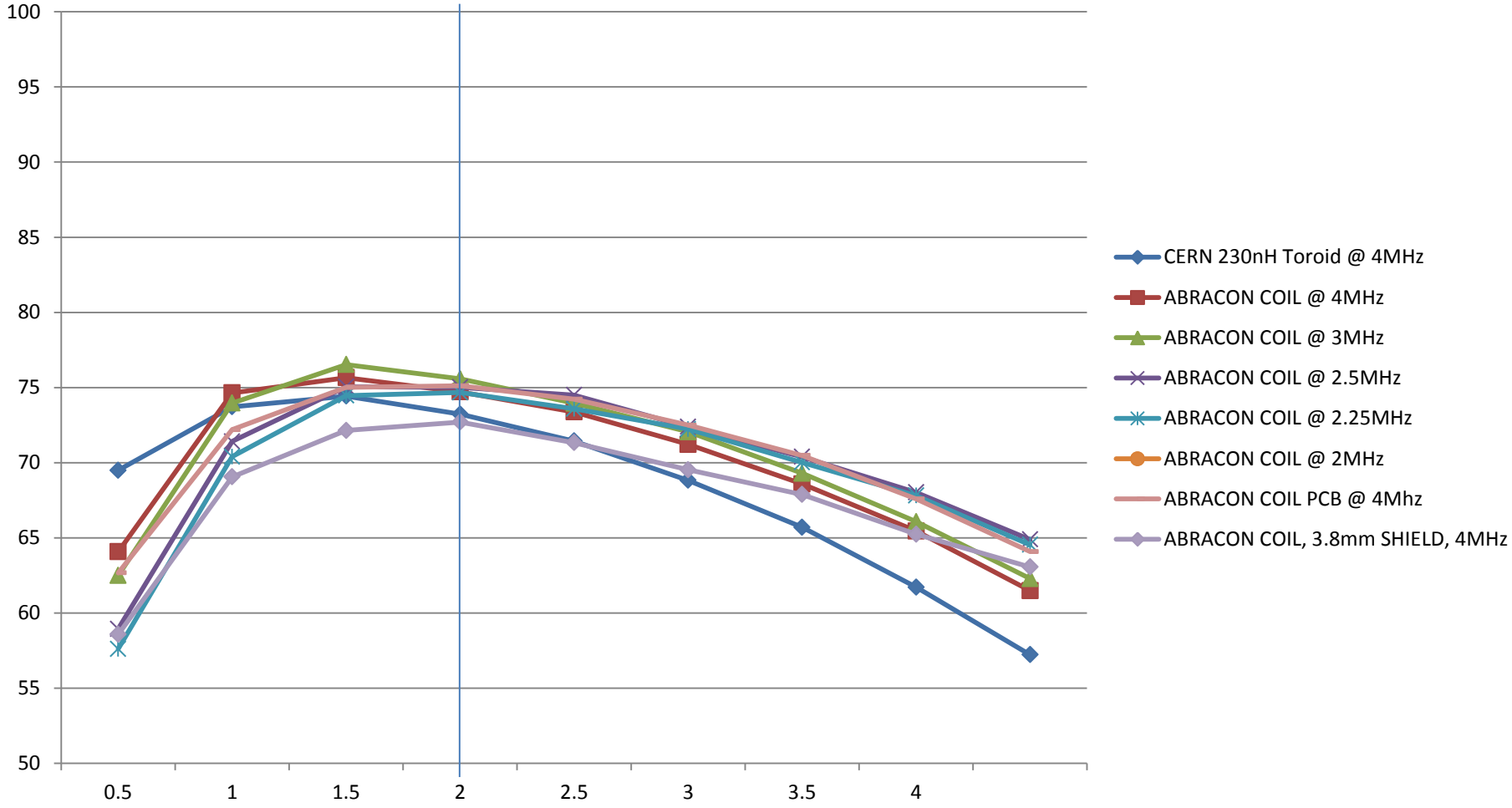
Yale Planar Converters

- Yale variants with and without integrated planar solenoid
  - Optional 560nH custom wound solenoid of similar geometry (industrial samples in progress)
- Switching frequency from 2MHz to 4MHz
  - For given inductance, better efficiency at higher frequency
- Highest component is 0805 filter capacitor at ~2mm
  - For simple cuboid shield, sets height **~2.3mm**
  - If necessary, shield may be profiled

- Liverpool unit 8mm wide
  - commercial 120nH solenoid
- Next version ~10mm wide
  - Solenoid in range 140 to 160nH (20% to 30% more)
- Switching frequency from 2MHz to 4MHz
  - For given inductance, better efficiency at higher frequency
- Highest component is the coil at 3.5mm
  - For simple cuboid shield, sets height **3.8mm**
  - If necessary, shield may be profiled

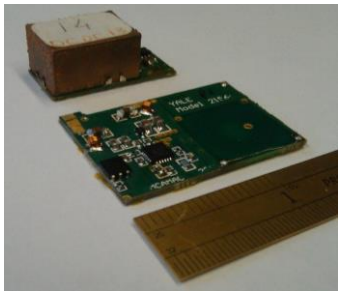
Liverpool "Abracon" Converter

Packaging for ATLAS ITk Strip Stave: Efficiency

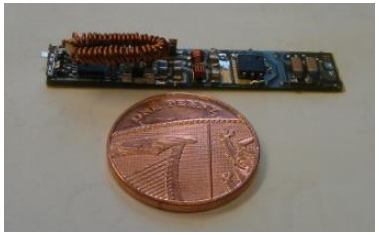


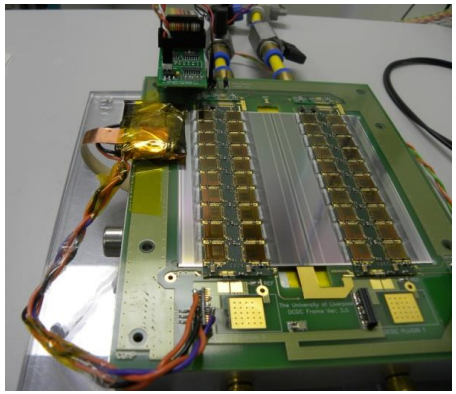
Expected efficiency of “Abracon” converter at 4MHz, 1.5V, 2A is 73%

Can DC-DCs *really* be placed on strip sensors?

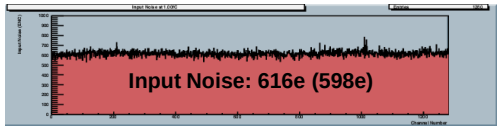


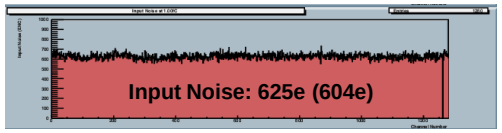
YES!





Converter placed <3mm from bond wires

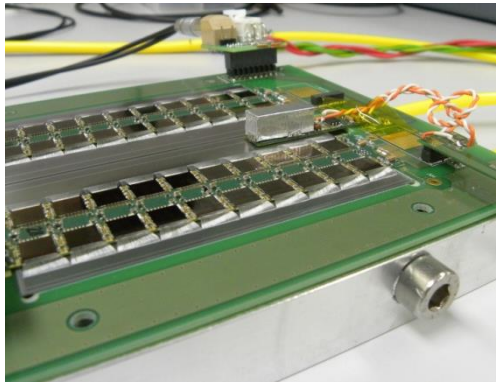




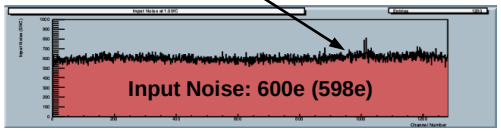
Reference measurement shown in brackets (CERN SM01C converter)

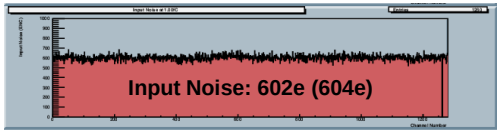
Tests with prototypes using both planar and wound coils show this is possible provided that

- Hermetic electrostatic shield is placed under the DC-DC
- Magnetic shield blocks path between coil and FE bonds



Leakage from shield box (~15e increase)

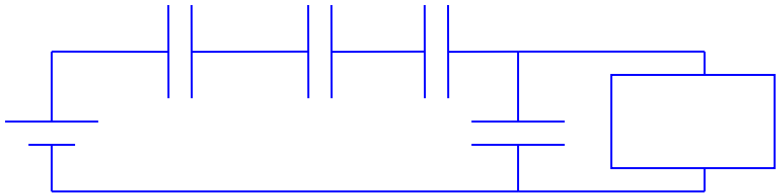




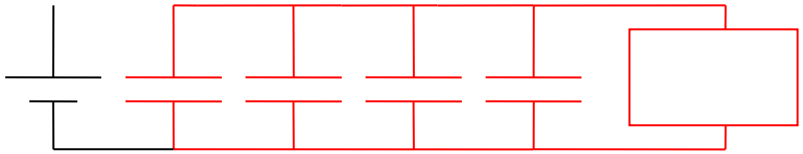
Reference measurement shown in brackets (CERN SM01C converter)

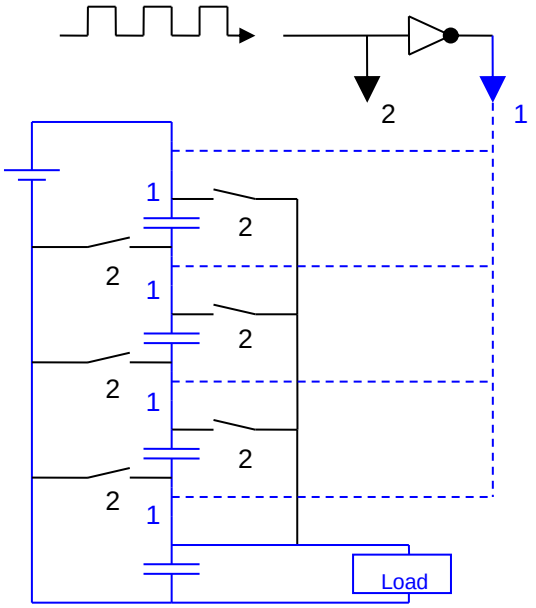
DC-DC with Switched Capacitors

Phase 1 – Charge in series



Phase 2 – Discharge in parallel



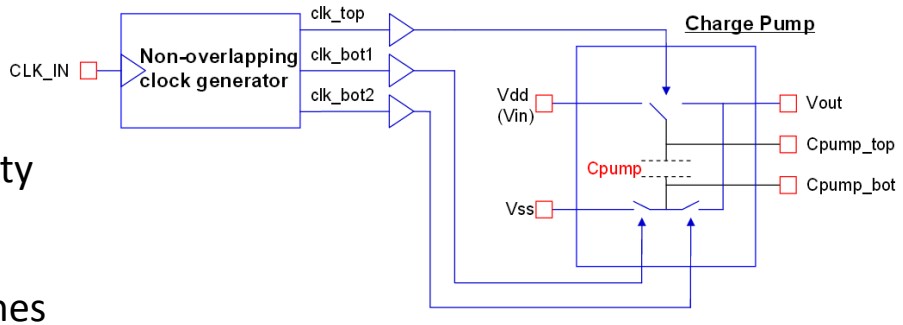


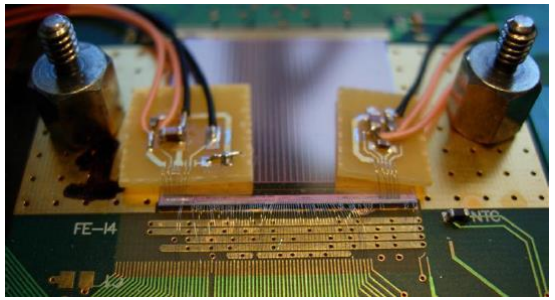
No inductors – can be implemented on our FE hybrids – even completely in the FE ASICs

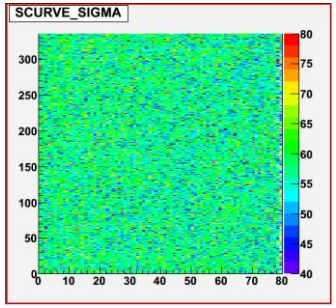
- Much industrial R&D focussed in this area
- A high efficiency alternative to on-chip LDOs
- May be used as part of a DC-DC or SP powering scheme
- Concept successfully demonstrated with ATLAS FE-I4A ASIC (**next slide**), CMS CBC2 etc.
- Optimum performance requires access to technologies with integrated capacitors

Example: Switched Capacitor DC-DC circuit in ATLAS Pixel FE-I4A

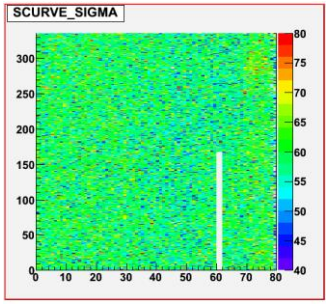
- Non-overlapping Clock Generator
  - generates 3 internal clocks from CLK_IN
  - same frequency but different phase & duty
- Charge Pump
  - consists of 4 transistors working as switches
  - manipulates pump capacitor under control of clocks
- External Pump Capacitor
  - Must be close to ASIC for good results
  - No significant impact upon noise performance when Cpump on top of FE-I4A
    - Missing pixels unstable, not related to DC-DC
- Demonstrates Technique is Viable
  - Best results would require access to ASIC technologies with embedded capacitors







Normal Power

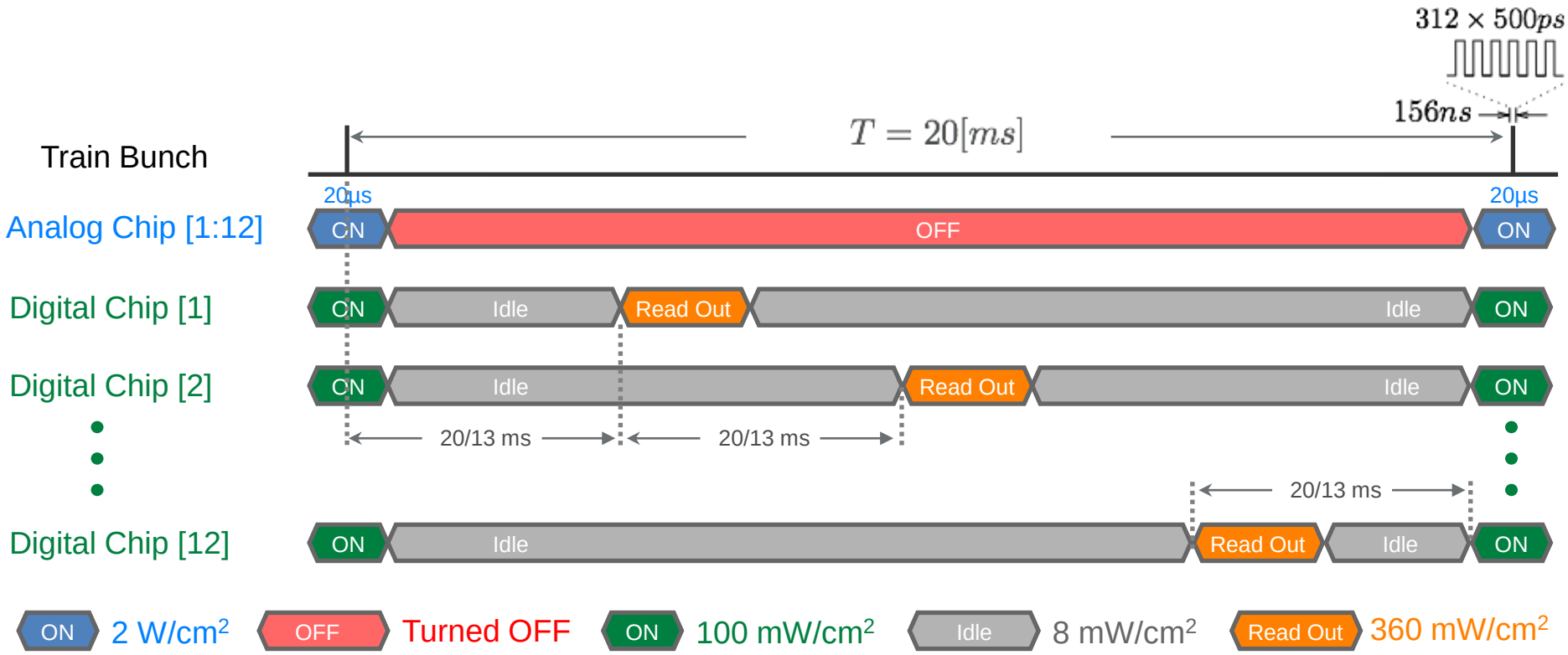


DC-DC Power

Possible Further DC-DC Developments

- CMS Tracker Powering schemes still under development
  - PS module particularly challenging
- A second stage buck converter is under discussion within CMS as a possible alternative to switched capacitor scheme
  - FEAST minimum output 1.2V
  - An ASIC for a “low output” converter could be based upon the experience with FEAST and implemented in well-known 250nm technology, so this should be straightforward.
- More exotic designs are of course possible if the community really needs them
  - Requirements should become more clear in the next few years…
- Example: DC-DC with GaN for higher input voltage and / or higher frequency operation
  - Higher frequency operation should permit more efficient operation for small inductors
    - Smaller package may permit higher efficiency for fixed, small inductance
  - May also be of interest as part of a multi-stage DC-DC powering scheme
    - 48V to 12V near detector (GaN)
    - 12V to XXV on detector (FEASTxx)
  - Optimal use of GaN power transistors with silicon driver would rely upon flip chip or similar advanced packaging technology
    - Inductance of control nodes must be minimised to get to high frequency
    - Packaging not cheap
  - Additional effort would be required to deliver this

Recall: Power Pulsing for CLIC / ILC

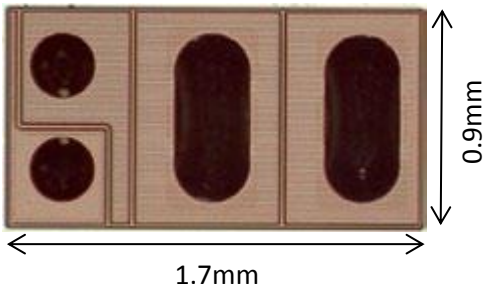


- ➡ Turn OFF most electronics between bunches (“Power Pulsing”)
- ➡ Factor of 1000 reduction in power for CLIC
- ➡ Factor of 200 reduction in power for iLC

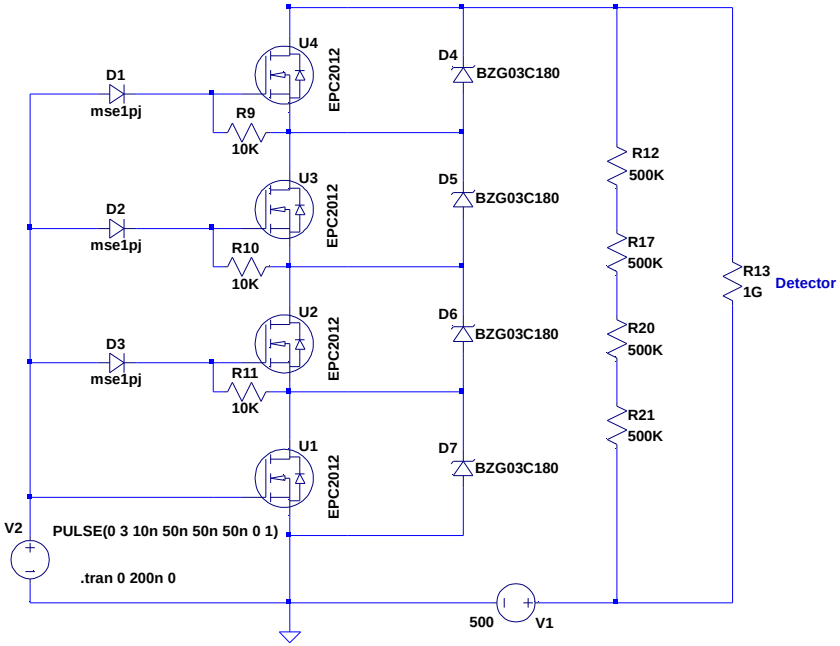
See “R&D for the Vertexing at CLIC””,
Sophie Redford, Tuesday of this workshop

ATLAS ITk: Sensor Bias Multiplexing

- Bias cables of course have mass
  - Can be a concern in tracking applications
- Could parallel power n sensors
  - May lose all of them if one fails as a short
- Propose use of rad-hard HV switches
  - To be able to disconnect any failed sensors
- Present phase: Device Identification
  - Study of commercial HV transistors
    - GaN, Silicon, Silicon Carbide
    - before and after irradiation
- Most Promising candidate to date
  - EPC2012 (200V GaN)

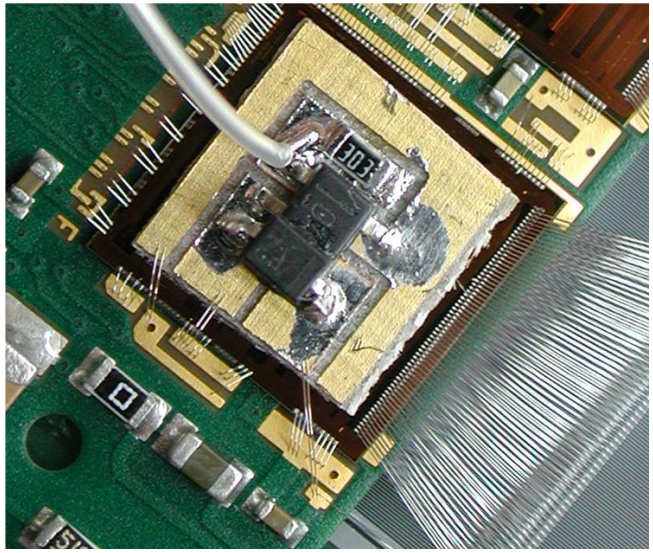


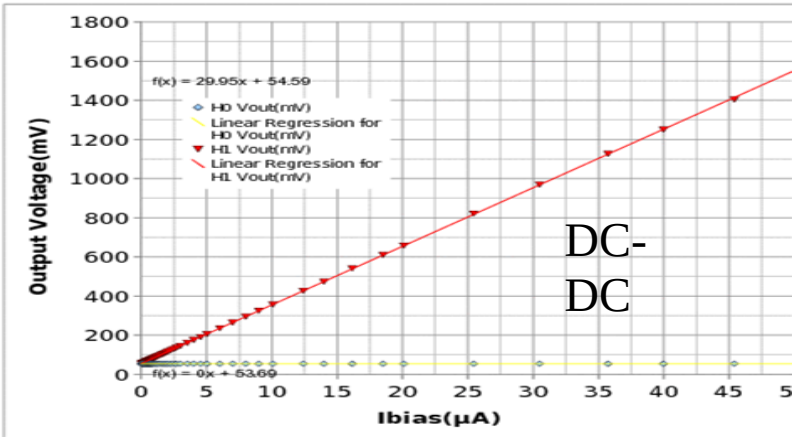
- EPC2012 may be used in a “stack” to switch higher voltages
  - Possible circuit below



- Waiting for 600V GaN samples…

ATLAS ITk Strips: On-Hybrid Sensor Current Measurement





- Fast Signal Return on Hybrid
  - Strip Bias AC coupled at 4 corners
- DC return
  - One corner has diode/op-amp combination
    - Normal DC path through op-amp
    - Backup DC path through diode (accommodates amplifier offset)
- Proof of Principle test using commercial parts
  - OPA365, 1N4148
  - **No additional noise for test module using DC-DC converter**
- Circuitry included in HCC chip
  - Op-amp plus ADC
  - Results in 2015

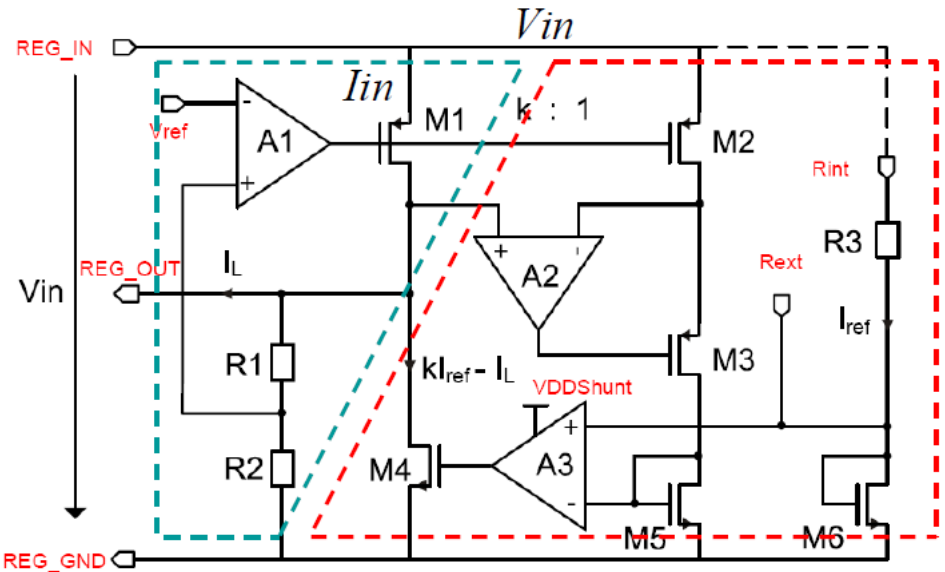
Conclusions

- Two main power strategies being explored for HL-LHC
  - Serial Powering
    - circuit blocks built, small scale system tests give encouraging results
  - DC-DC Buck converters
    - demonstrated to meet the requirements of Phase 1 Upgrades
    - work towards “tracker friendly” packaging ongoing by ATLAS & CMS
- In addition
  - Switched capacitor DC-DC conversion is a viable, high efficiency alternative to on-chip LDO regulators
  - Power Pulsing is a useful technique for Linear Collider detectors and others with a low duty cycle
  - Identification of radiation hard “HV” switch transistors, together with a proof of principle of on-module sensor current measurement, may lead to further reductions in HV cables
- There is no “one size fits all” solution
  - Each detector system has its own efficiency/mass/power/space constraints

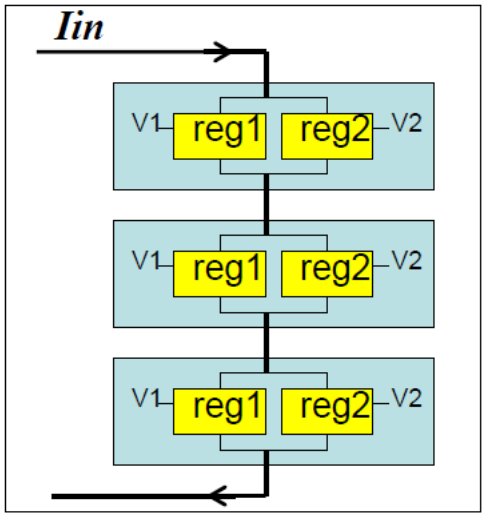
Backup

Example: ATLAS Pixel Shunt-LDO

- Combined Shunt and LDO (ShuLDO) in FE-I4
  - The **left** part is a standard LDO
  - The **right** part is the shunt circuit
- Benefit wrt standard shunt regulators
  - Shunt-LDO regulators generating **different output voltages** can be placed in parallel without any problem regarding mismatch and shunt current distribution



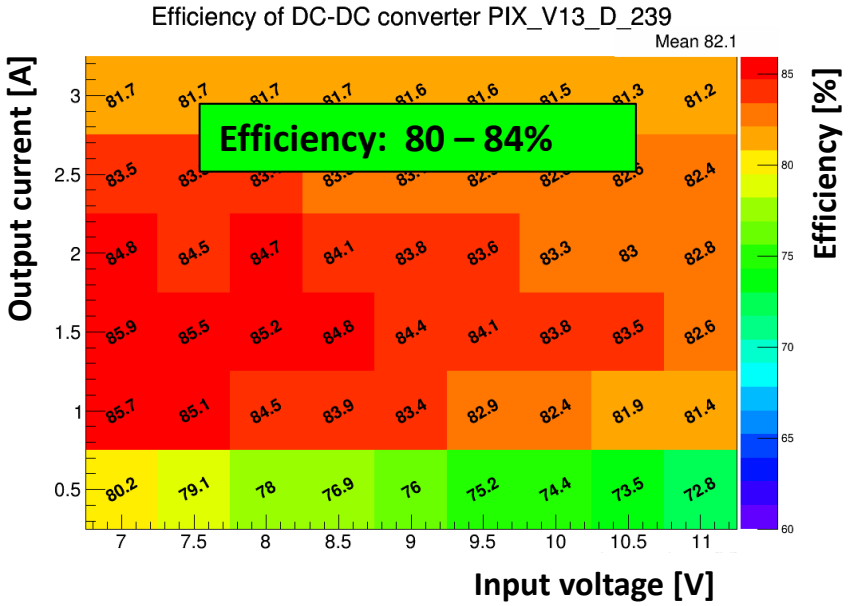
Simplified schematic of shunt-LDO

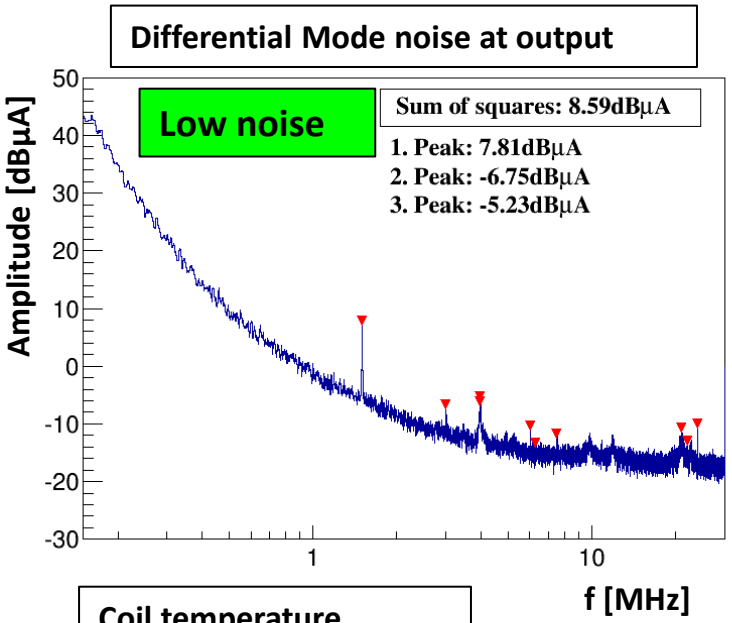


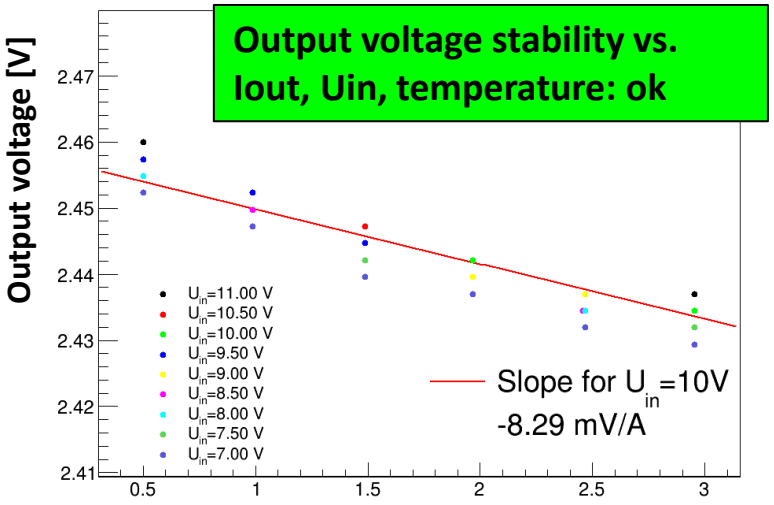
shunt-LDOs in parallel

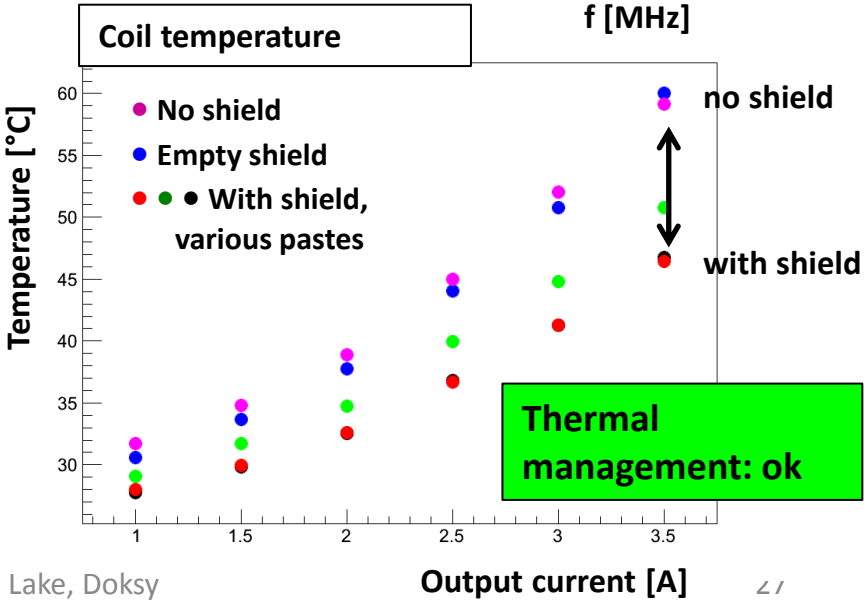
CMS Pixel DC-DC Performance

Figures from Katja Klein



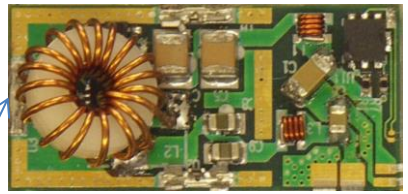


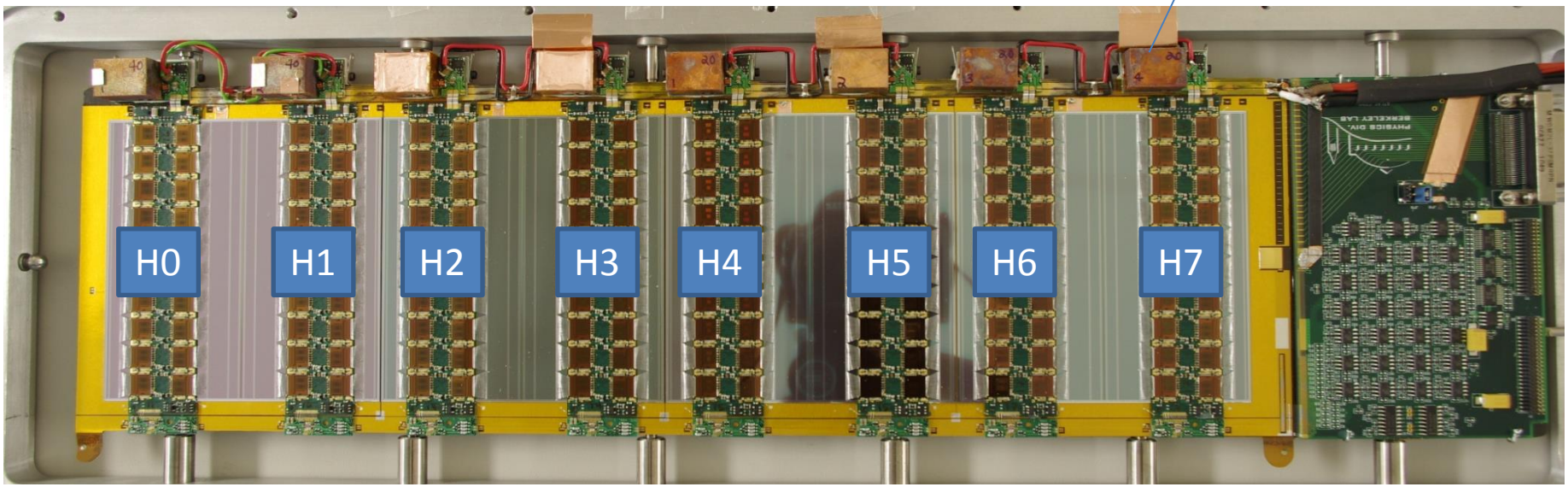




Example: ATLAS Strip Stave (DC-DC)

- STV-10 Buck Converters from CERN group used *on stave*
  - Based on commercial chip due to high current requirement
  - Low mass shield (plated plastic)
- Three short (8 hybrid) prototypes built
  - All with good results, even with converters adjacent to the front end
- Longer (24 hybrid) prototype under construction

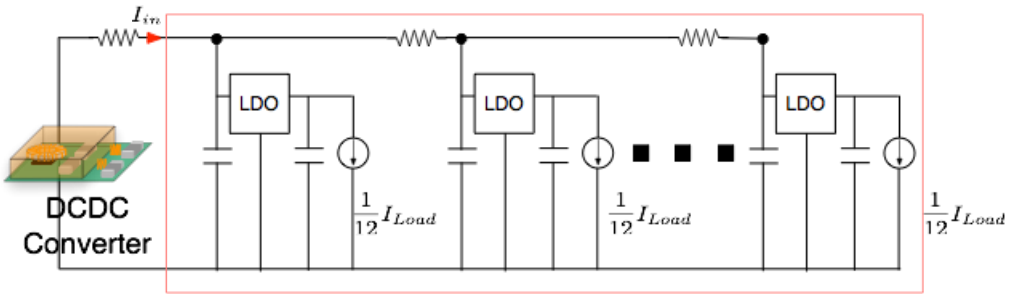




Power Pulsing for CLIC / ILC VERTEX

Possible Implementation

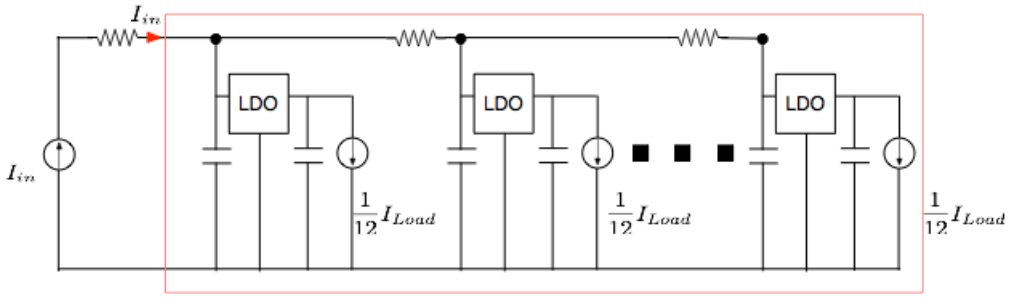
- Provide (10uF) capacitor by each FE chip
  - Functions as a local “battery”
- Add LDO to provide local regulation
  - May be part of FE chip



DC-DC Option

The capacitors must be re-charged between bursts

- Could use DC-DC converter
  - Too massive for LC application
- Could use current source
  - Favoured option



Current Source Option

Read reference below for more detail!

After Cristian Alejandro Fuentes Rojas et al, “Power pulsing schemes for analog and digital electronics of the vertex detectors at CLIC”, TWEPP 2013