Upgrades of the ATLAS inner detector for HL-LHC (pixels)

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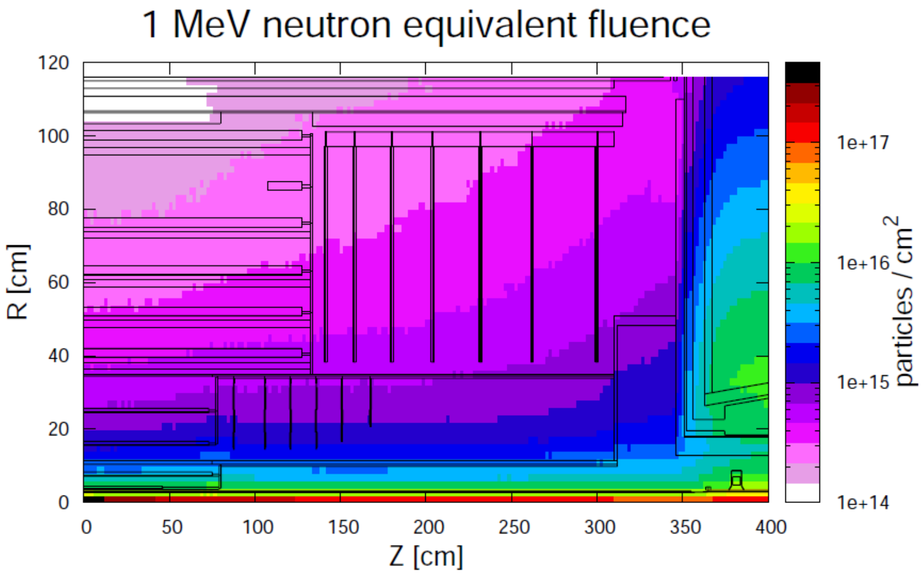
on behalf of the ATLAS Collaboration

Overview

- Introduction
- Module development:
  - New FE Chip
  - Sensor developments: planar, 3D, diamond, CMOS
- Read-out:
  - Triggering aspects & data transmission
  - Possible read-out scenario
- Mechanics

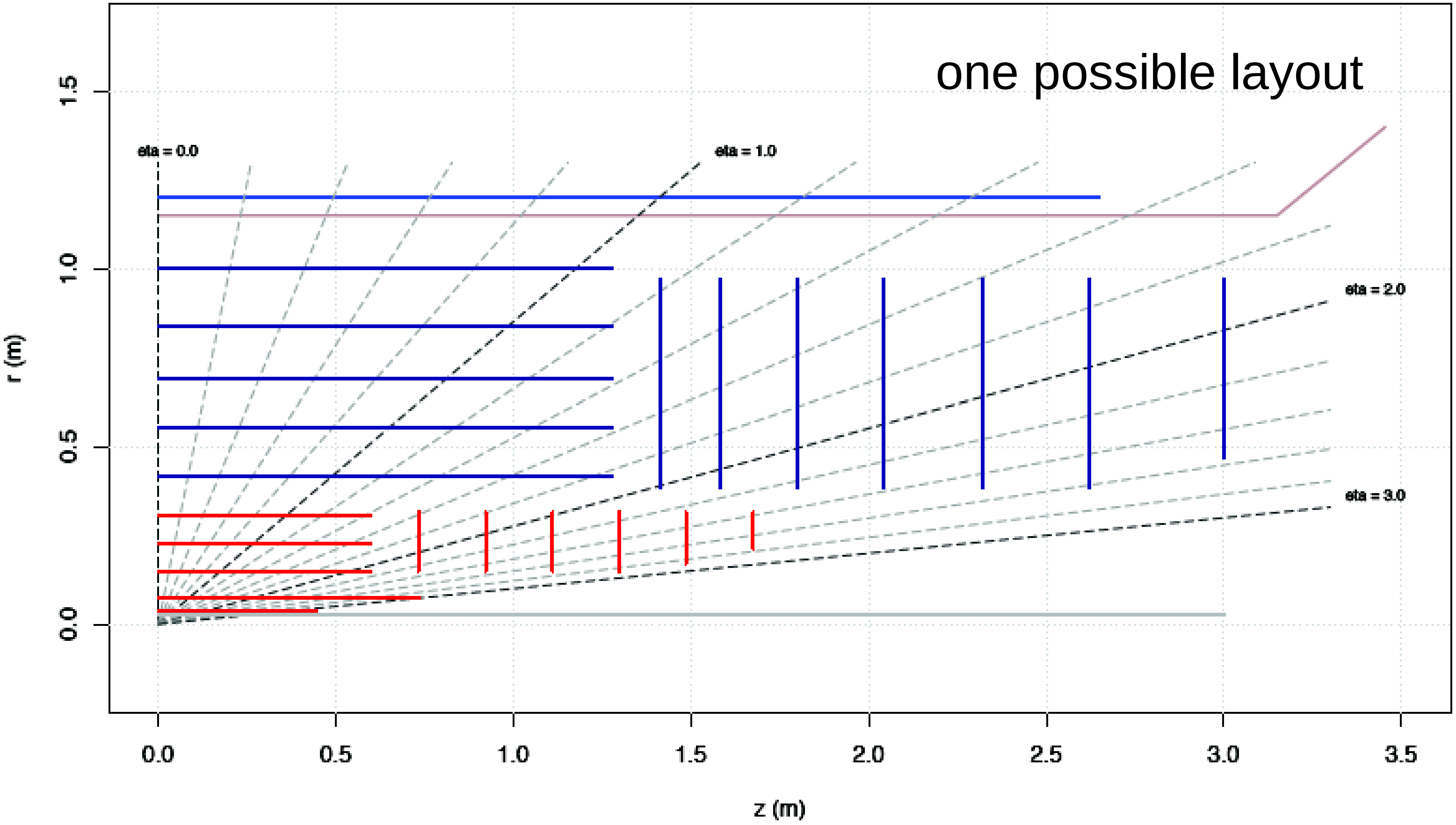
ATLAS ITK (1)

- ATLAS phase2-upgrade: complete re-design of inner tracking system for HL-LHC operation
  - Most of current detector not suitable for HL-LHC
  - Goal: maintain or improve tracking efficiency and small fake rate + b-tagging capabilities
  - Several challenges:
    - Higher track density
    - Higher irradiation dose, fluence
    - Higher hit rates → all silicon detector
    - Re-design of triggering system



ATLAS ITK (2)

- Plans for new “inner tracker” (ITK) taking shape
- New layout: all-silicon with outer strip layers and inner pixel layers



ATLAS ITK (2)

- Plans for new “inner tracker” (ITK) taking shape
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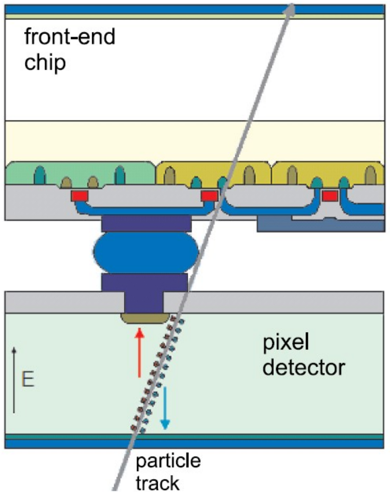
this talk

  - Pixel activities started to ramp up this year
  - Benefiting from 1st upgrade (insertable b-layer, IBL) that just completed:
    - Already had a re-design of the read-out (FE, off-det.)
    - Considered and used new sensor concepts:
      - 3D in outer layers of IBL (inner: planar sensors)
      - Diamond sensors in IBL-style diamond beam monitor (DBM)
    - Improved mechanics/cooling concepts

ITK Pixel Modules

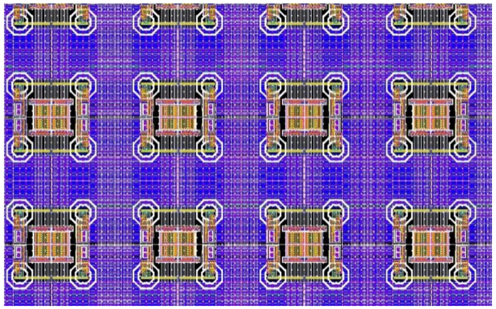
- Modules: use well-established hybrid concept
  - Sensors:
    - Planar-, 3D-silicon, diamond
    - New concept: CMOS, combined with hybrid r/o
  - FE chip: new design for all pixel layers (unclear availability of foundry that produced IBL FE)



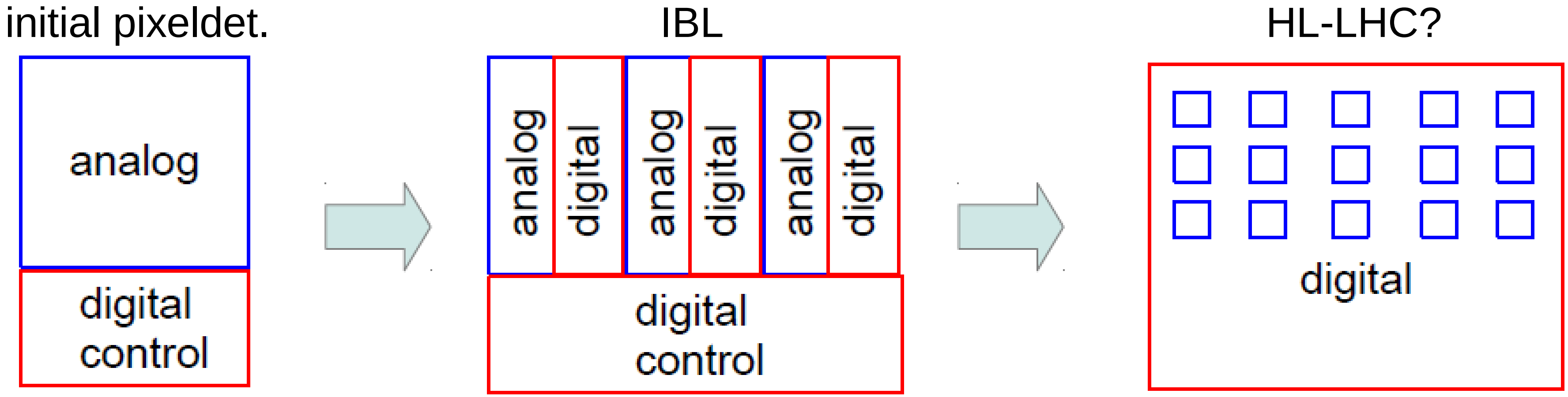
- In any case, many improvements needed:
  - Increased radiation hardness
  - Smaller pixels
  - Efficiency improvements in sensor design
  - Low(er)-cost interconnect technology

ITK Pixel FE Chip (1)

- Expected design specifications for FE chip:
  - Format, power similar to IBL FE
  - Pixel size:
    - Hit rate estimate: 2 GHz/cm^2
    - Preserve 50µm spacing between bumps
    - 2500 µm^2 pixel area: needs a recovery time of 200ns → larger area not feasible (squared 50x50 µm^2?)
  - Trigger rate: 1MHz single level (+ safety margin)
    - This requires several Gbps output per chip
  - Many things are the same for ATLAS and CMS → collaboration via RD53



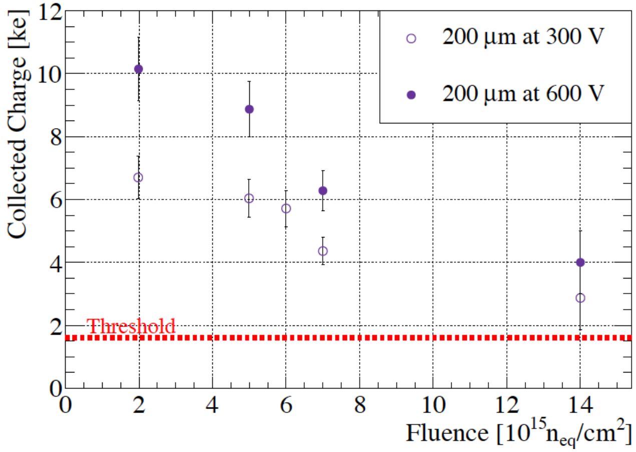
ITK Pixel FE Chip (2)



- Need improvement in digital/analog isolation (50kHz firing rate for 50x50 µm^2 pixel)
- Combined with low threshold (IBL: ~1000e possible): *very* challenging
- Check radiation hardness of new 130nm or 65nm vendors:
  - Target: 1 GRad
  - Qualification studies with 3 vendors on-going, but much more to do
- Design changes needed for high output rate

ITK Pixel Sensors (planar)

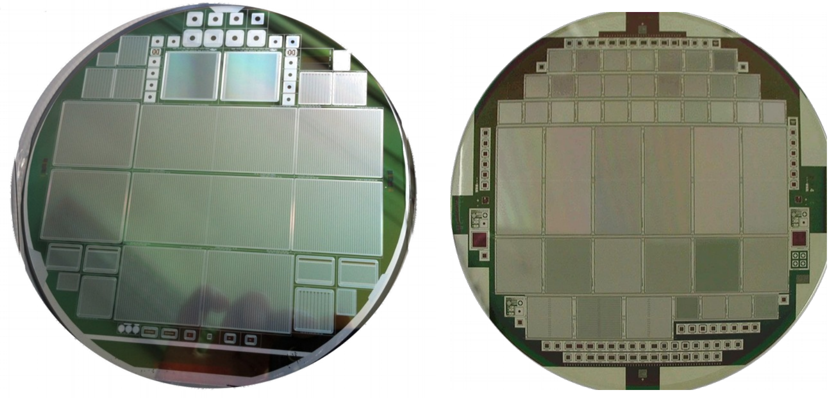
- Planar sensors (mostly n-in-p, also n-in-n)
  - Good candidate for outer layers: larger areas
  - Usage for inner layers: radiation hardness?
    - Charge collection studies done after irrad. to ~$10^{16} n_{eq} cm^{-2}$

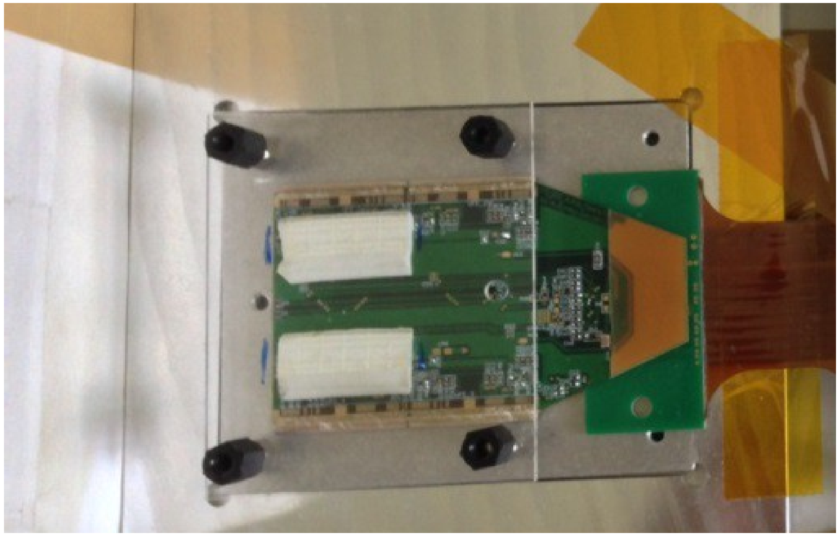


  - Other aspects investigated:
    - Better efficiency with active edge sensors
    - Thin sensors (<200 µm)
    - Pixel capacitance: small enough for FE?
    - Improve biasing structures (know ineff. from past)

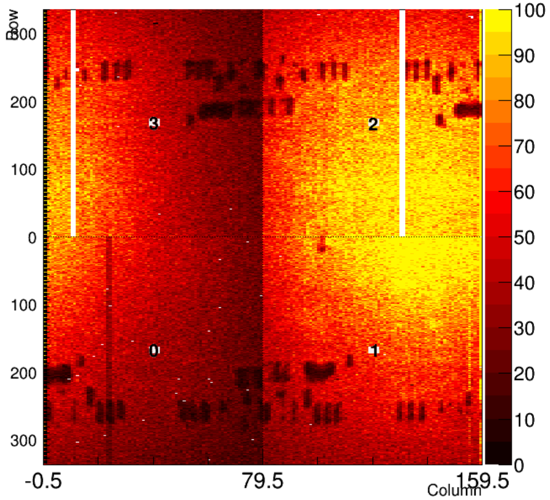
ITK Pixel Sensors (planar-quad)

- 2x2 FE modules built with planar sensors
  - Aim: reduce bump bond cost (scales per module)
  - Starting from IBL design: 2x 2-FE-sensor
  - Helps to build electrically functional quad-modules
  - Flexes designed for these modules, bump bond tests





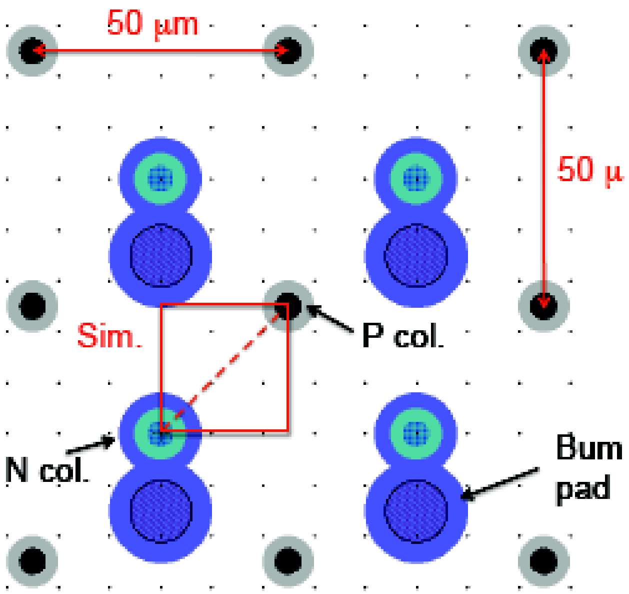
Test with Am241 source, all 4 FE read out in parallel



ITK Pixel Sensors (3D)

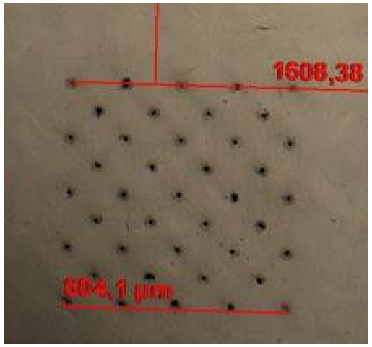
- 3D-sensors: driven by IBL vendors (CNM, FBK)
- Option for inner layers: adapt IBL design for new geometry and thickness
  - Smaller pixel size requires thinner sensors to take advantage of the high pixel spatial resolution
  - Radiation hardness : smaller inter-electrode spacing
  - Slim or active edges
  - Must tune pixel capacitance to meet FE requirements

3D cell layout (50 x 50)



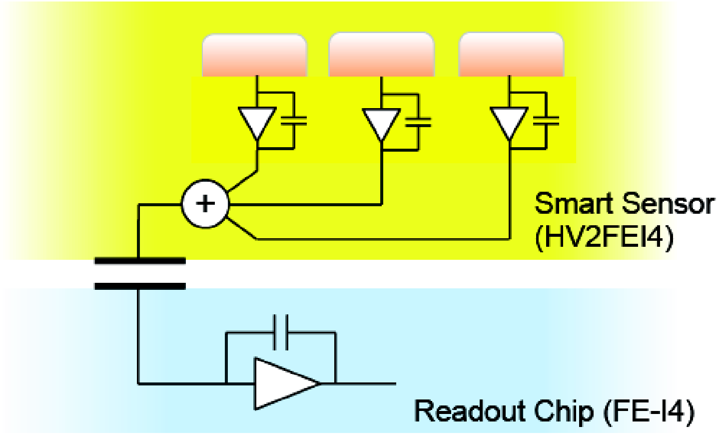
ITK Pixel Sensors (diamond)

- Diamond also option for inner layers
  - Fluence >$10^{16} n_{eq} cm^{-2}$: acceptable signal degradation
  - Stable operation at low thresholds (1000e or lower)
  - Sensor supply for 1-2 m^2 should be possible
- Vendor availability? Many produce pCVD but few at sensor quality
- Debug the bump-bonding issues from DBM
- Thinner sensors, 3D-diamond, ...



ITK Pixel Sensors (CMOS)

- HV/HR-CMOS: combine with hybrid concept
  - Use recent developments on CMOS “smart diodes”
  - Attach to “regular” FE chip for full read-out features
- Example: HV2FEI4 CMOS on IBL FE:
  - Combined operation possible
  - Used in src tests, testbeam
- Interconnect: bump bonds, gluing, TSV,...?



- Starting demonstrator project to evaluate if suitable for ATLAS

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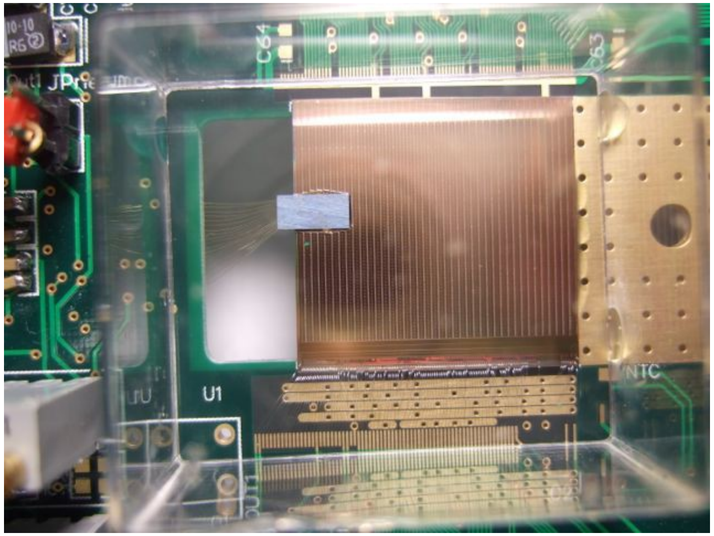

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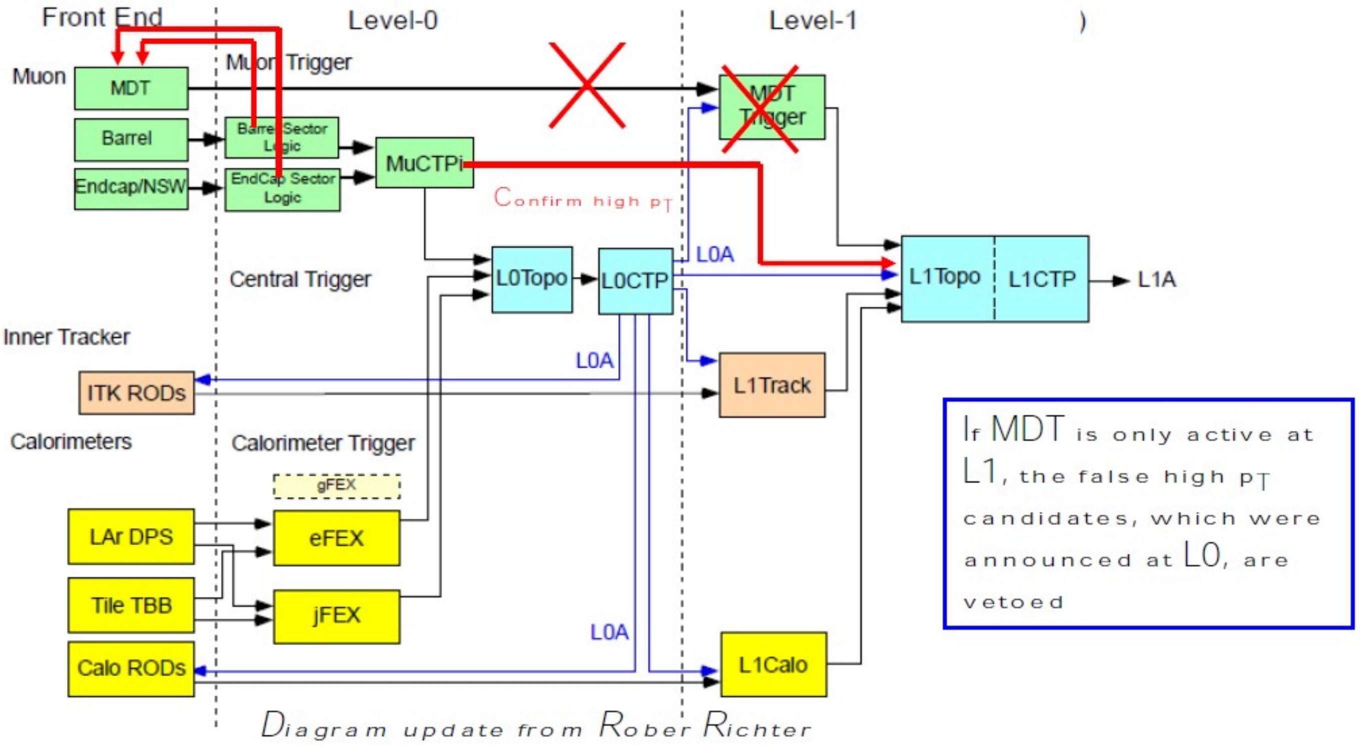
Triggering

- HL-LHC will see a new L0 trigger in ATLAS – partial/full read-out:
  - L0 : 1 MHz - 6 µs latency
  - L1 : 400 KHz – 24 µs latency
  - Pixel will do full read-out on L0

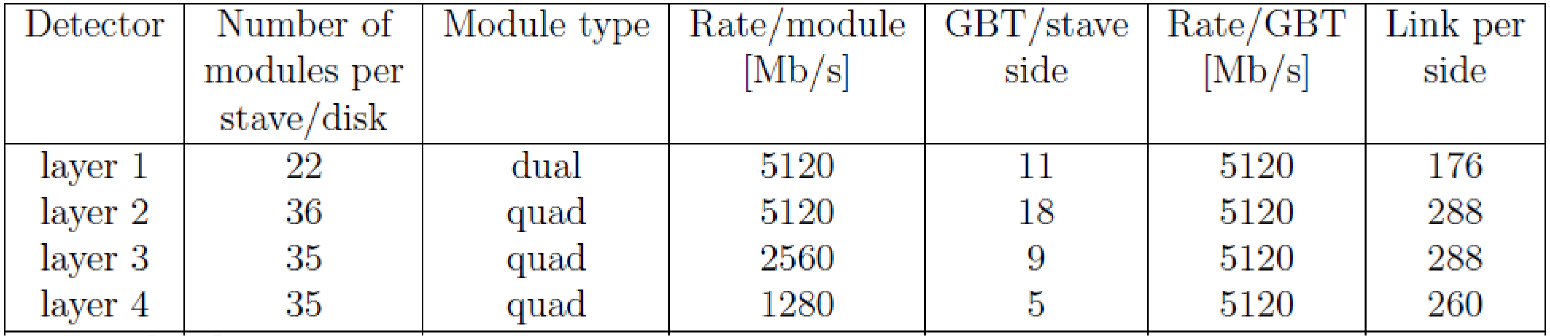


If MDT is only active at L1, the false high p_T candidates, which were announced at L0, are vetoed

Diagram update from Rober Richter

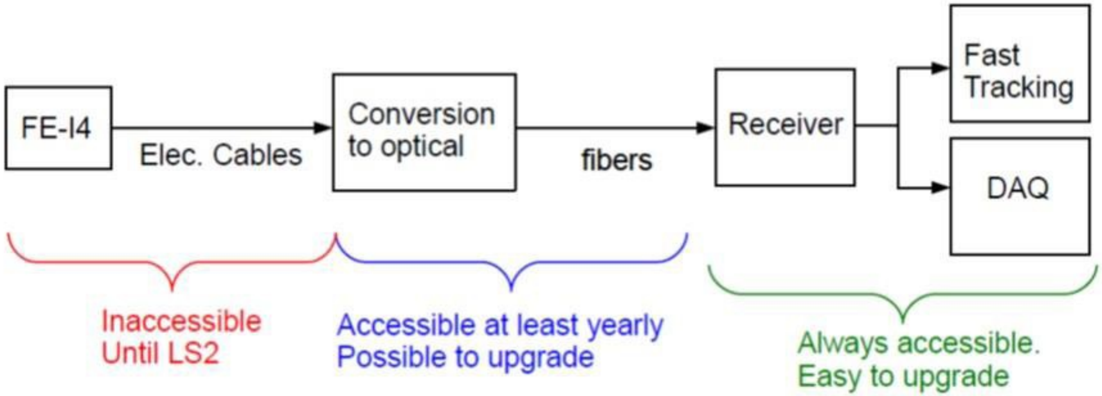
ITK Pixel Readout (1)

- Data rates and bandwidths at 1MHz trigger:



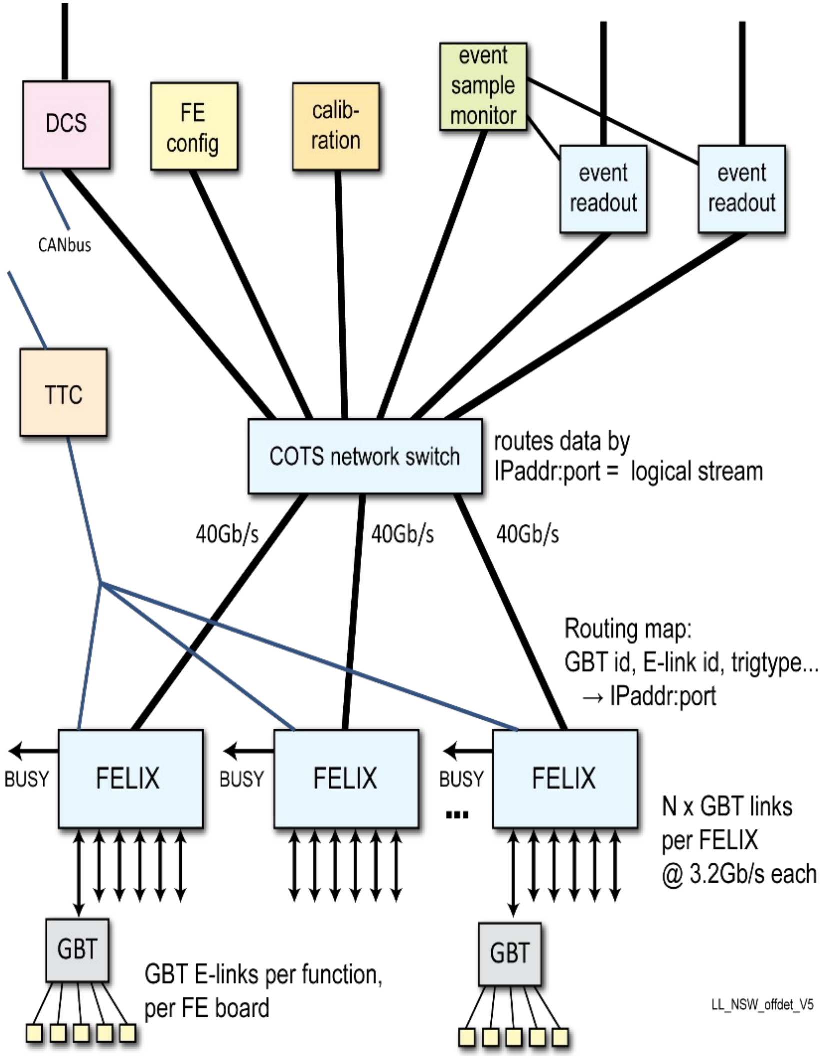
Detector	Number of modules per stave/disk	Module type	Rate/module [Mb/s]	GBT/stave side	Rate/GBT [Mb/s]	Link per side
layer 1	22	dual	5120	11	5120	176
layer 2	36	quad	5120	18	5120	288
layer 3	35	quad	2560	9	5120	288
layer 4	35	quad	1280	5	5120	260

- Data links:
  - Prefer to move opto comp. outside of det.volume: fast electrical cables
  - Then via fast optical links: GBT fast enough?



ITK Pixel Readout (2)

- Then, general ATLAS concept:
  - data routed via switch
- Pixels: use DAQ HW also for calibration
  - Goes beyond pure data transport needs
  - Address scan control and data decoding (histogram) apects



routes data by IPaddr:port = logical stream

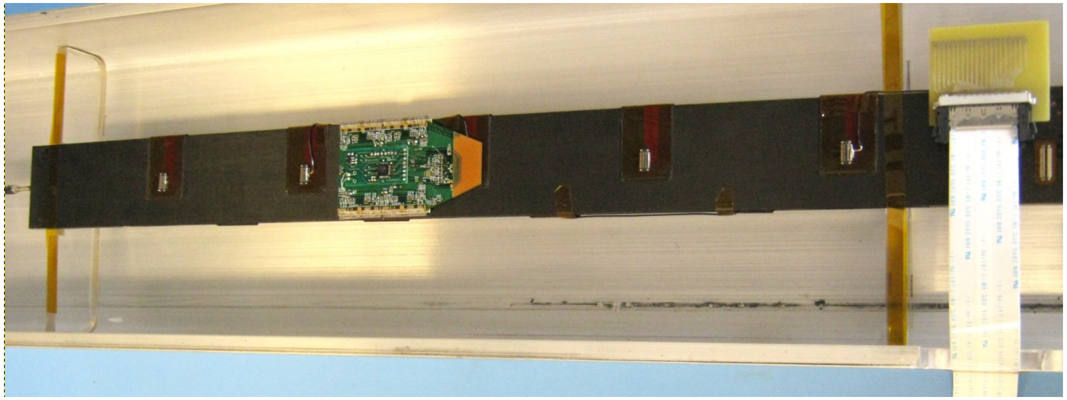
Routing map:
GBT id, E-link id, trigtype...
→ IPaddr:port

N x GBT links per FELIX @ 3.2Gb/s each

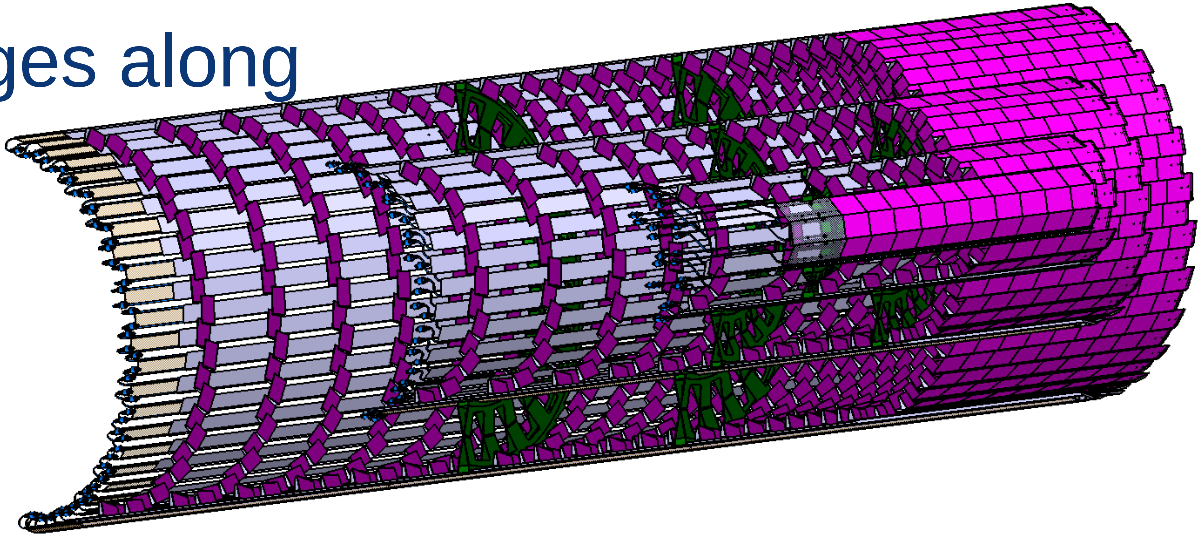
GBT E-links per function, per FE board

ITK Pixel Mechanics

- Developments on support structures
  - Example: Stavelets = shorter staves



- More dynamical layout, e.g. Alpine
  - Stave profile changes along longitud. direction, modules attached to inclined support



Summary

- HL-LHC ATLAS-Pixel development is picking up speed with more details under investigation
- Many challenges ahead:
  - New FE design with new technology
  - Decide on best sensor technology(ies?)
  - Many new aspects beyond module design: read-out, mechanics,...
- Schedule: “technical design review” in 2017