LHCb upgrade: Upstream Tracker

Macha Lake, Vertex 2014

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on behalf of the LHCb UT group

University of Zurich

September 15th, 2014

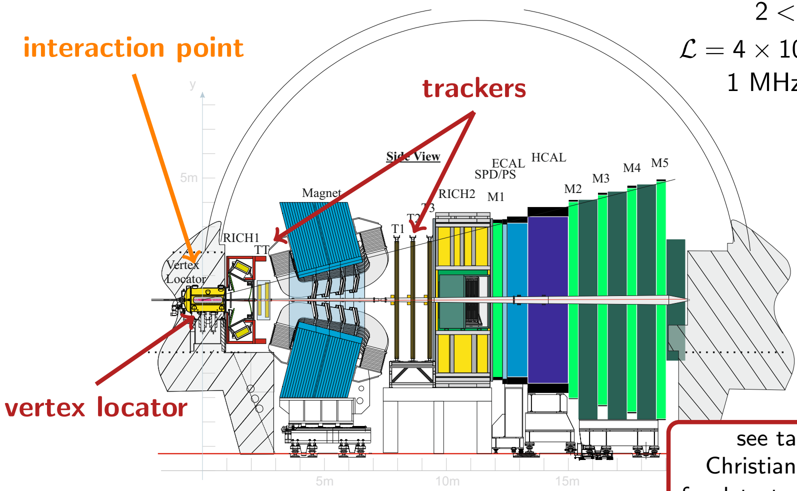
University of Zurich[UZH]

The current LHCb detector

$2 < \eta < 5$

$\mathcal{L} = 4 \times 10^{32}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}$

1 MHz readout



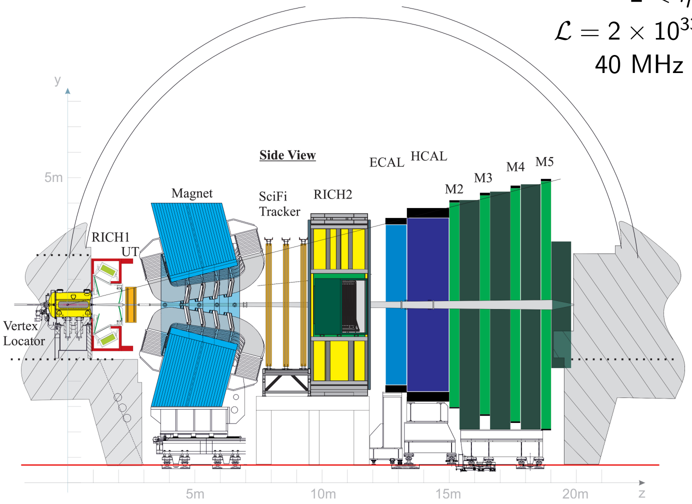
see talks from Christian and Espen for detector and tracking

The upgraded LHCb detector

$$2 < \eta < 5$$

$$\mathcal{L} = 2 \times 10^{33}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}$$

40 MHz readout



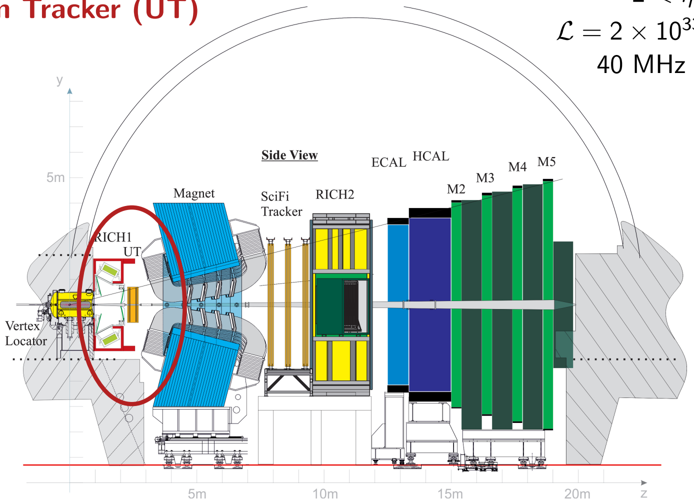
The upgraded LHCb detector

Upstream Tracker (UT)

$2 < \eta < 5$

$\mathcal{L} = 2 \times 10^{33}$ cm^{-2} s^{-1}

40 MHz readout

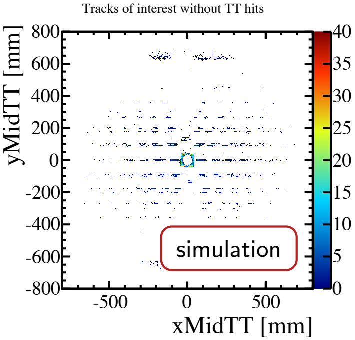


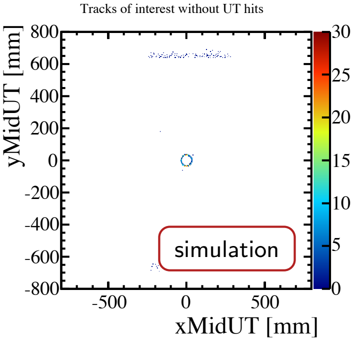
Motivations

- LHCb upgrade physics case $\Longrightarrow$ see Heinrich's talk
- Importance of UT in HLT tracking
  - fast estimate of momentum, $3\times$ speed up
  - improved acceptance coverage at small polar angles
- Higher luminosity
  - finer granularity to cope with increased particle density
- From 1 to 40 MHz readout
  - new front-end electronics
- Aim to collect 50 fb^{-1}
  - improved radiation hardness

Improved acceptance coverage

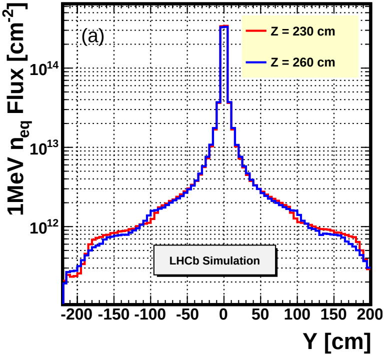
- Reduced beampipe clearance and insulating material
- Circular cut out of sensors around the beampipe
- Extrapolated track position
  for particles originating from beauty hadron decays

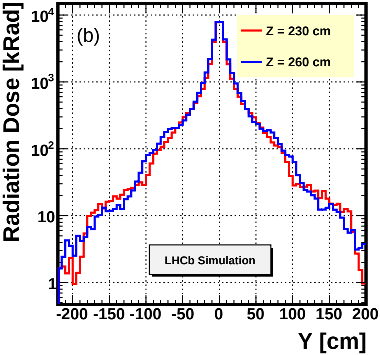




Irradiation constraints

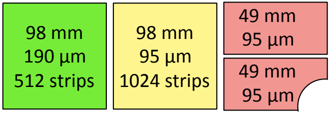
- After 50 fb^{-1}
  - max fluence 5×10^{14} 1 MeV n_{eq}/cm^2 } including safety factor
  - max radiation dose 40 MRad } including safety factor
  - keep $T_{sensor} < -5°C$
    in order to limit the bias voltage to $300 - 500$ V after irradiation

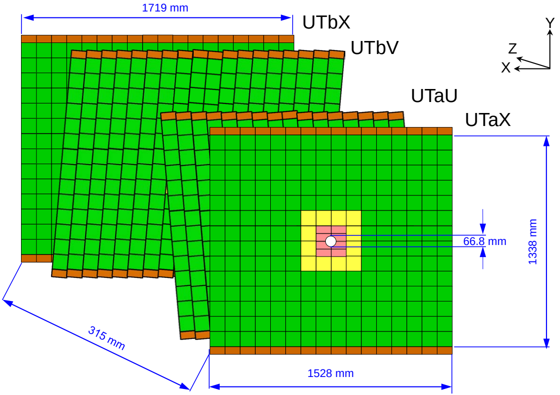




Geometry

- 4 planes inside light tight box flushed with N_2 or dry air
- Single-sided silicon microstrip sensors (strip pitch and length depending on position)
- Strips vertical on X, $\pm 5^\circ$ on U/V planes
- Circular cut out around the beampipe
- 68 **staves**, staggered 10 mm in z to provide overlap in x





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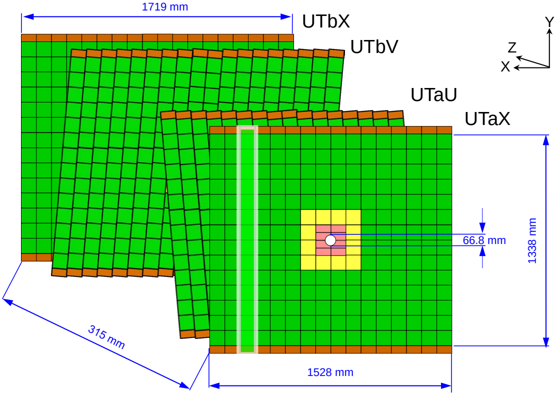
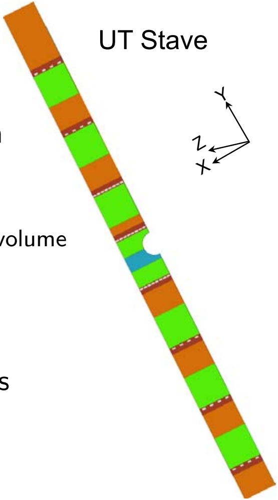


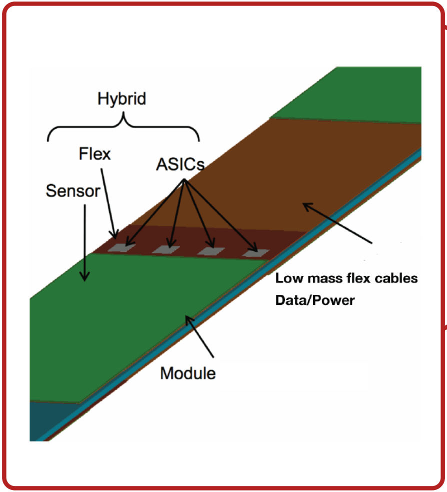
98 mm 190 µm 512 strips	98 mm 95 µm 1024 strips	49 mm 95 µm
		49 mm 95 µm

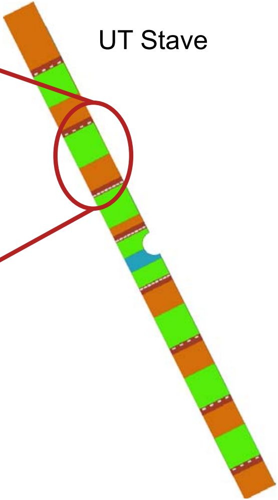
Stave

- Active detection area $97.28 \times 1336\ mm^2$
- 14/16 sensors mounted on both faces to provide overlap in y
- Data/power flex cables from top and bottom
- SALT ASIC close to sensor
  - $128 \times$ preamplifier, shaper, and ADC
  - zero suppression and serialisation to reduce data volume
- Active cooling needed
  - bi-phase CO_2
  - cooling pipes embedded in the staves
- Shorter strips than in TT $\Longrightarrow$ thinner sensors
  - 250 instead of 500 μm
- Total material budget similar to TT

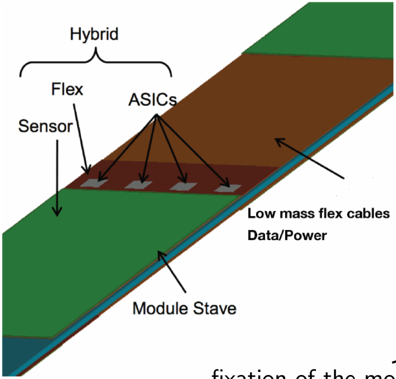


Stave - zoomed in

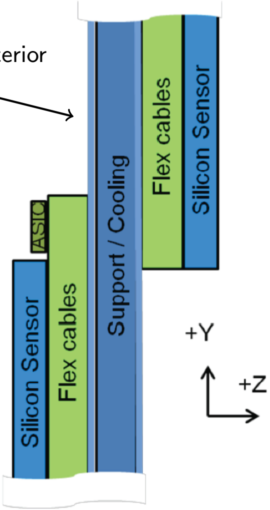




Mechanics and cooling



CFRP facing sheets surrounding foam core interior

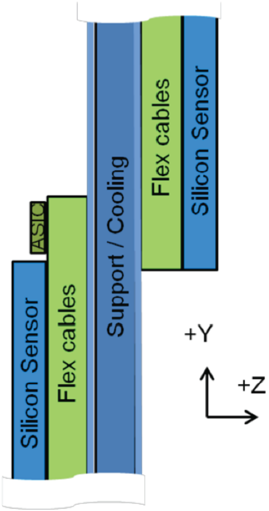


fixation of the module on the stave under discussion

Cooling

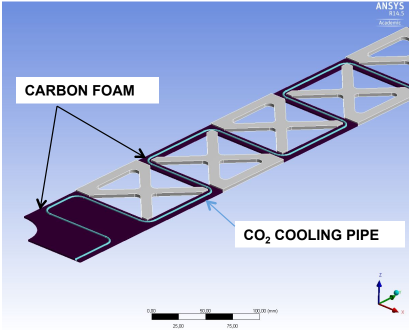
- Requirements
  - $T_{\text{sensor}} < -5^\circ\text{C}$
  - $\Delta T_{\text{sensor}} < 5^\circ\text{C}$
  - $T_{\text{ASIC}} < 40^\circ\text{C}$
  - low material budget
- Bi-phase CO_2 cooling system
  - thin-walled Ti cooling tubes, 2 mm inner diameter and 0.1 mm wall thickness
  - stainless steel as backup solution
- Heat load mainly due to ASICs

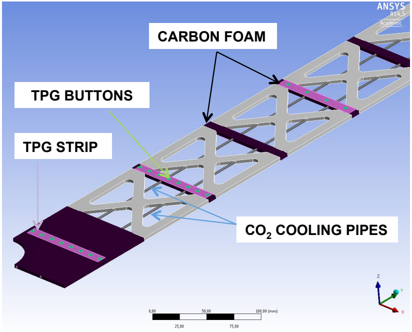
0.77 W/chip
900 W/plane
3.6 kW in total



Pipe design

- **Baseline: snake pipe**
  - pipe running underneath each row of ASICs
  - best thermal performance
  - to be validated with full stave prototypes
- **Backup: parallel pipe**
  - straight tubes combined with heat spreaders and thermal vias

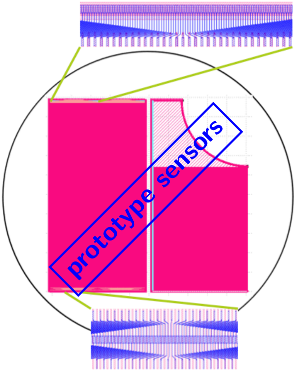




Sensors

- Single-sided silicon microstrip sensors
  - strip pitch and length depending on position
  - 250 μm thickness
  - n^+-in-p in the central region, p^+-in-n in the rest
- Read out by 4 or 8 ASICs
- Circular cut out of innermost sensors
- Embedded pitch adapter
  - from 190 to 73 μm pitch
  - reduce material budget and number of wirebonds
  - external glass pitch adapter also investigated

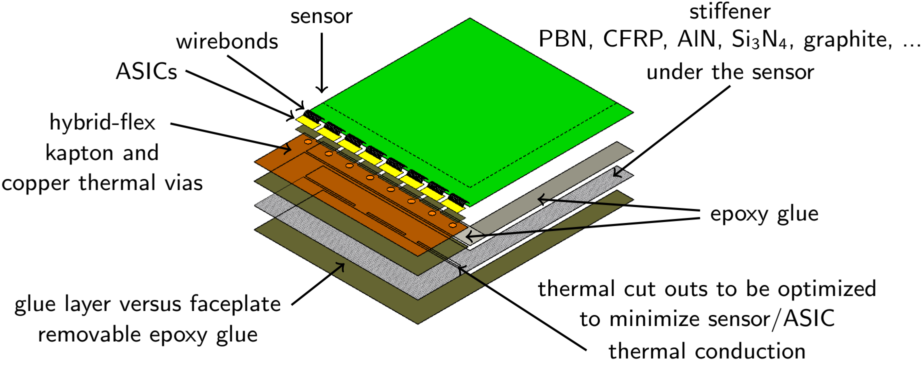
Type	Pitch (μm)	Length (mm)	Strips
A	190	97.28	512
B	95	97.28	1024
C	95	48.64	1024
D	95	48.64	1024



second metalization layer for type A sensors

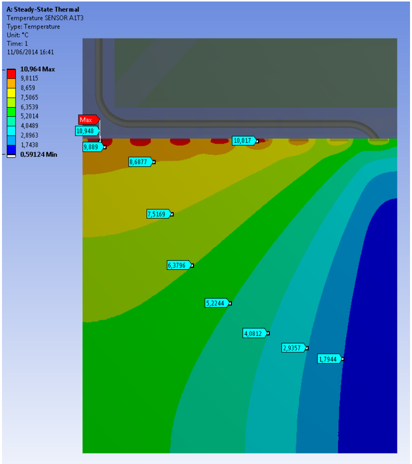
Modules

- Evolving design
  - facilitate handling during production and testing
  - allow to replace individual modules in case of failure

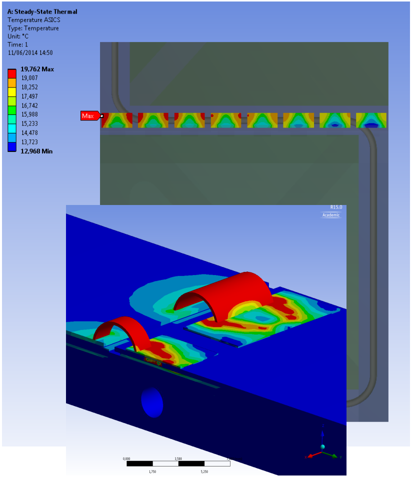


Thermal simulation

sensor temperature

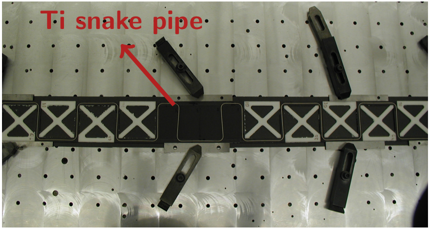


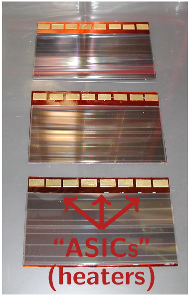
ASICs temperature

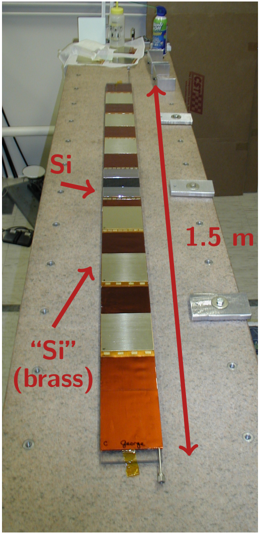


Stave prototyping

- First mechanical/thermal prototype completed
  - realistic stave materials (CFRP, foam core)
  - snake pipe design
  - Ti tube bent and epoxied into the stave
  - maximum heat load mimicked by heaters
  - successfully cooled down, well below -5°C on sensors
  - measurements ongoing, including deflection and thermal contraction



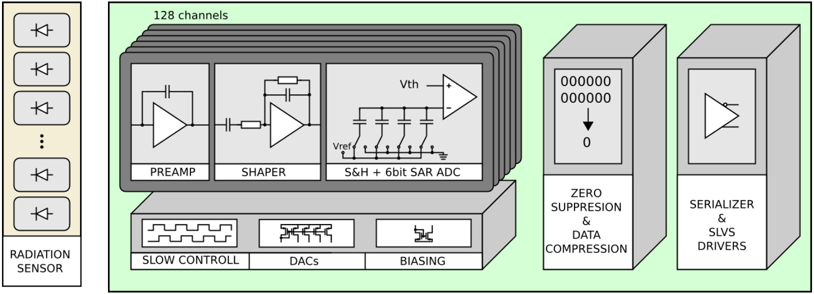




SALT ASIC

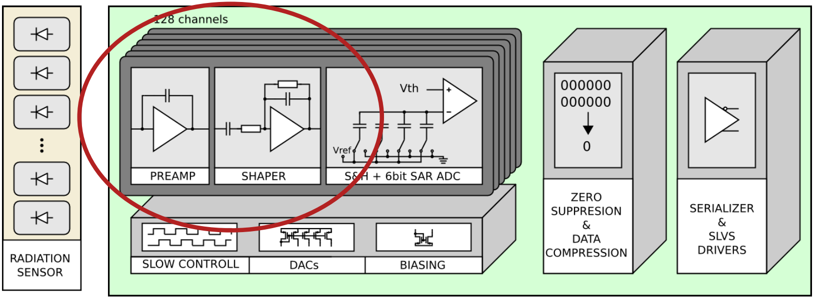
SALT = Silicon ASIC for LHCb Tracker

- 40 MHz readout
- 128 channels
- TSMC CMOS 130 nm technology
- 73 μm pitch on input pads



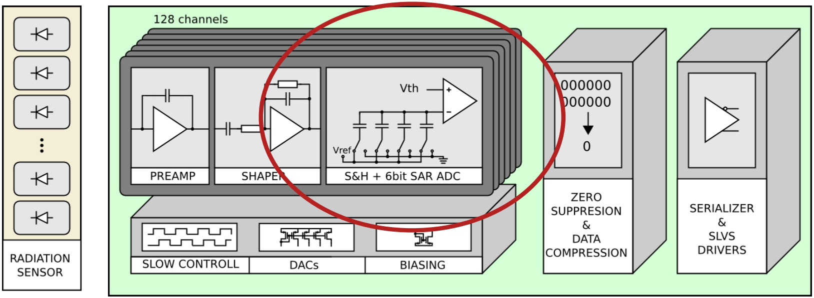
SALT ASIC - analog block

- Peaking time ~ 25 ns
- Remainder after $2\times$peaking time $\sim 5\%$ $\Longrightarrow$ minimise pile up, spill over
- Sensor capacitance $5 - 15$ pF
- Power consumption $1 - 2$ mW/channel
- Both polarities $\Longrightarrow$ n^+-in-p and p^+-in-n



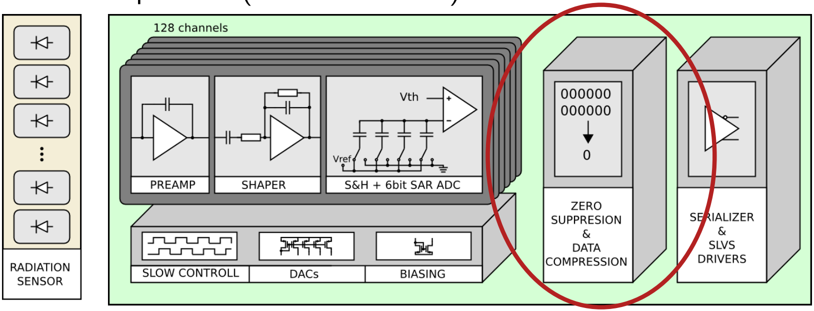
SALT ASIC - ADC

- SAR, 6 bit resolution
- power consumption < 0.5 mW at 40 MS/s



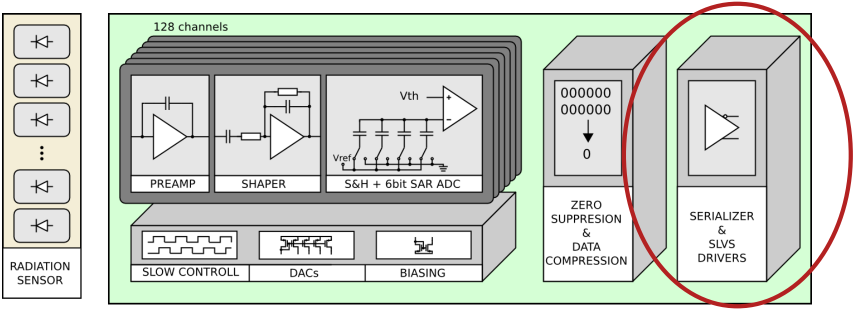
SALT ASIC - digital signal processing block

- Bad/noisy channel masking
- Pedestal subtraction
- Mean common mode subtraction
- Zero suppression
- Data compression (header and data)



SALT ASIC - serialisation

- Create and transmit data frames to peripheral electronics
- Serial links $\Longrightarrow$ e-links
  - 5 e-links per ASIC but $2-5$ active depending on sensor position
- SLVS I/O standard
- 320 MBit/s data rate



Flex cable

- Connect hybrids and peripheral electronics
- Run along the stave, up to 0.776 m long

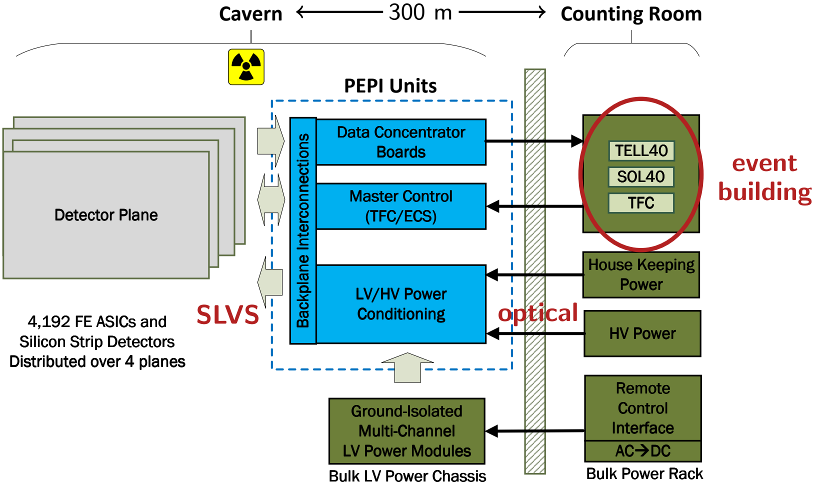
- Requirements
  - low material budget
  - low voltage drop
    $\Longrightarrow$ 0.5 V round trip drop
  - signal integrity
- First prototype design
  - 2 layers
  - kapton with copper traces
  - **signal**
  - **power**

- Prototypes ready to be tested by the end of September

traces terminated with bonding pads where hybrids will be mounted

Peripheral electronics

PEPI = periphery electronics processing interface



Test beam activities

- Prototype sensors
  - irradiated with different doses, up to 20 MRad
  - to be tested in Oct/Nov 2014 test beam at SPS
- SALT ASIC not yet ready

  $\Longrightarrow$ Beetle-based readout system (Alibava)
  - commissioned during exploratory test beam in Jul/Aug 2014
  - synchronized with Timepix telescope offline
- Prototype sensors with circular cut out expected by end of 2014
- SALT ASIC-based readout system in 2015 test beam
- In parallel, laser test stands in Zurich and Syracuse

Planning

- R&D $\Longrightarrow$ 2014-2016
- Production and testing $\Longrightarrow$ 2015-2018
- Installation $\Longrightarrow$ Q_1 2019

Summary

- 40 MHz readout $\Longrightarrow$ importance of UT in HLT tracking
- Main design goals
  - finer granularity
  - improved acceptance coverage at small polar angles
  - low material budget
  - radiation hardness, n^+-in-p sensors in the central region
- CO_2 distributed cooling system embedded in the staves
- R&D and validation of design choices underway
- TDR submitted and approved

  CERN-LHCC-2014-001, LHCB-TDR-015

Participating institutes

CERN

INFN
Istituto Nazionale
di Fisica Nucleare

University of
Zurich UZH

UNIVERSITY OF
Cincinnati

AGH

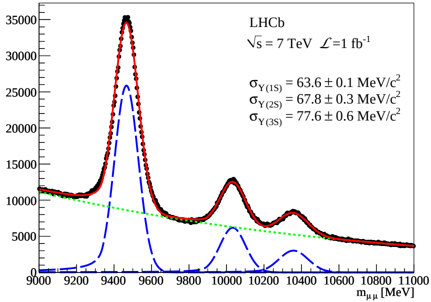
Thanks for the attention

Spare slides

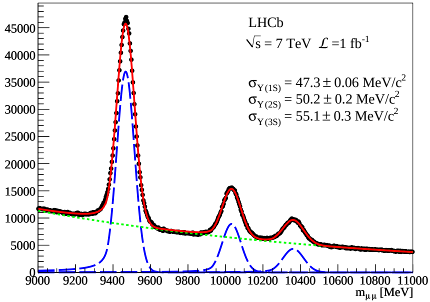
Physics goal of TT/UT

- Reconstruct K_S^0 and Λ decaying after the VELO
- Improve momentum resolution by adding TT/UT hits to tracks

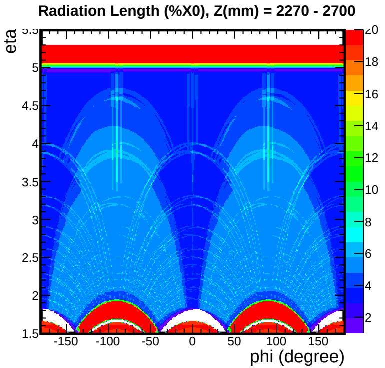
without TT hits

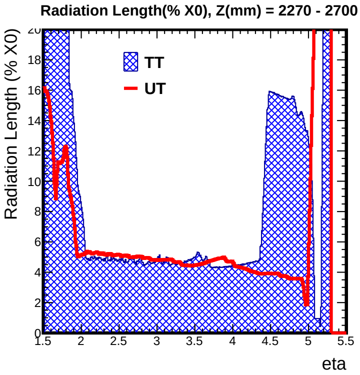


with TT hits



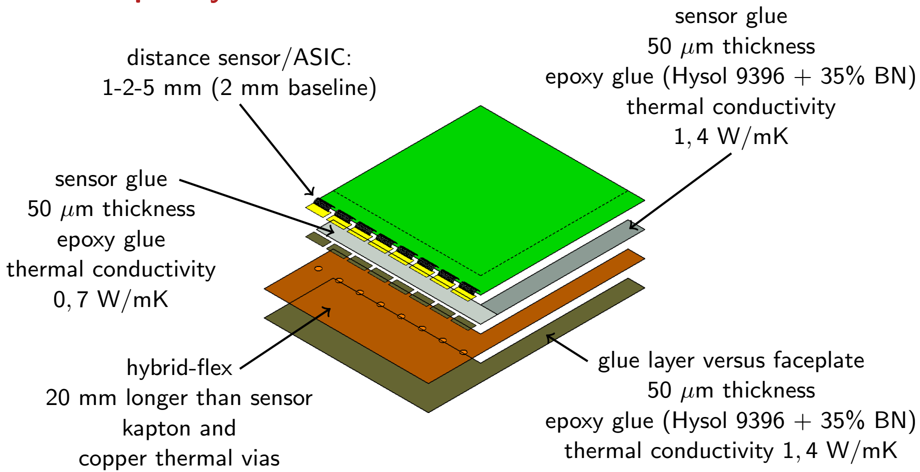
Material budget



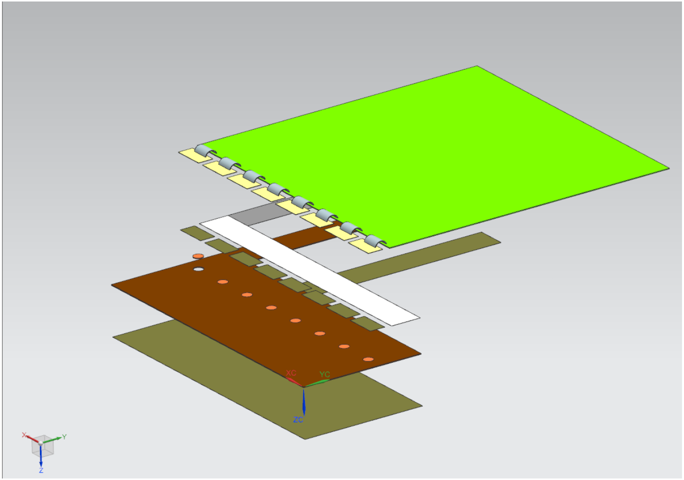


Modules

- **L-shaped hybrid**

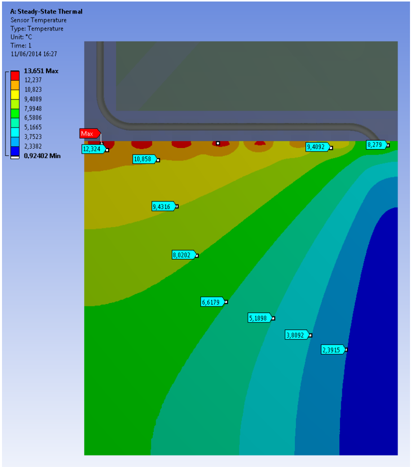


L-shaped hybrid

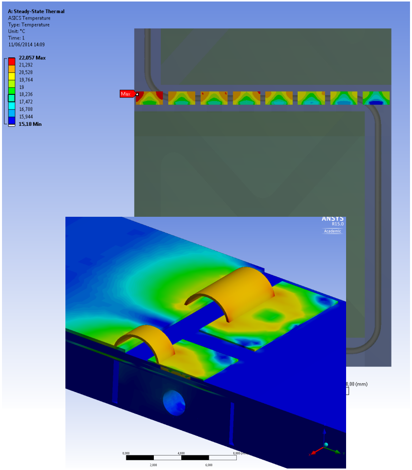


L-shaped hybrid thermal simulation

sensor temperature

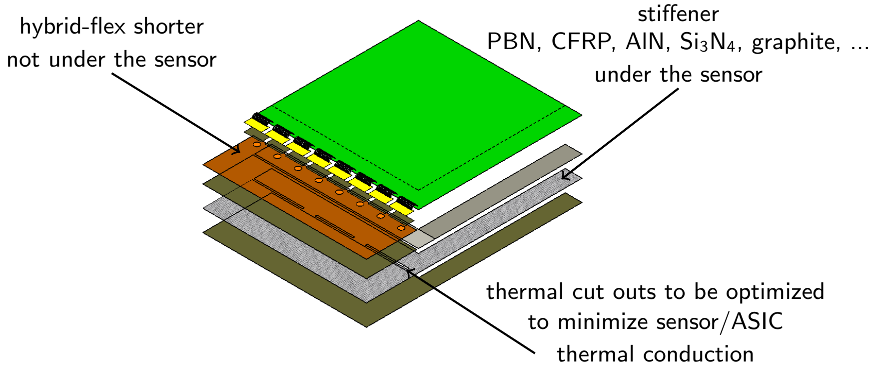


ASICs temperature

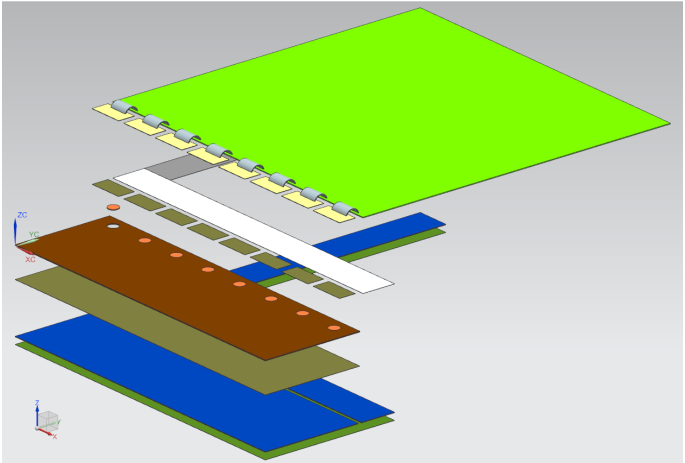


Modules

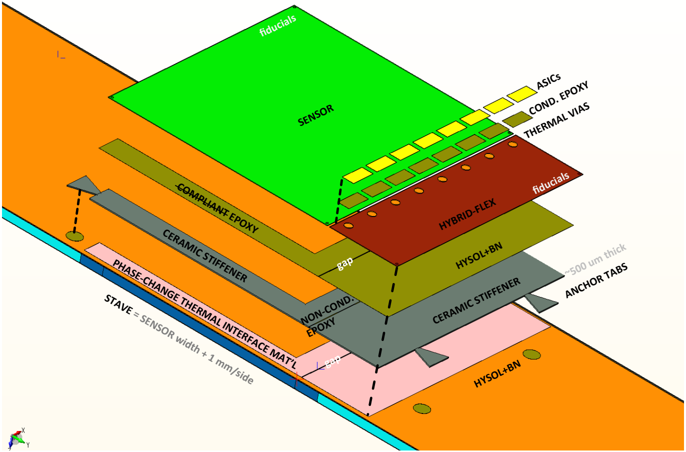
- **Short hybrid + stiffener**



Short hybrid + stiffener

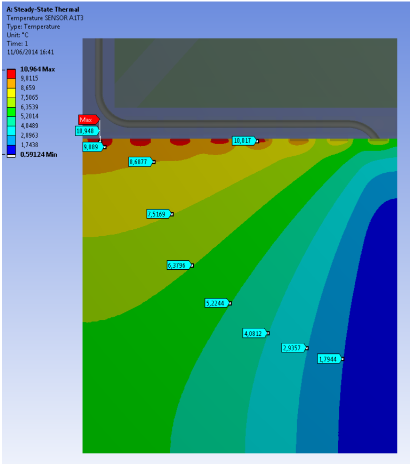


Short hybrid + stiffener - latest version

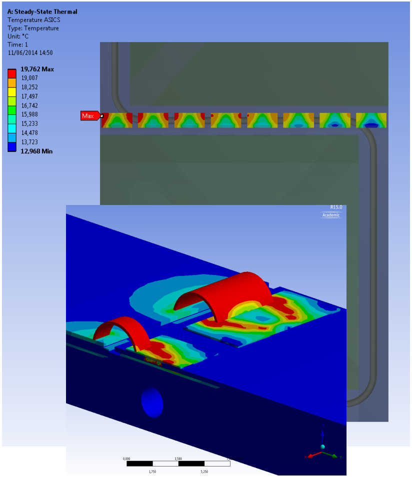


Short hybrid + stiffener thermal simulation

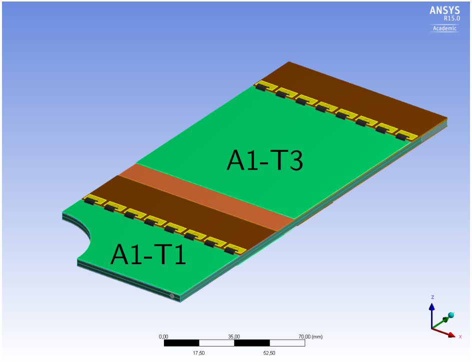
sensor temperature

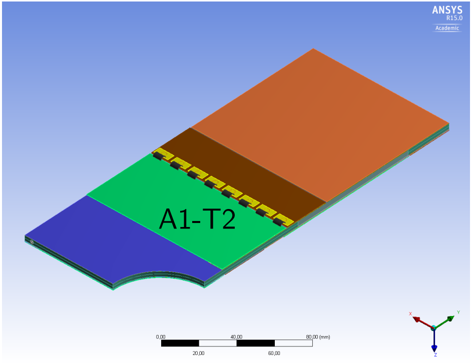


ASICs temperature

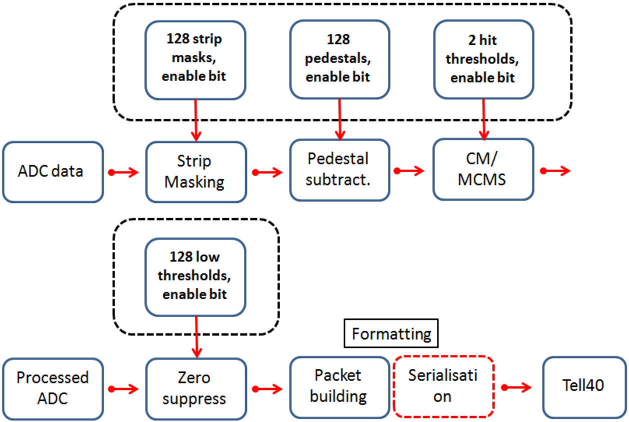


Modules used in the thermal simulation





SALT ASIC - baseline digital signal processing chain

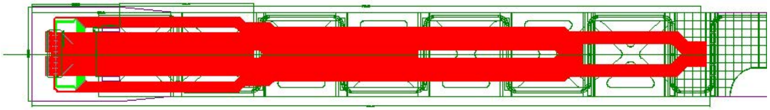


Flex cable

- Connect hybrids and peripheral electronics
- Run along the stave, up to 0.776 m long

- Requirements
  - low material budget
  - low voltage drop
  - signal integrity
- First prototype design
  - 2 layers on-stave, 4 layers off-stave
  - rectangular shape, 97 mm wide
  - central axial symmetry
  - 0.5 V round trip drop

layer	material	thickness (μm)
top	copper	18
dielectric 1	polyamide	100
inner 1	copper	18
dielectric 2	polyamide	100
inner 2	copper	18
dielectric 3	FR-4	1200
bottom	copper	18

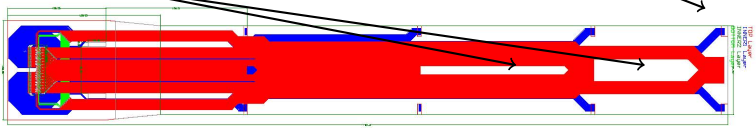


Flex cable - first prototype design

- Design
  - **Signal traces**
  - **Power traces**
  - 150/100 μm trace/space width
  - FCI MEG-Array connector
- Prototypes ready to be tested by the end of September

vias to access power from the top

cuts to improve thermal contact



traces terminated with bonding pads where hybrids will be mounted

Stave power distribution

- Hybrids connected in local power groups
  - each quadrant divided in 4 power groups
  - 1 dedicated MARATON channel per power group
  - each power group with isolated ground reference

quadrant of UTa plane

Quadrant of the UTa plane style:

FE ASICs

	0	1	2	3	4	5	6	7	Per Pwr Grp # of FE ASICs	Per Pwr Grp Total Current (Amps)	
0	4	4	4	4	4	4	4	4	64	34.112	Power Group 4
1	4	4	4	4	4	4	4	4			
2	4	4	4	4	4	4	4	4	64	34.112	Power Group 3
3	4	4	4	4	4	4	4	4			
4	4	4	4	4	4	4	4	4	56	29.848	Power Group 2
5	8	8	4	4	4	4	4	4			
6	8 8	8	4	4	4	4	4	4	64	34.112	Power Group 1
										132.18	

quadrant of UTb plane

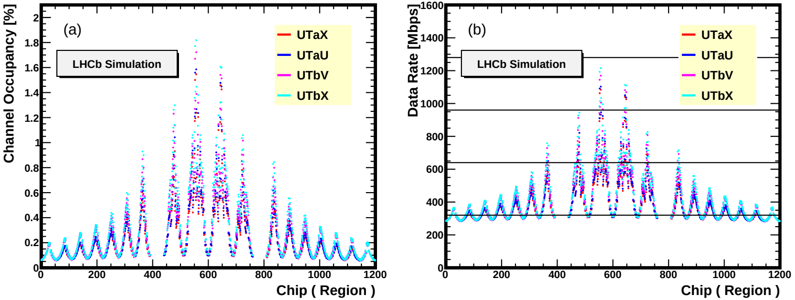
Quadrant of the UTb plane style:

FE ASICs

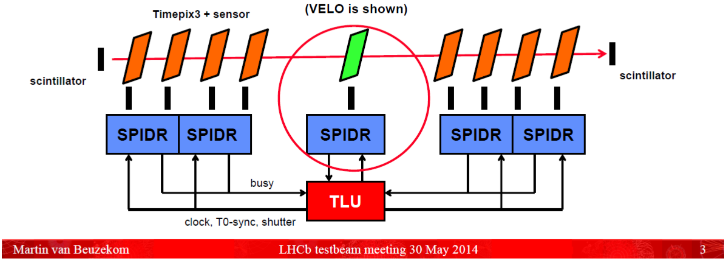
	0	1	2	3	4	5	6	7	8	Per Pwr Grp # of FE ASICs	Per Pwr Grp Total Current (Amps)	
0	4	4	4	4	4	4	4	4	4	72	38.376	Power Group 4
1	4	4	4	4	4	4	4	4	4			
2	4	4	4	4	4	4	4	4	4	72	38.376	Power Group 3
3	4	4	4	4	4	4	4	4	4			
4	4	4	4	4	4	4	4	4	4	64	34.112	Power Group 2
5	8	8	4	4	4	4	4	4	4			
6	8 8	8	4	4	4	4	4	4	4	68	36.244	Power Group 1
											147.108	

Occupancy

- From minimum bias simulation at $\mathcal{L} = 2 \times 10^{33}$ cm^{-2} s^{-1}, $\sqrt{s} = 14$ TeV
  - average #hits/event = 1000
  - average cluster size = 1.44
  - average occupancy = 1.8%

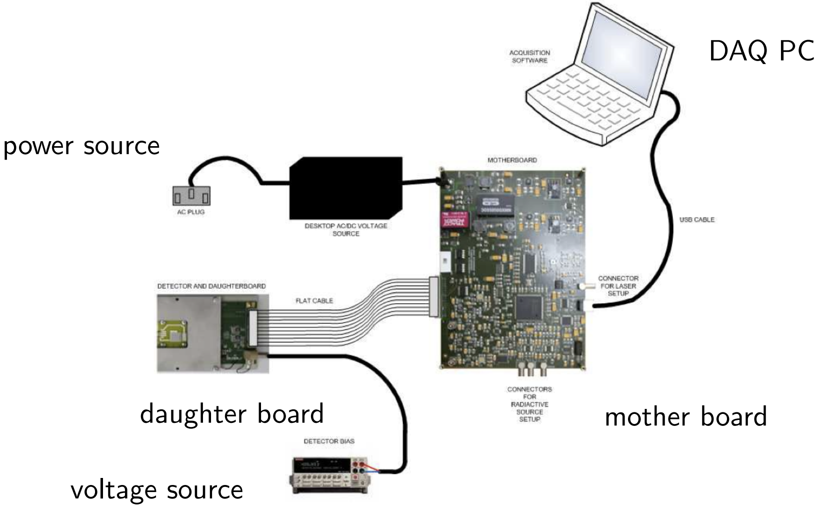


Timepix telescope



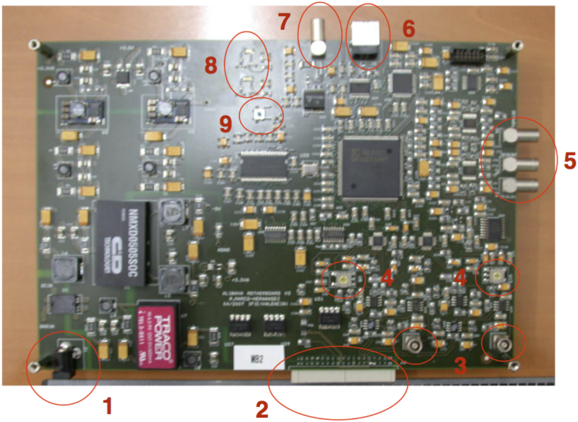
- 8 planes
  - 4 upstream and 4 downstream of the detector under test (DUT)
- Triggerless mode, data-driven
- 1 DAQ PC per plane, recording data continuously
- Offline software (Kepler) to merge data from different planes/files

Alibava system



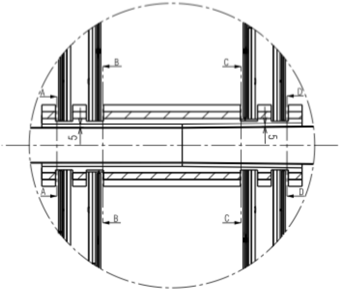
Mother board

1. 1 power connector
2. 1 flat cable connector
3. 2 vertical LEMO connectors
   (output signal oscilloscope)
4. 2 switches of 3 pos
   (modify ADC input range
   of Beetle chips:
   -1024, ± 512, or 1024 mV)
5. 3 LEMO connectors
   (trigger input)
6. 1 USB connector
7. 1 LEMO connector
   (trigger output)
8. 1 red LED
9. 1 reset button



Region around the beampipe (TT)

- 5 mm clearance between beampipe and insulation walls



Cut along the beampipe
Scale 1:5