Upgrades of CMS inner tracker for HL-LHC (pixels)

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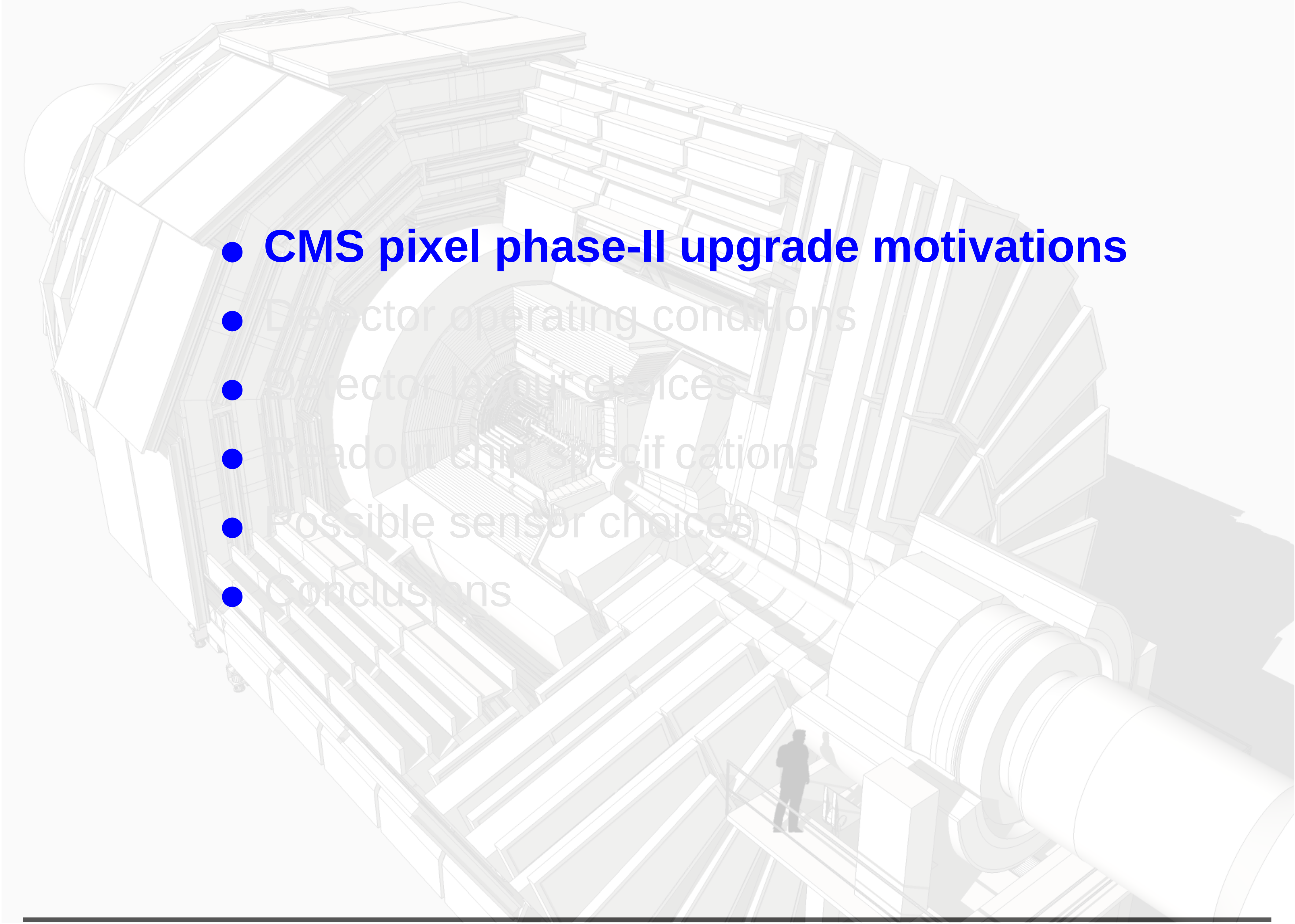
Introduction

- CMS pixel phase-II upgrade motivations
- Detector operating conditions
- Detector layout choices
- Readout chip specifications
- Possible sensor choices
- Conclusions



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Phase II upgrade motivations

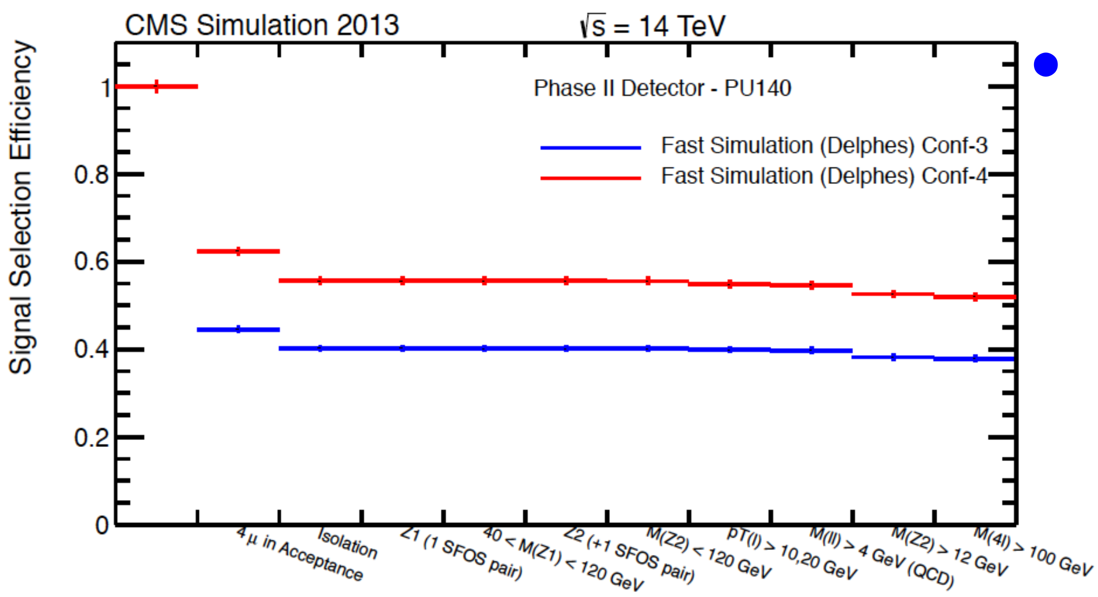
Major achievement of LHC: Higgs discovery in 2012!

That's not the whole story, are other questions that need to be answered

- Need to investigate the entire Higgs sector
  - Higgs coupling and property measurements;
  - Di-Higgs searches with the aim of Higgs self coupling measurement;
  - Vector Boson Scattering (VBS) measurements (crucial forward tagging jets).
- Standard Model (SM) measurements
  - Precision measurements (e.g. M_W, $\sin\theta_W$, α_s)
  - Search for rare SM processes, enhanced by BSM (e.g. $B_{s,d} \rightarrow \mu\mu$)
  - Differential measurements of W, Z, di-boson, Top

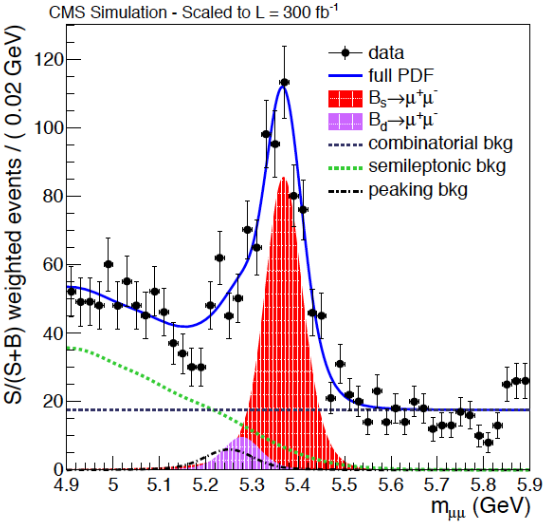
Luminosity	300/fb	3000/fb
Coupling parameter	7-parameter fit	
k_γ	5-7%	2-5%
k_g	6-8%	3-5%
k_W	4-6%	2-5%
k_Z	4-6%	2-4%
k_u	14-15%	7-10%
k_d	10-13%	4-7%
k_l	6-8%	2-5%
Γ_H	12-15%	5-8%

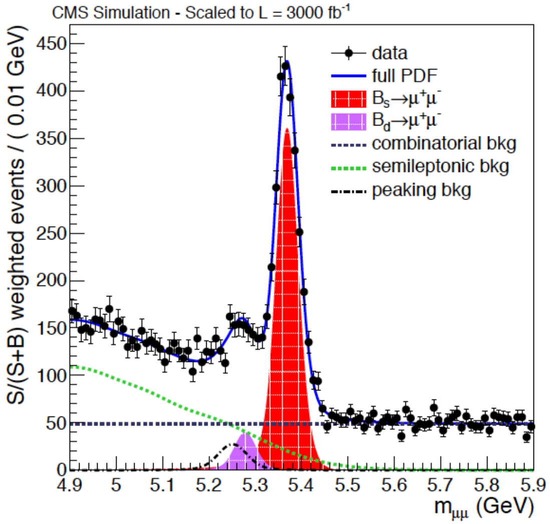
Phase II upgrade, some motivations



- Efficiency cut flow for **H** $\rightarrow$ **ZZ** $\rightarrow$ $\mu\mu\mu\mu$
  - Conf-3: sub-detectors have same angular acceptance as current version, but central tracking detector and the forward electromagnetic calorimeters are replaced and improved
  - Conf-4: tracking, electromagnetic and hadronic calorimetry, and muon detector, are increased in acceptance up to $\eta \sim 4$.

- $B_{s/d} \rightarrow \mu\mu$ mass resolution for 300/fb and 3000/fb
  - Improvement in mass resolution for the 3000/fb projection expected from *improved inner tracking system* and by removing end-cap candidates





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HL – LHC environment

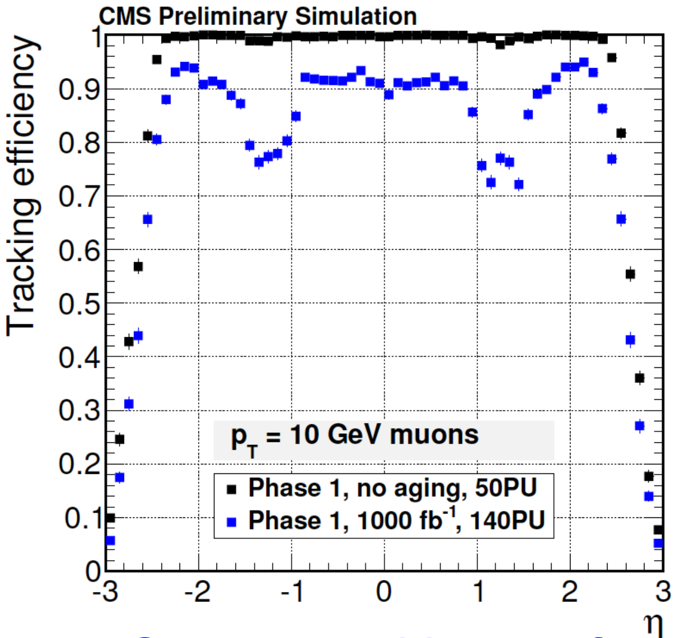
LHC						HL-LHC	
Run1 $8x10^{34}\ s^{-1}cm^{-2}$ 30/fb E=7-8 TeV BX=50ns <PU>~20-30	**LS1**	**Run2** $2x10^{34}s^{-1}cm^{-2}$ 300/fb E=13-14 TeV BX=25ns <PU>~50	**LS2**	**Run3** $2x1034s^{-1}cm^{-2}$ 300fb E=14TeV BX=25ns <PU>~50		**LS3**	**PostLS3** $5x10^{34}s^{-1}cm^{-2}$ 3000/fb E=14TeV BX=25ns <PU>~140

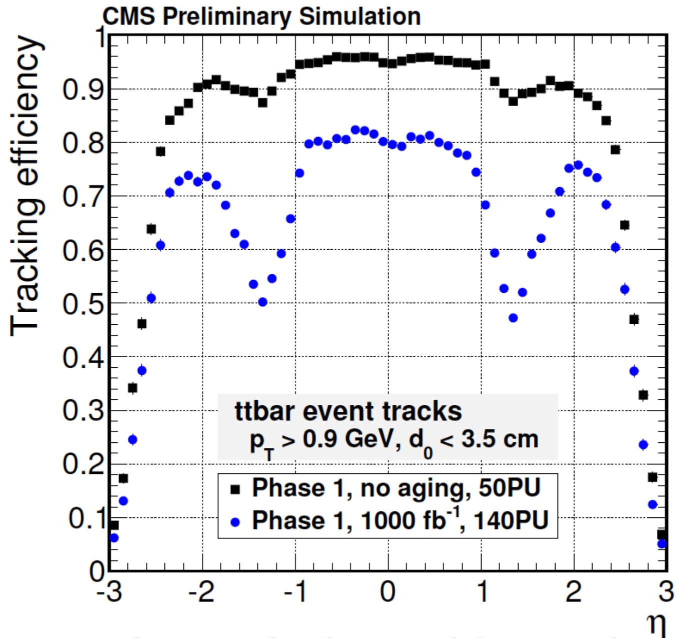
past	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	future

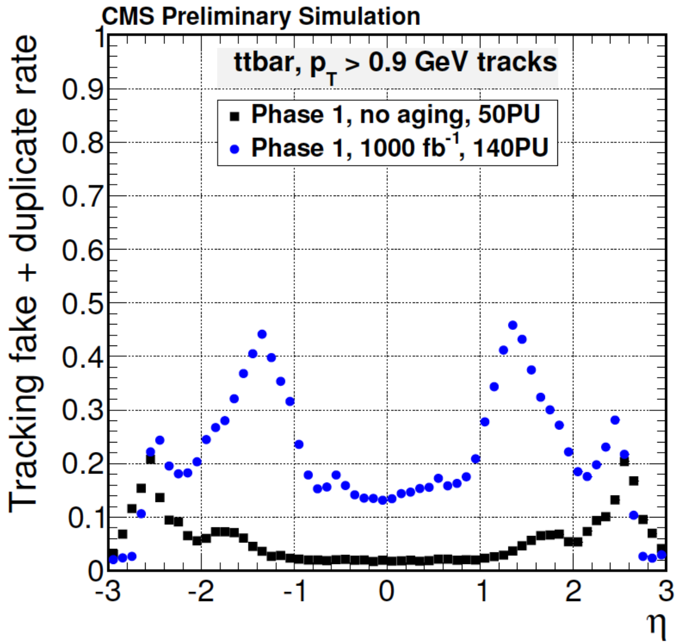
- High Luminosity (HL) - LHC: upgrade damaged low-β triplets and install crab-cavities to optimise bunch overlaps
- √s = 14 TeV!
- $L_{inst} = 5x10^{34}\ cm^{-2}\ s^{-1}$ (➔ ~10 times now) i.e. L_y = 250 fb^{-1} / year (L_{total} ~ 3000 fb^{-1} in 10 years)
- 25ns bunch spacing and <PileUp> = 140 (→ now 25)
- Radiation @30 mm from IP: $2x10^{16}\ n_{eq}\ /\ cm^2$ (→ ~10 times Phase-I)!
- Dose @30 mm from IP: 10 MGy (1 Grad)!
- Hit rate: ~2 GHz / cm2 (➔ ~10-20 times current one)

Huge R&D is required to cope with harsh environment

Pixel Detector operating conditions







- Overall tracking performance degradation with ageing:
  - After 500 fb^{-1} impact parameter degradation of more than 50%;
  - <PU> = 140 imply an irreducible data loss of ~7%.
- Effects on the physics program:
  - Efficiency loss diminishes effectiveness of high-p_T lepton isolation, and degrades jet energy and missing transverse energy resolution!
  - Fake tracks cause biases and resolution degradation in jet energy measurements, increase background levels, and adversely affect high-p_T lepton isolation criteria.

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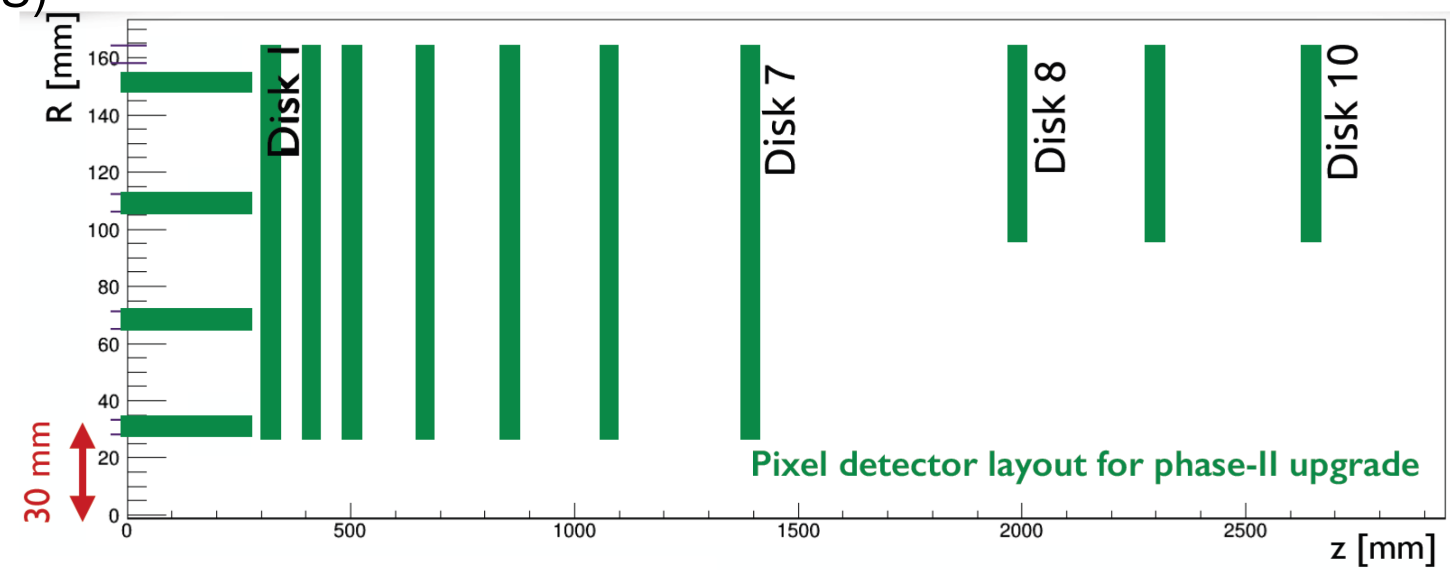
Pixel detector layout choices

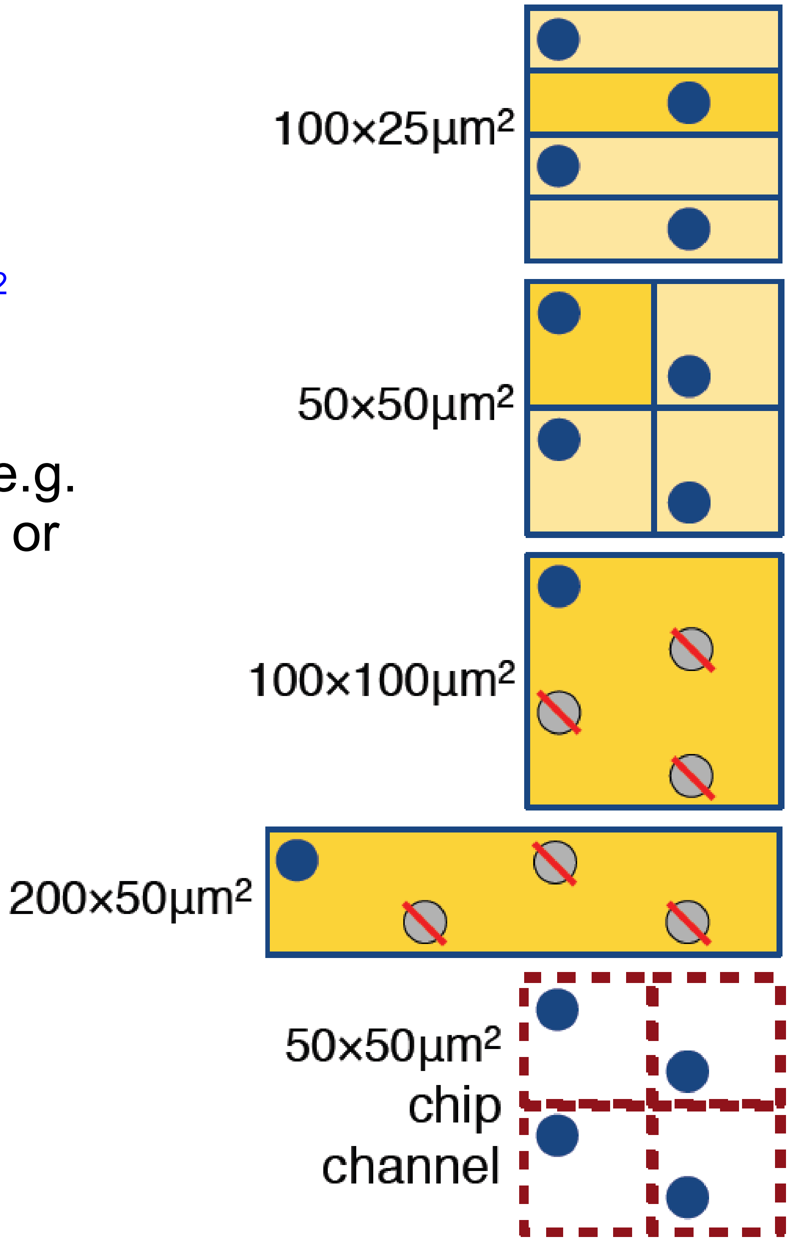
- **Improve resolution at high-p_T** and improve two-track separation → increase granularity (*present tracker has degraded track finding performance in high-energy jets due to hit merging in the pixel detector*)
- **Improve resolution at low-p_T** and reduce secondary interactions → reduce material
- **Increase forward acceptance** (*to cover peak production region of jets from Vector Boson Fusion and and VBS, among highest priorities of the physics program, by mitigating PU effects in jet-ID and energy measurement*)
    - 4 barrel layers (→*3 layers now*)
    - 10+10 forward disks, covering up to $\eta \simeq 4$ *(2+2 disks now, up to $\eta \simeq$ 2.4)*
- **Preserve "ease-to-access" of current detector** (*possibility to replace degraded parts during TS*)



Basic Pixel Detector design concepts

Sensor pixel cell size:

- Aim to large chip: ~20x20 mm^2 (current FEI4 dimensions)
- Readout chip channel size: 50x50 μm^2
- Target sensor cell: 50x50 μm^2 or 25x100 μm^2
- Staggered bumps:
  - possibility to switch off 1/2 or 3/4 pixels (e.g. outer regions with pixels of 100x100 μm^2 or 50x200 μm^2)



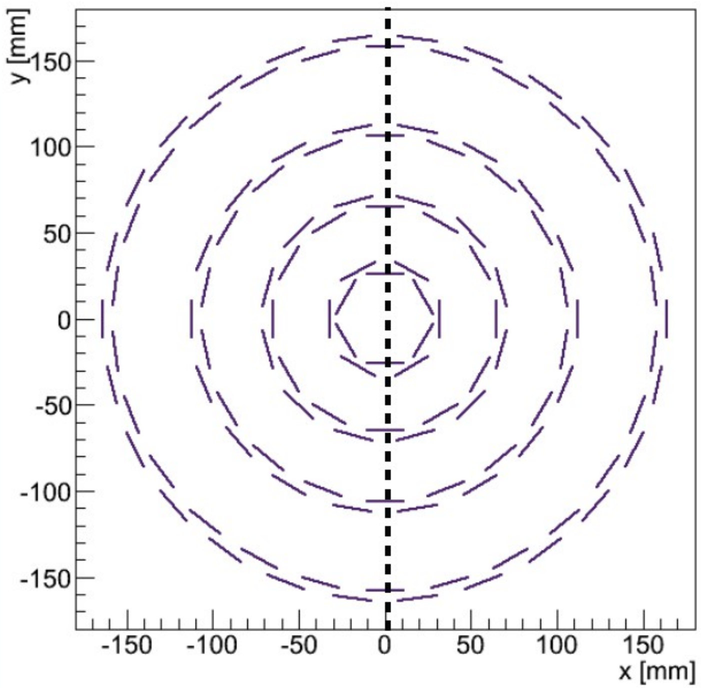
Readout chip:

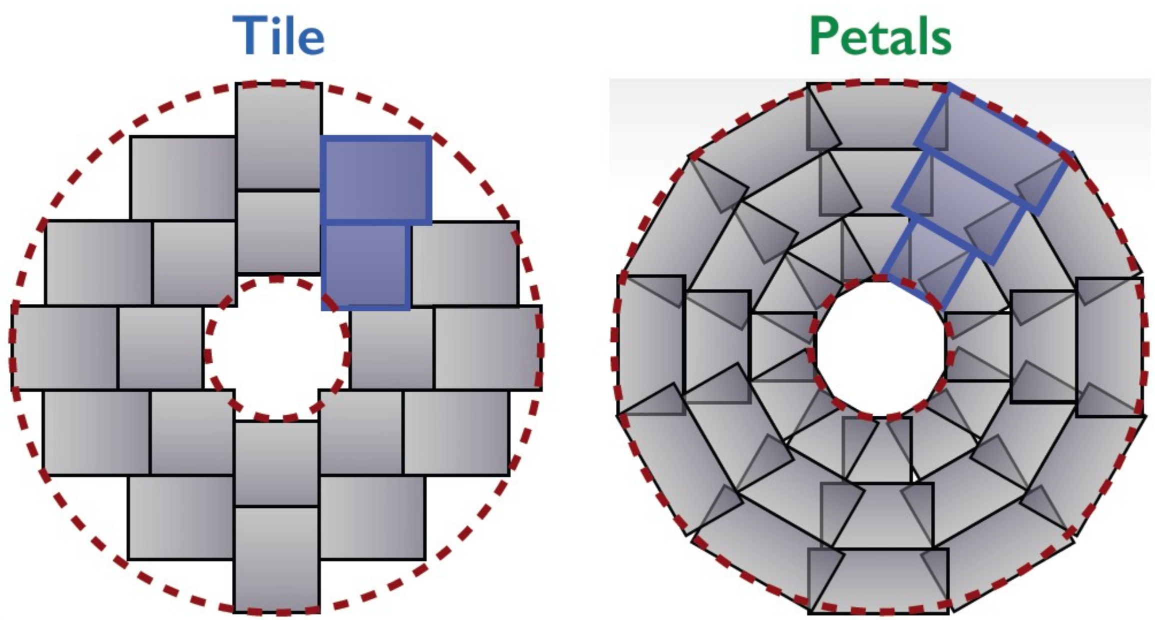
- Candidate technology: 65 nm CMOS (RD-53 cross-collaboration Atlas-CMS for development)

Total active area
~ 4 m^2 (1.5 x Phase1)

Pixel Detector Layout studies

- **Barrel Geometry**: two module types with 4x2 or 4x1 chips and *no projective hole at z=0*
- **Forward Geometry**: two possible coverage schemes considered

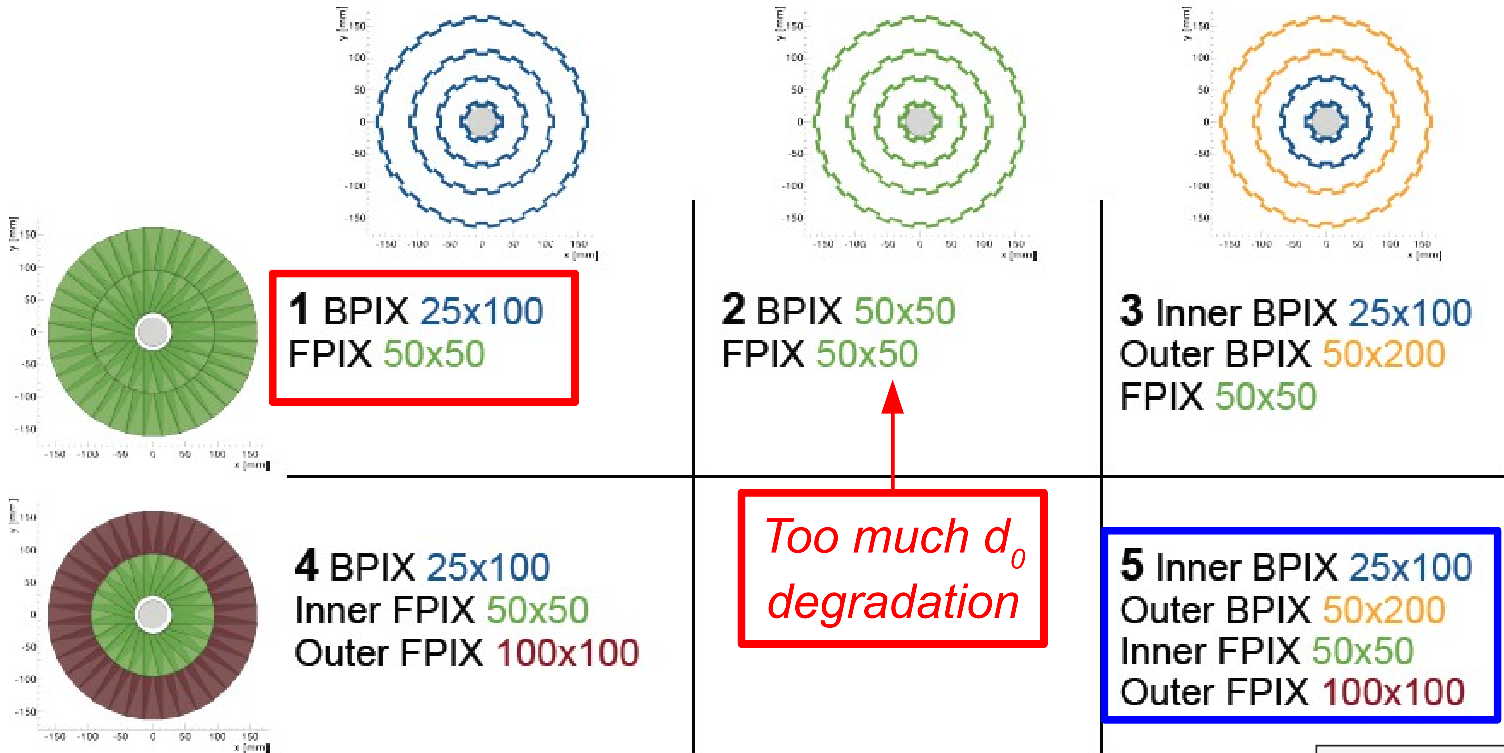




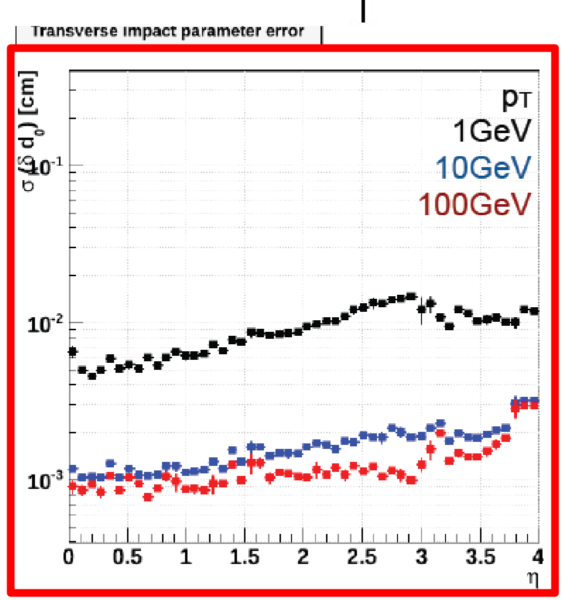
Geometry	Coverage	Overlap	# modules	# chips
Tiles	89%	12%	26	160
Petals	98%	45%	44	232

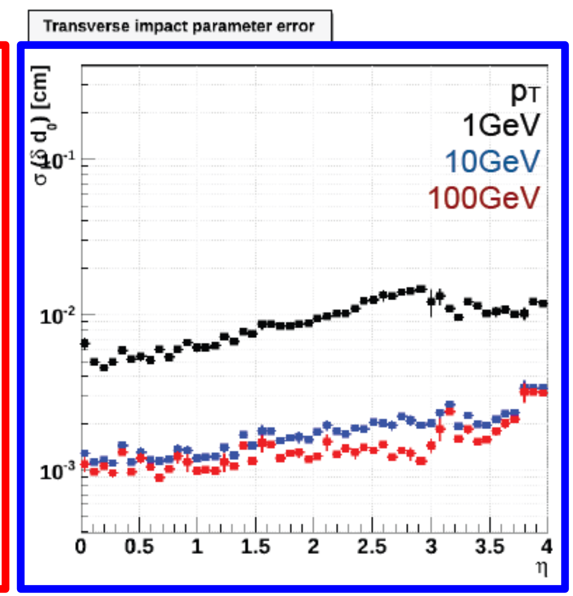
- **Numbers/layer**
- Tile modules: 4x2,4x1,2x2
- Petal modules: 4x2, 2x1
- **Chip size 21x23 mm² active area**

Pixel detector layout studies



- Pixel cell size studies
- *Too much d_0 degradation with pure squared pixels in BPIX*;
- Two extreme configurations, #1 and #5, have comparable tracking performance;
- Config. #5 has ~1/2 channels of #1!





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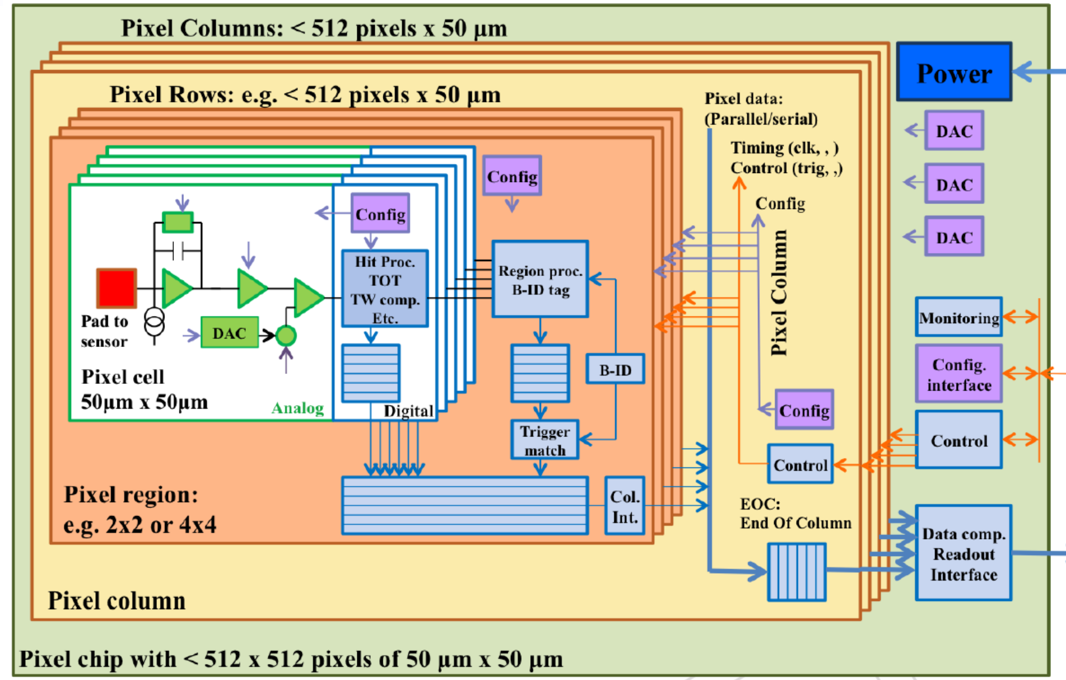
Pixel Readout Chip specifications

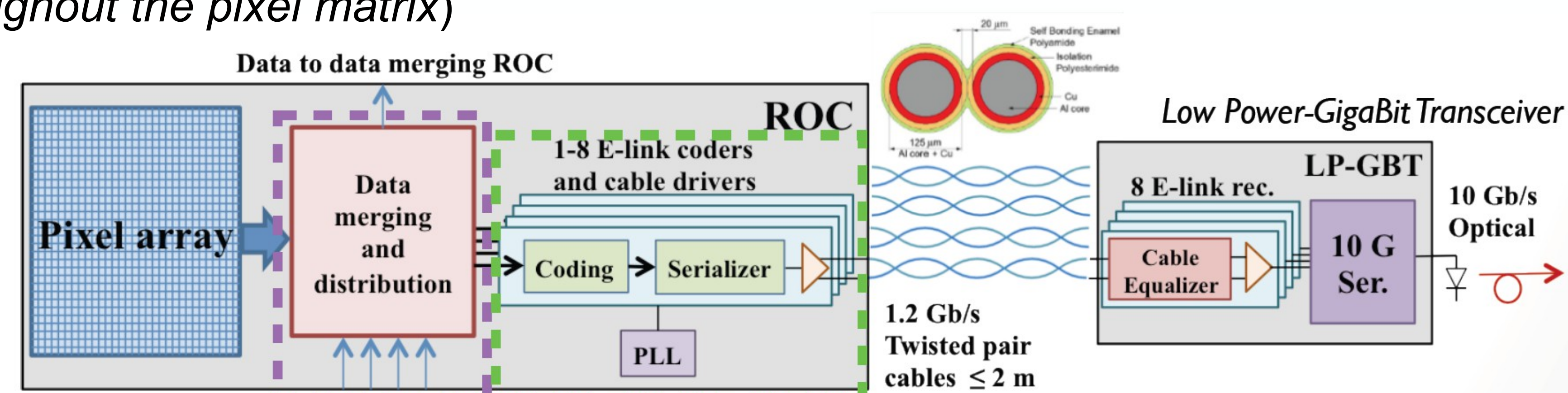
Generation	Present	Phase-I	Phase-II
Pixel size	100x150 μm^2	100x150 μm^2	50x50 (25x100) μm^2
Sensor, Thickness	2D, 285 μm	2D, 285 μm	thin 2D, 3D
Chip size	8x10mm^2	8x10mm^2	> 20x10 mm^2
Transistor	1.3x10^6		~10^9
Hit rate	100 MHz / cm^2	400 Mhz/ cm^2	**~ 2 GHz / cm^2**
Hit memory per chip	0.1 Mb	1 Mb	**~ 16 Mb**
Trigger rate	100 kHz	100 kHz	**~ 1 MHz**
Trigger latency	3.2 μs	3.2 μs	~ 12 μs
Readout rate	40 Mb/s	400 Mb/s	~ 2 Gb/s
Radiation	15 Mrad, r=42 mm L = 150 fb^{-1}	120 Mrad, r=29 mm, L = 500 fb^{-1}	**1 Grad, r=30mm, L = 3000 fb^{-1}**
Technology	250 nm	250 nm	**65 nm**
Architecture	Analog	Digital	Digital
Buffer location	End of Column	End of Column	Pixel
Power	~ 0.15 W/ cm^2	~ 0.15 W / cm^2	~ 0.3 – 0.5 W / cm^2

Pixel readout chip and data link specifications

- Possibility to tune bias currents of analogue front-end to account for different sensor choices

- Digital hit processing, including trigger latency buffer, implemented in pixel regions (e.g. 2x2 or 4x4pixels) followed by data merging, formatting and readout after the first level trigger accept (*price of local digital processing: digital noise injection into the front end to be controlled. Clocks and trigger signals must be distributed throughout the pixel matrix*)



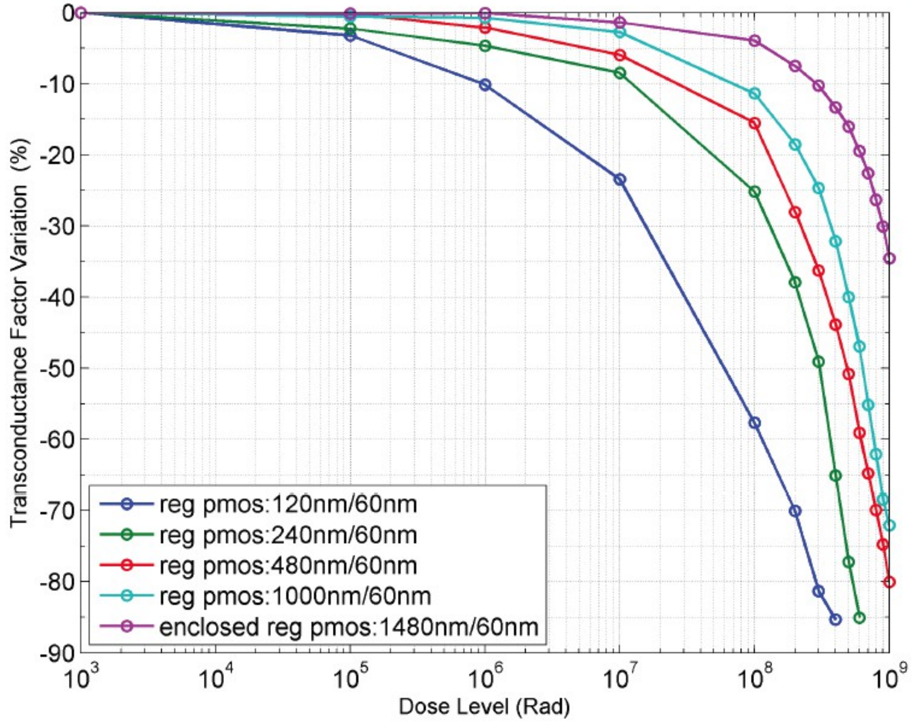


The chip will also implement data merging functionality (from 2 or even 4 chips in the innermost region)

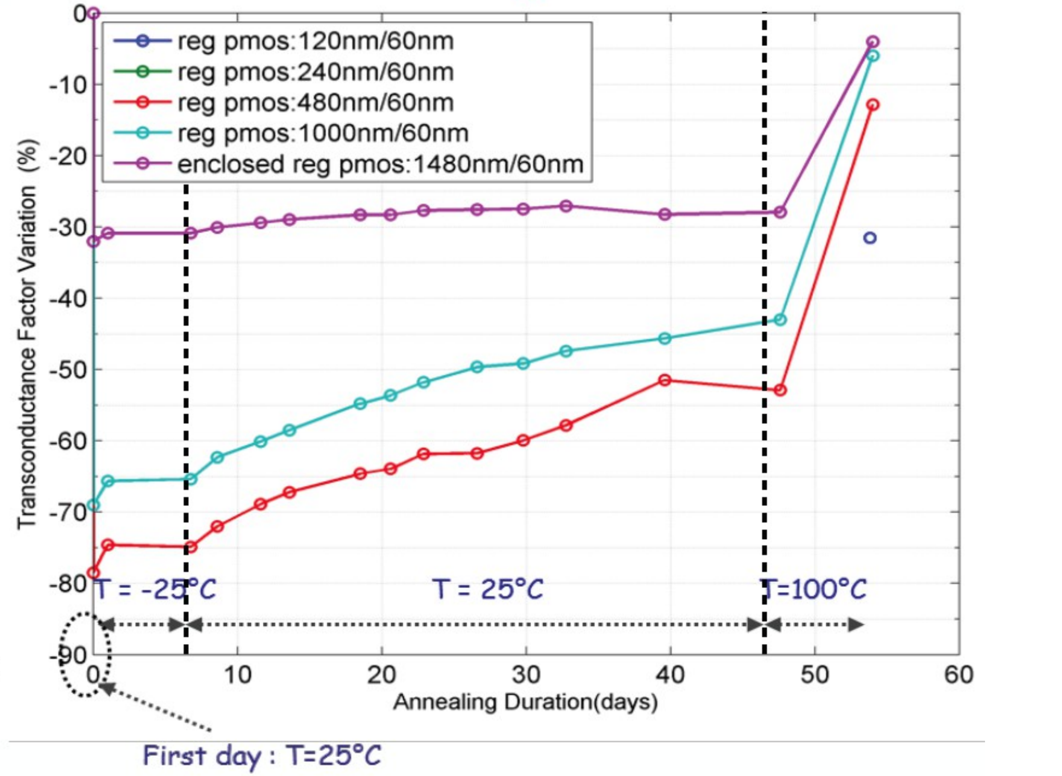
The chip should provide up to 8 data output e-links of 1.3 Gb/s

Radiation hardness of 65 nm CMOS technology

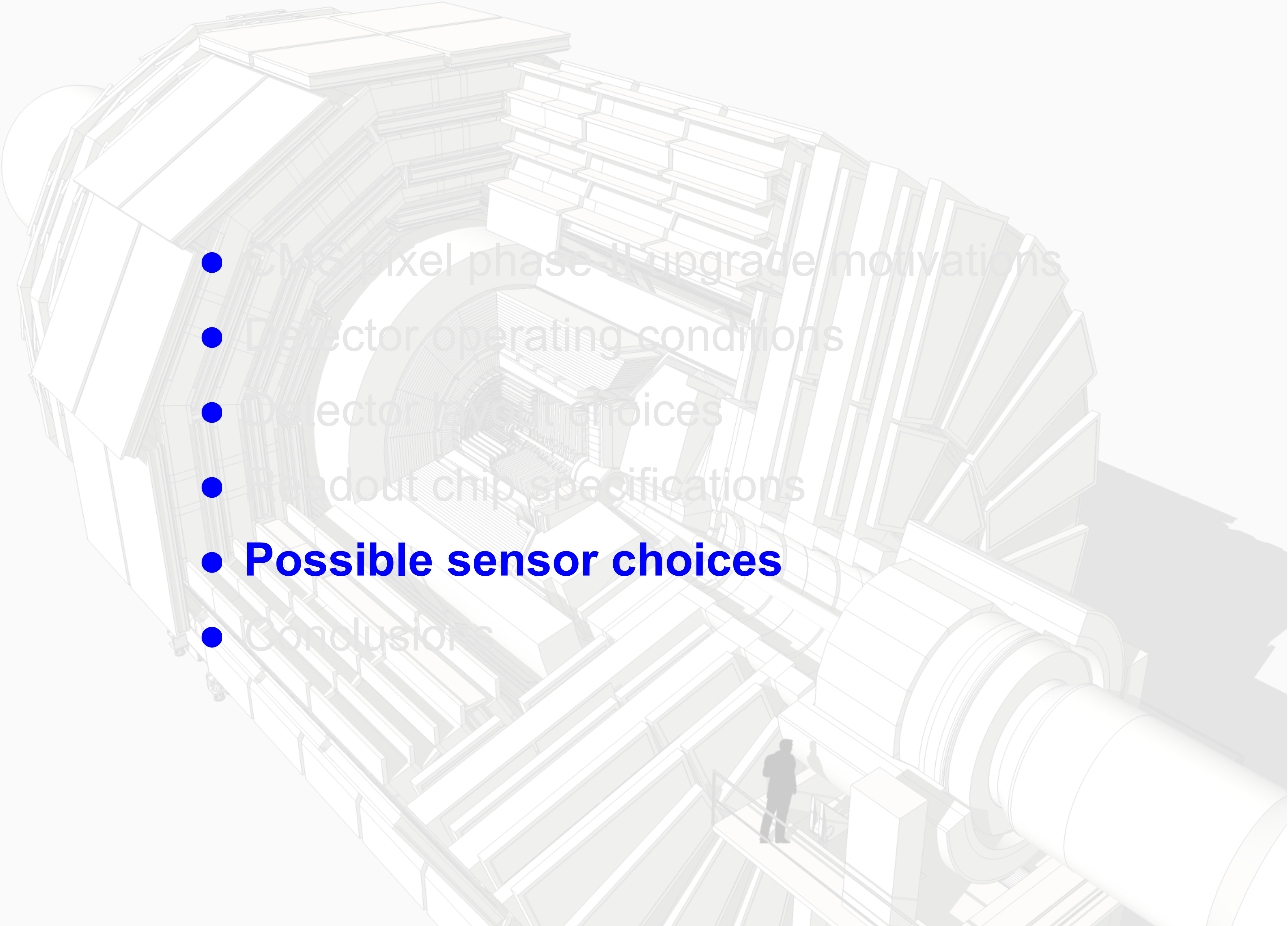
Transconductance factor variation vs dose



Transconductance factor var. vs annealing time



- Among other effects, PMOS-FETs (especially minimum size ones) show large transconductance degradation vs. dose (becomes very steep at dose > 100 Mrad)
- Damage mechanism have yet to be fully understood
- It appears that some of the radiation damage in the chip could be annealed with high temperatures → possibly define plausible annealing scenarios during detector maintenance to optimise longevity of sensors and electronics (detailed evaluation of annealing effects on sensor performance)



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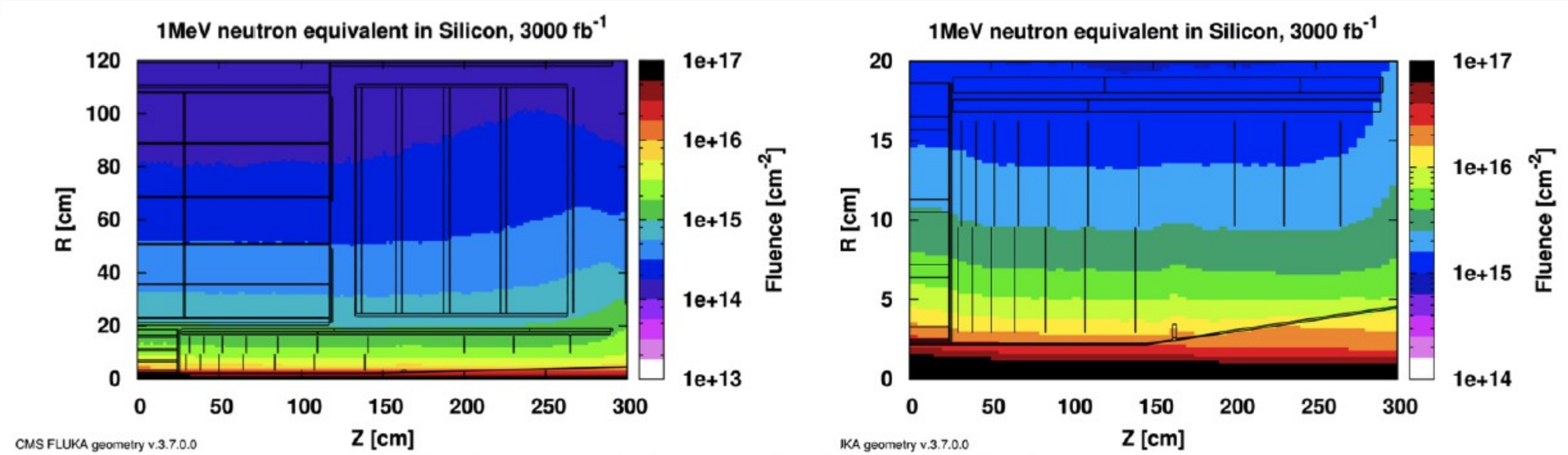
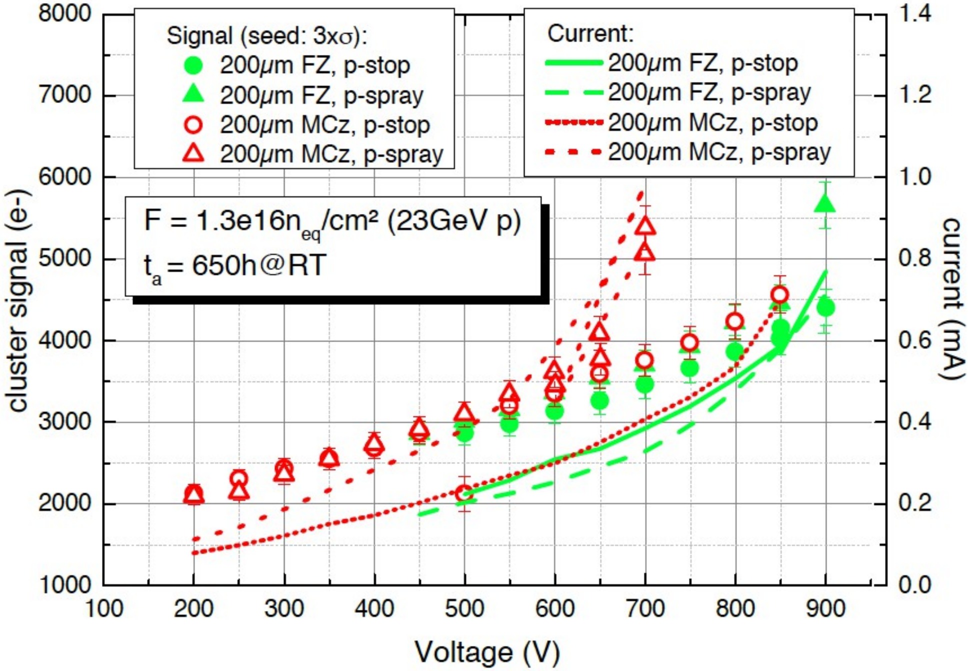
Possible sensor choices

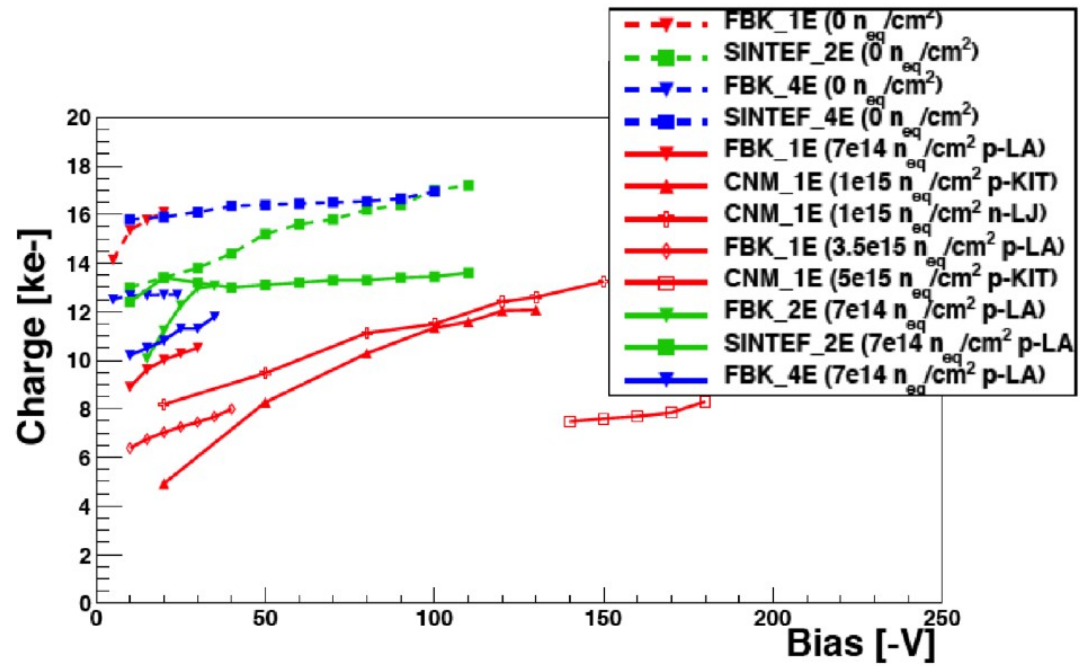


Radiation tolerance dominates technological choice for sensors. Possible sensors technologies:

- Favoured technology: planar Silicon
  - Define suitable *n-in-p* process and design (more cost effective than present *n-in-n*)
  - Thin thickness
  - Requires robust spark rejection material
- Alternative/complementary for innermost layer: 3D Silicon
  - Intrinsically higher radiation resistant (the shorter charge collection distance);
  - production process more expensive and not suitable for large volumes, use of 3D sensors could be limited to the small regions of highest particle fluence;
  - Define suitable sensor thickness and electrode geometry
  - Address production issues (e.g. yield and cost)

Possible sensor choices





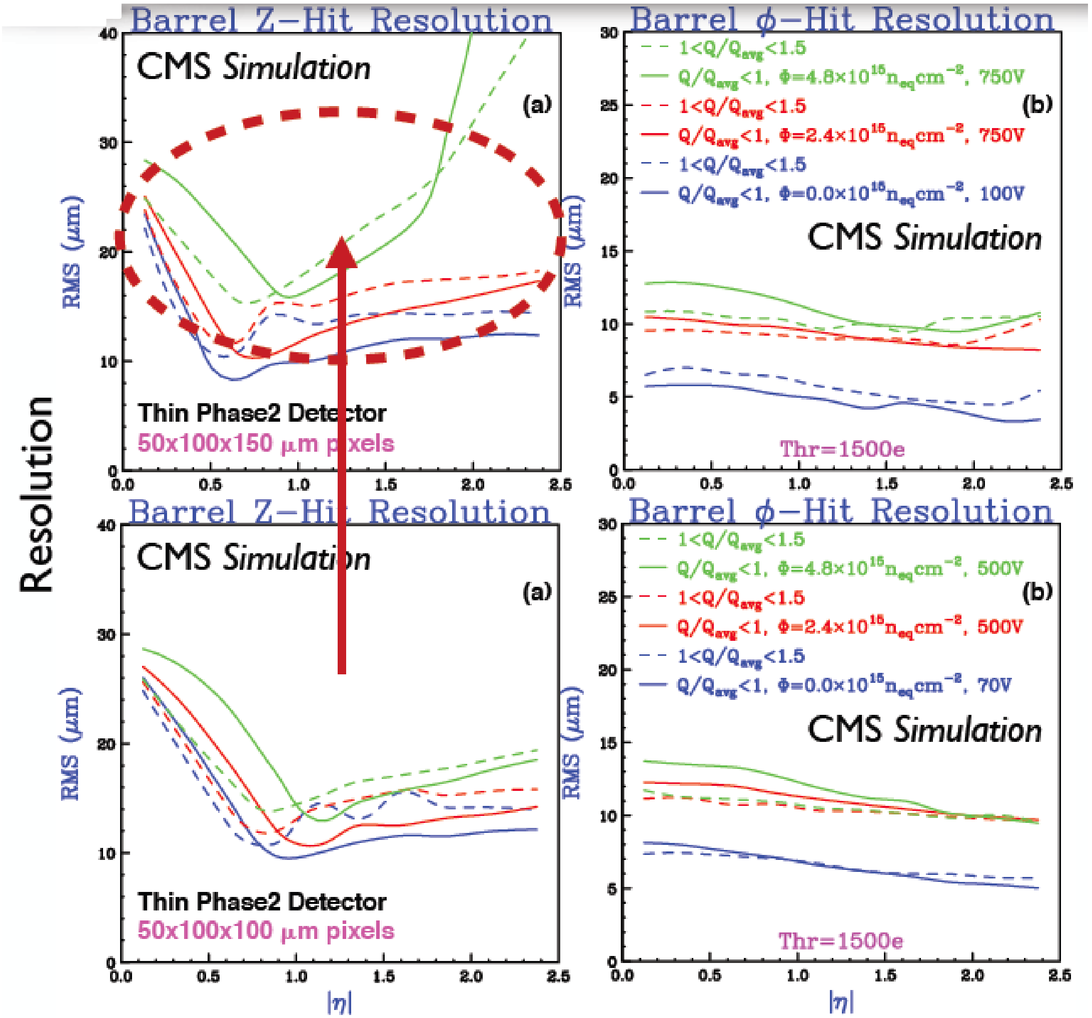
- Signal charge and leakage current in **planar n-in-p silicon pixel structures** in different processes and isolations (irradiation 1.3×10^{16} n_{eq} / cm^2)
- Signal charge in **3D n-in-p silicon pixel structures** from different vendors and with different column configurations (before and after irradiation up to $3.5\ 10^{15}$ n_{eq} / cm^2)

Need to define:
- Sensor thickness
- Sensor process (FZ, MCz, EPI)
- Spark rejection material
- Pixel isolation and bias scheme

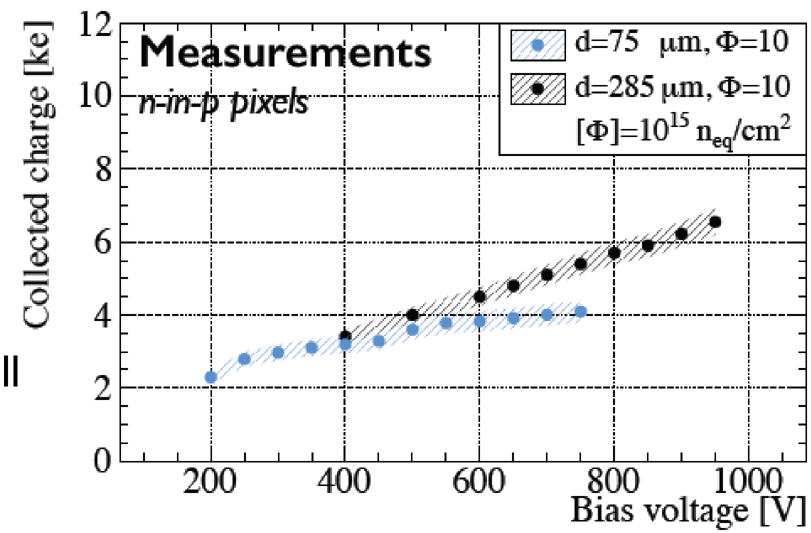
Need to define:
- Column electrodes positions and size
  → sensor thickness
- Production process: single/double sided

Thin planar Silicon sensors: thin thickness

Barrel resolutions



- Thin planar sensors advantages:
  - Higher fields with same bias → shorter drift time → less trapping → ultimately, better radiation hardness
  - Reduced full-depletion voltage
  - Smaller clusters → reduce merged cluster fraction in dense jets
- At very high fluences **thick** and **thin** planar sensors give similar charge



Assumptions:

- Noise 150 e^- and other readout and calibration effects are small
- Extrapolate irradiated Silicon model, tuned on data up to 1.2×10^{15} neq / cm^2, to larger fluence, 4.8×10^{15} n^{eq} / cm^2
- Average E-fields of 50 kV / cm can be achieved

Conclusions

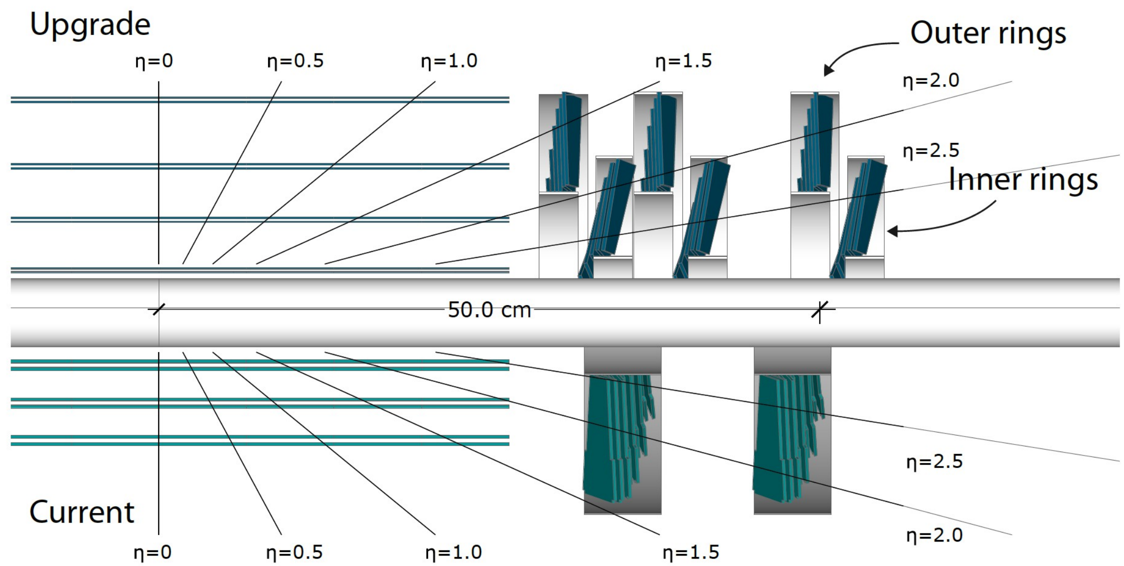
- Pixel detector operating conditions during Phase-II are extremely challenging
  - Pile-Up = 140
  - Radiation @ 30 mm from IP: 2×10^{16} n_{eq} cm^2
  - Dose @ 30 mm from IP: 10 MGy (1Grad)
  - Hit rate ~ 2 GHz/ cm^2
- Final detector layout and geometry is under definition
- Redout chip development (Atlas-CMS collaboration): 65 nm candidate technology → need to demonstrate radiation hardness up to foreseen 10 years operation at HL-LHC
- Sensor development: Silicon thin planar n-in-p (and/or Silicon 3D for innermost layer) candidate technology → need to define sensor process, bias isolation geometry, thickness, electrode geometry.

Still a lot of work ahead (hopefully) leading to future physics discoveries!

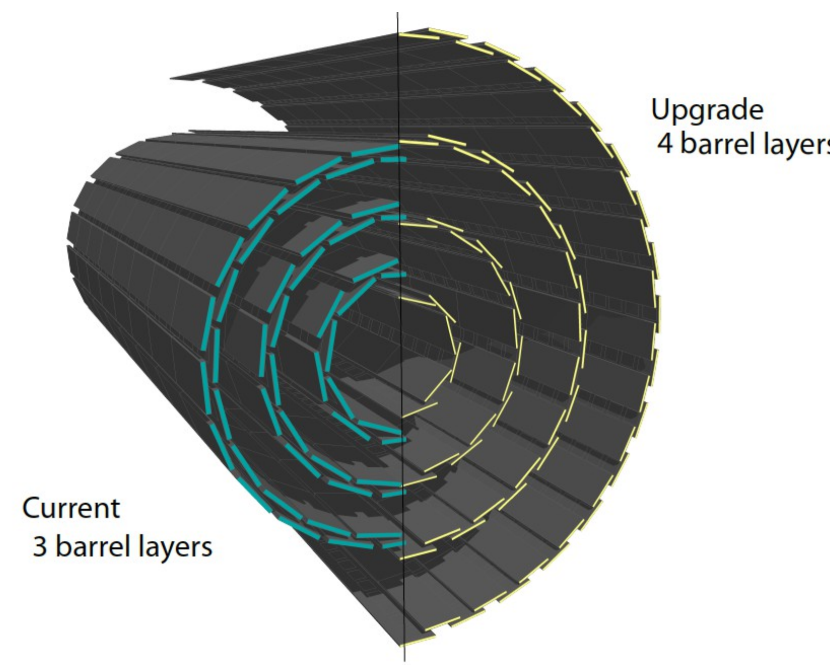
Backup

Phase I - post 2017 Pixel Detector

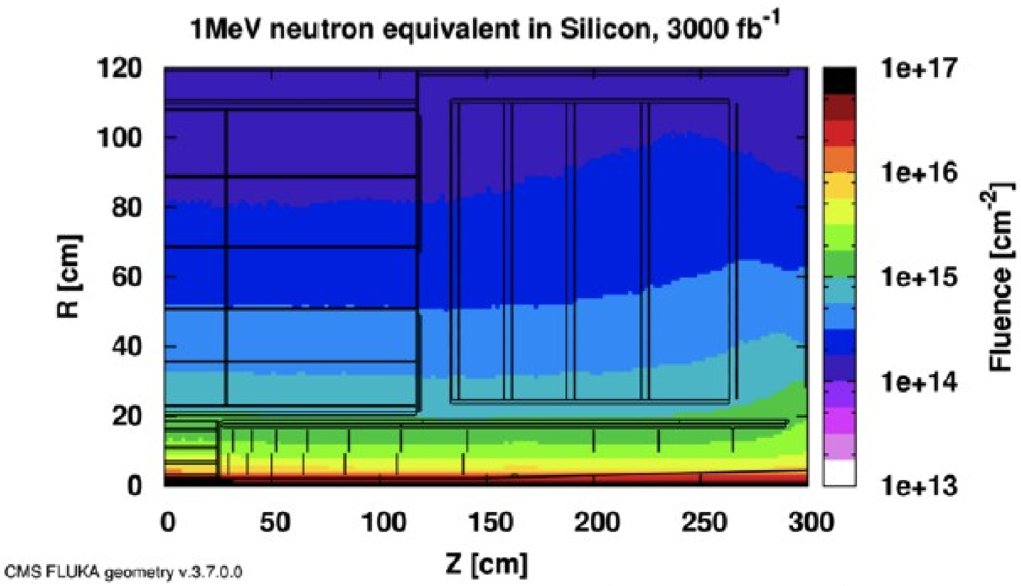
- The Phase1 pixel detector is an improved version of the current pixel detector.
- 4 layers / 3+3 disks (100x150 μm^2, n^+-in-n): improved track resolution and eff ciency
- New readout chip: reduced dynamic ineff ciency at high rate and PU

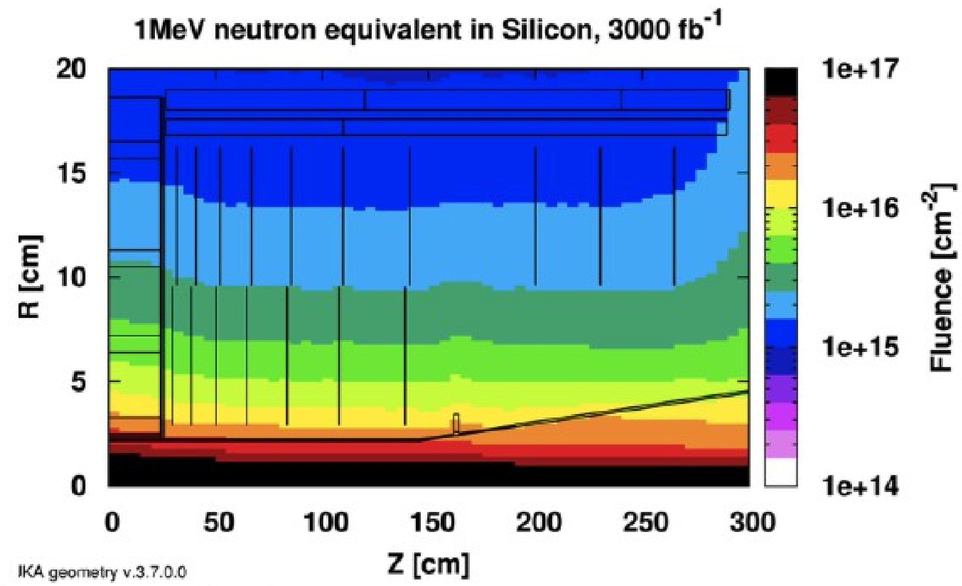


- Reduced material: CO_2 cooling, new cabling and DC-DC powering scheme
- Will be installed during the 2016 Technical Stop; a pilot disk 3 blade is being installed for 2015 for testing



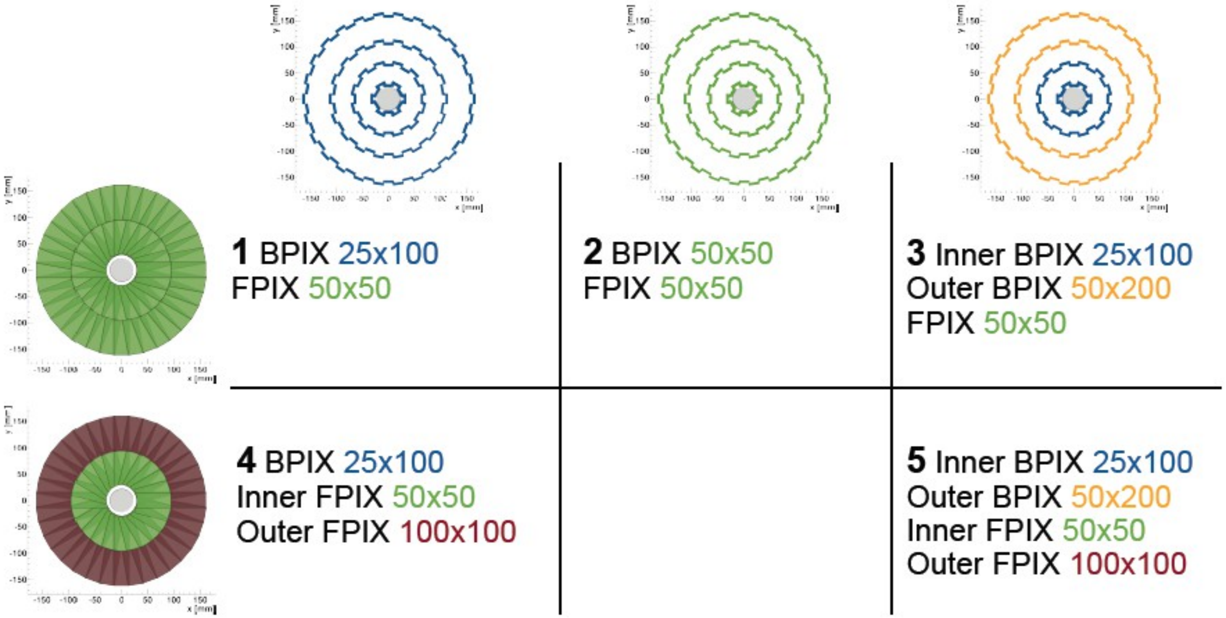
Fluences



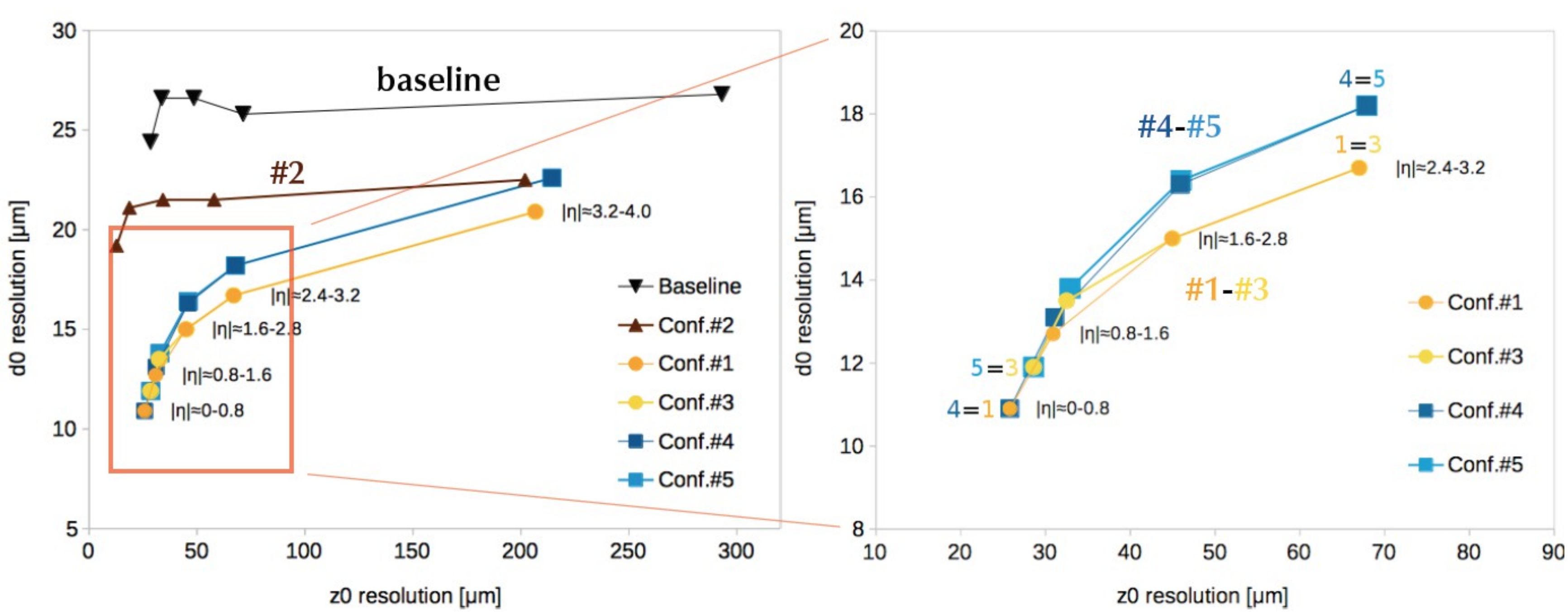


- Left: map of the expected particle fluence in the Tracker volume corresponding to an integrated luminosity of 3000 fb^{-1}, expressed in terms of 1 MeV neutron equivalent fluence.
- Right: detail of the fluence in the pixel volume. The expected fluence has a strong dependence on radius, while it is almost independent of the z coordinate.

Impact parameters resolutions d_0 vs z_0



- Petal configurations with mixed pixel sizes show better tracking performance than Petal #2 and baseline (Phase-I) geometries



Phase-I Tracking Performance