The Belle II Pixel Detector for SuperKEKB

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on behalf of the
DEPFET Collaboration

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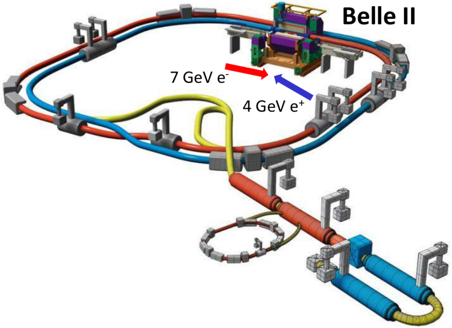
Content

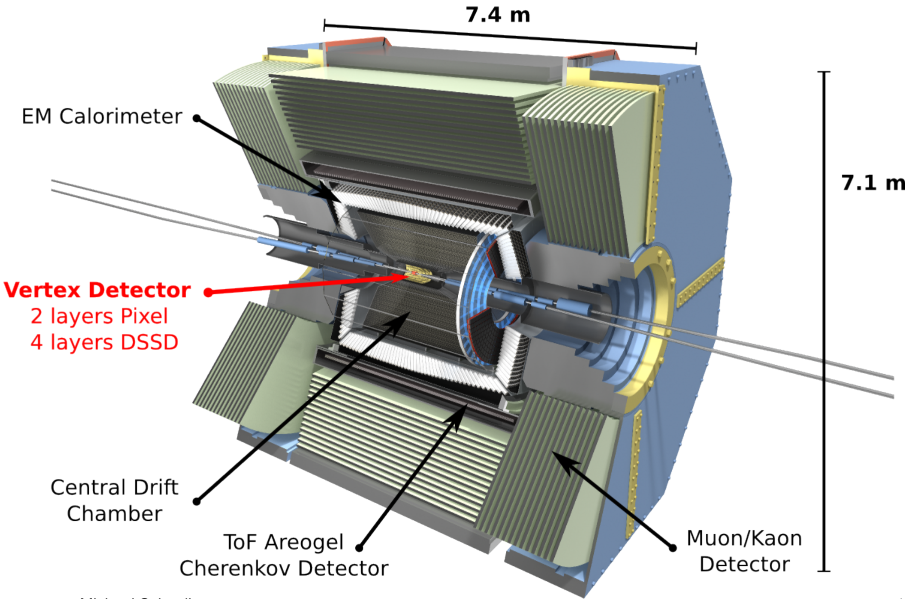
Overview of SuperKEKB

- Upgrade of KEKB using the same tunnel
- Asymmetric e^+e^- energy collider utilizing the nanobeam scheme (10 μm x 60 nm) for a significant higher luminosity of $8 \cdot 10^{35}\ cm^{-2}s^{-1}$ (50x KEKB)
- B-factory with center of mass energy at the Y(4S) resonance

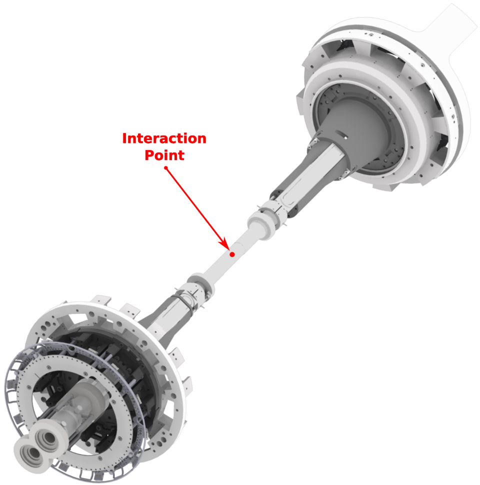


- Precise measurements of the CKM triangle, search for new physics in rare B-, D-meson and τ-decays
- Expect 40 times more data and an similar increase in background $\rightarrow$ New detector required

Belle II Detector



Belle II Vertex Detector



- Beryllium beam pipe radius: 10 *mm*
- 2 layers DEPFET Pixel Detector (PXD) with 8 million pixels at 1.4 and 2.2 cm
- 4 layers of Silicon strip Vertex Detector (SVD) using DSSDs with slanted parts at 3.8, 8.0, 11.5 and 14 cm (see next talk)

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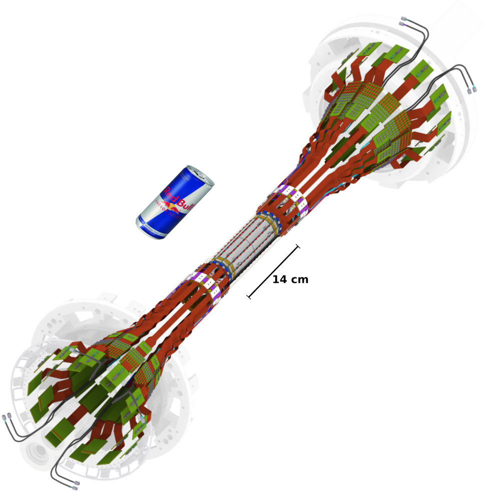

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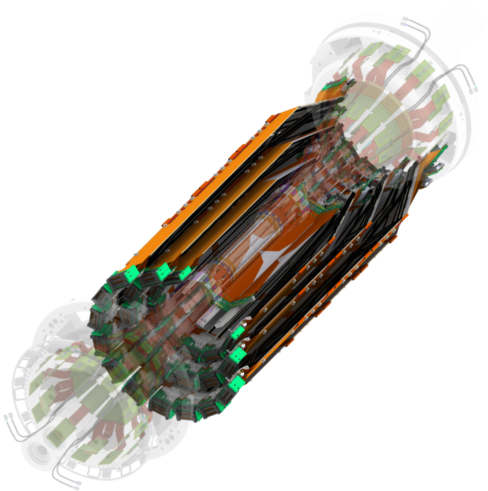

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Belle II Vertex Detector

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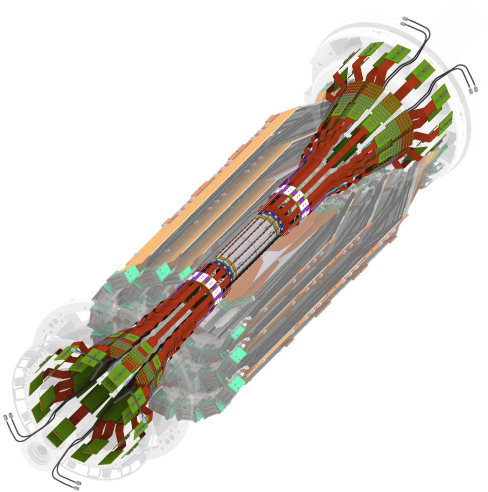

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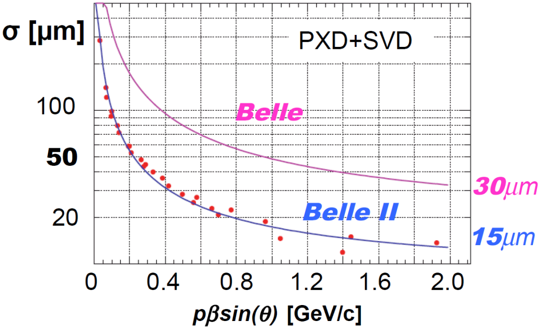
Requirements for the Pixel Detector

- Thin (low material budget) self sustaining modules to avoid MS (0.2 % X_0/layer)
- Radiation hard: 1.8 Mrad/Year
- Occupancy: < 3 %
- Acceptance Angle: 17 - 155°



- Higher vertex resolution required than in Belle because of decreased boost $\beta\gamma$ = 0.28 vs 0.42 (KEKB)
- To keep occupancy a continuous 20 μs readout mode is required

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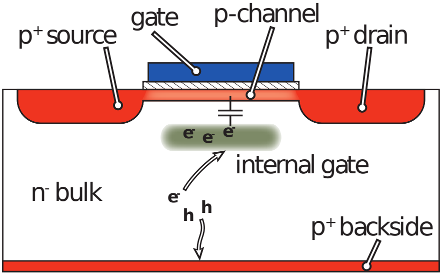
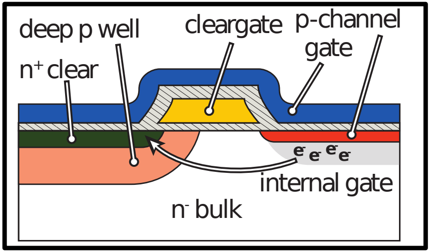
DEpleted P-channel Field Effect Transistor

- FET transistor on a fully depleted silicon bulk
- Additional n-implant causing a potential minimum below the transistor channel (internal gate)
- Electrons are stored in the internal gate modulating the p-channel current (internal amplification $g_q =\sim 500\ pA/e^-$)
- Clear process required to remove the stored charges



Clear process



DEPFET Matrix Readout

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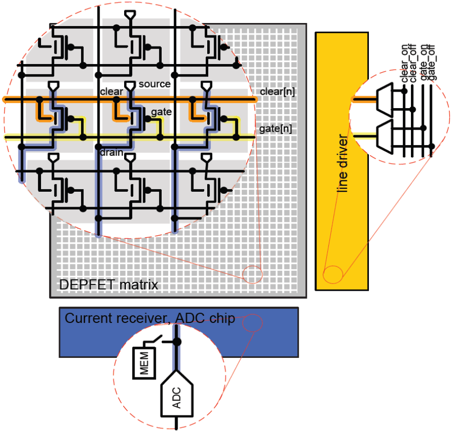
- DEPFET pixels arranged in a matrix
- Constant "rolling shutter" readout (four rows each time)
- Long drain and gate/clear lines to place chips on the balcony out of the active area
- Only active rows consume power, the others are still sensitive to charge
- Several ASICs required (Switcher, Current Digitizer...)

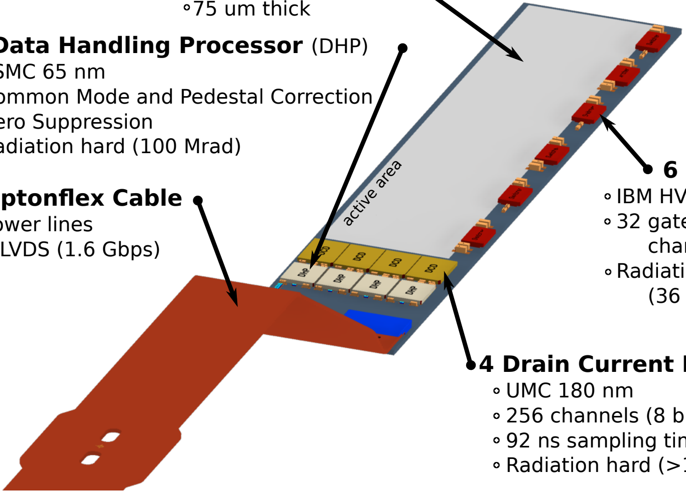


A DEPFET Half Module

DEPFET Matrix
- 250 x 768 px
- 75 um thick

4 Data Handling Processor (DHP)
- TSMC 65 nm
- Common Mode and Pedestal Correction
- Zero Suppression
- Radiation hard (100 Mrad)

Kaptonflex Cable
- Power lines
- 4 LVDS (1.6 Gbps)

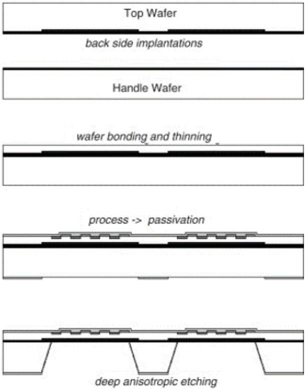


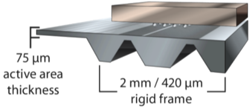
6 Switchers
- IBM HVCMOS 180 nm
- 32 gate and clear channels
- Radiation hard proved (36 Mrad)

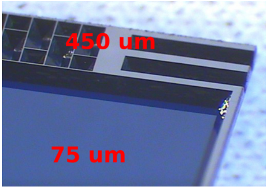
4 Drain Current Digitizer (DCD)
- UMC 180 nm
- 256 channels (8 bit ADC)
- 92 ns sampling time
- Radiation hard (>10 Mrad)

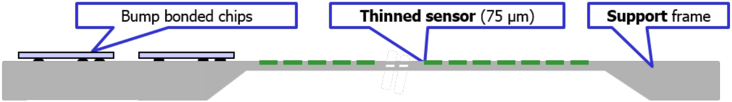
Thinning Technology

- Use anisotropic etching down to 75 μm on active area
- Balcony for steering ASICs and support frame
- 90 steps involved in Wafer processing

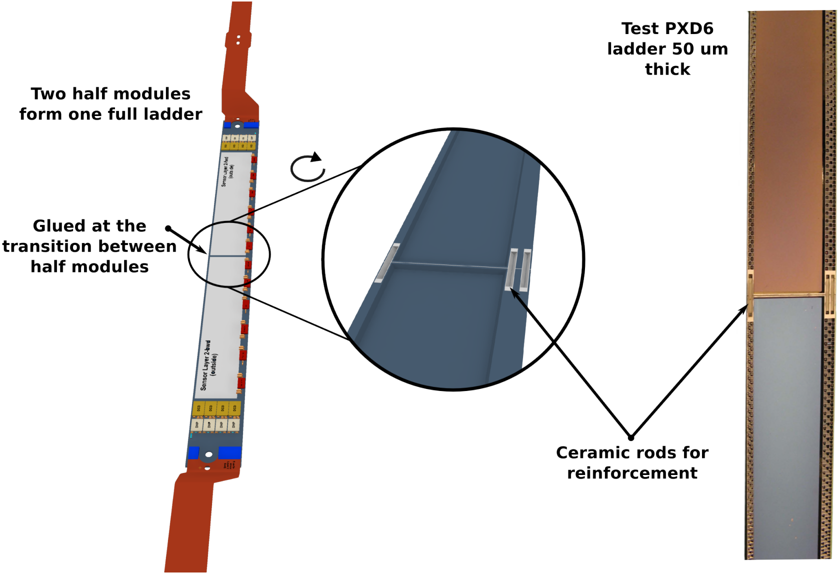








Building a DEPFET Ladder



Complete Pixel Detector

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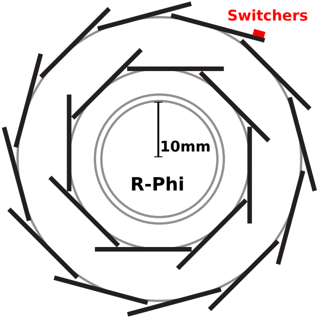
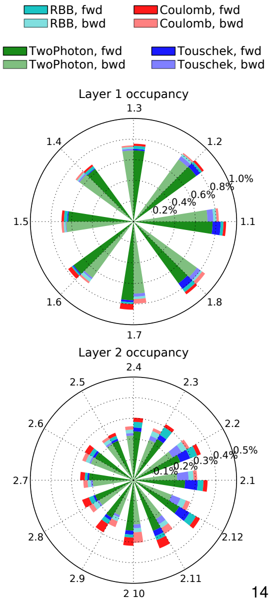
Info	Layer 1	Layer 2
Modules	8	12
Radius	14 *mm*	22 *mm*
Size	15x136 *mm*	15x170 *mm*
Pixel size	50x55 μm 50x60 μm	50x70 μm 50x85 μm
# Pixels	250x1536	250x1536
Thickness	75 μm	75 μm



- Windmill structure to keep Switchers from sensitive area
- Challenging task: 40 sensors and 560 ASICs on $4.5 \cdot 10^{-5}\ m^3$
- 40 half modules each $4 \cdot 1.6\ Gbps = 256\ Gbps$
  $\rightarrow$ Needs data reduction

Expected Background

Background	Layer 1	Layer 2
QED	0.8 %	0.3 %
Touschek	< 0.03 %	< 0.03 %
Radiative Bhabha	< 0.13 %	< 0.13 %
Beam-Gas	< 0.01 %	< 0.01 %
Total	< 1.0 %	< 0.5 %



- Synchroton radiation studies ongoing
- An average $B\bar{B}$ event creates 10 tracks
- PXD is dominated by background hits!

DAQ System

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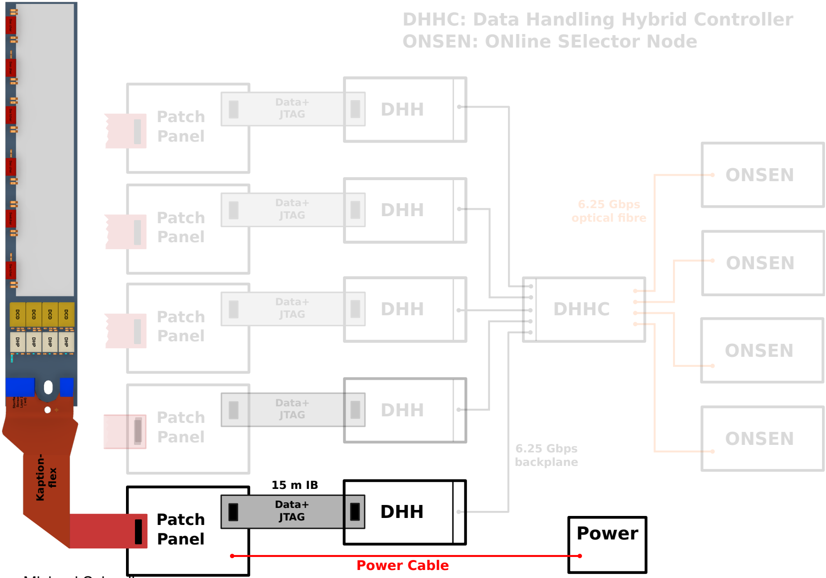
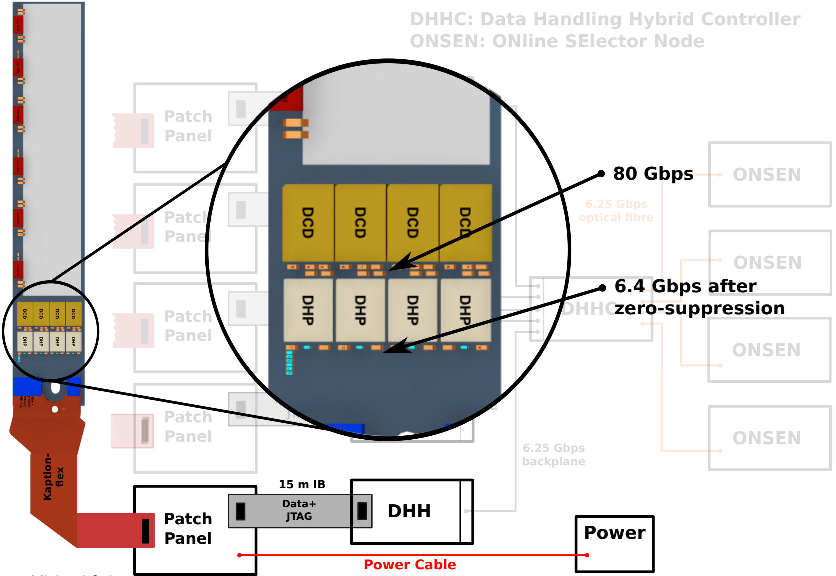
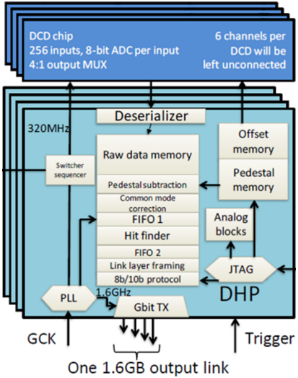


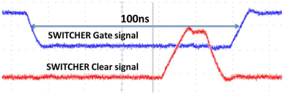
DAQ System: Zero Suppression

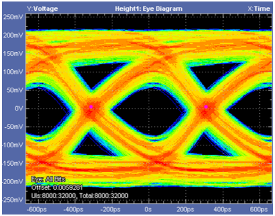


Data Handling Processor

- Common mode and pedestal correction
- First step of data reduction (zero suppression)
- Data handling up to 2.6 % occupancy without loss
- Controls Switchers and DCD
- High speed data transfer with pre-emphasis link driver (50 cm Kaptonflex + 15 m Infiniband cable)







DAQ System: Data Handling Hybrid (DHH)

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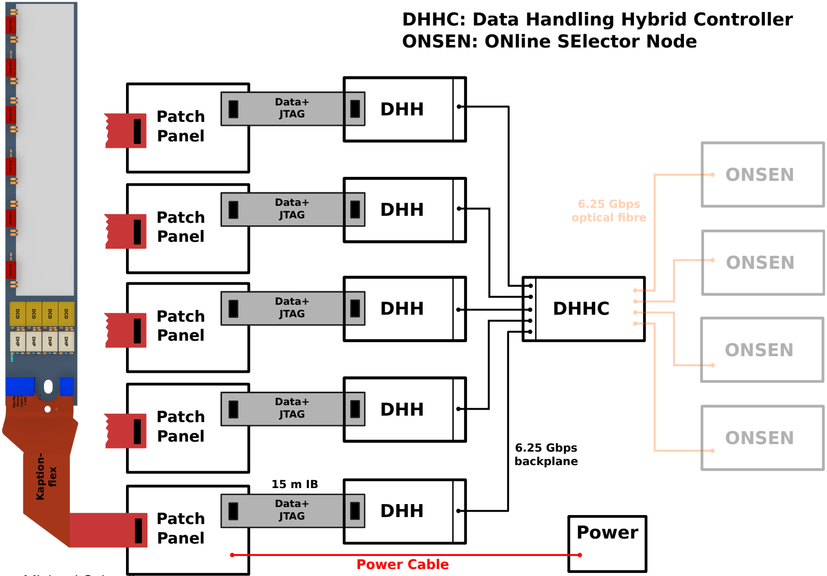
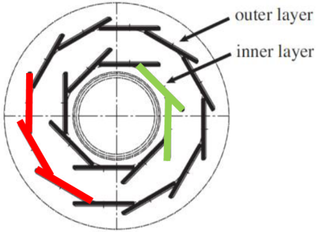


DHH System

- 5 DHHs connected to one DHH Controller (DHHC)
- Load balancing: 3 layer 2 and 2 layer 1 per DHHC
- Built-on Virtex 6 FPGAs in ATCA standard
- Tasks of the DHH system:
  - Distribute timing and slow control signals to PXD FEE
  - Clustering of pixel data
  - Converting of LVDS high speed to optical signal (connected to ONSEN)



DAQ System: ONline SElector Node

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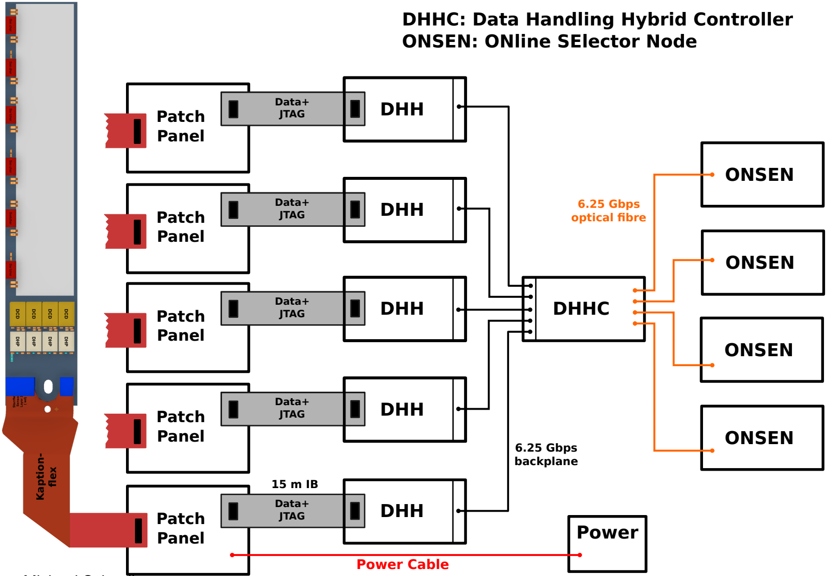

ONline SElector Node (ONSEN)

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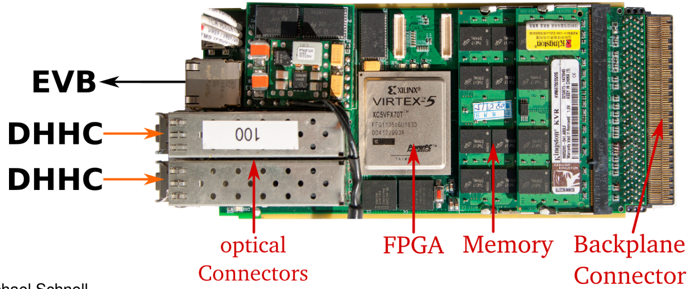
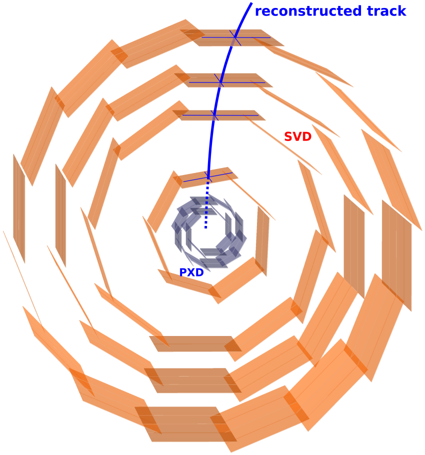
- Build on the xTCA standard
- Using Advanced Mezzanine Cards (AMC) with Virtex 5 FPGA
- Receives data from DHHC over 6.25 Gbps optical links
- Performance data reduction over pixel selection with Region Of Interests (ROI)
- Sends data to EVent Builder (EVB) over Gbit Ethernet.



Data Reduction Idea with SVD Tracking

- Idea: Use hits of the surrounding strip detector, find and fit tracks, back extrapolate on the PXD and create Region of Interest (ROI)
- Complementary approach with two systems to save as much physics data as possible
- HLT: Track reconstruction based on sector-neighbour finding and neural network
- DATCON: Fast FPGA-based track reconstruction system using the Fast Hough Transformation



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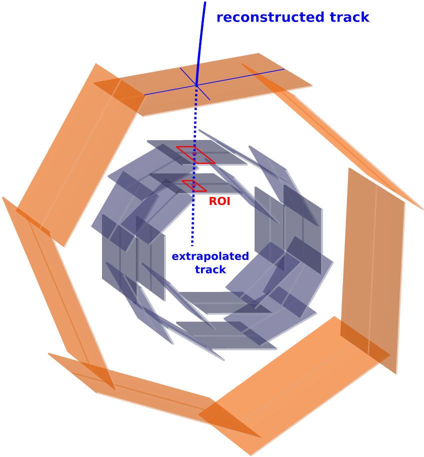
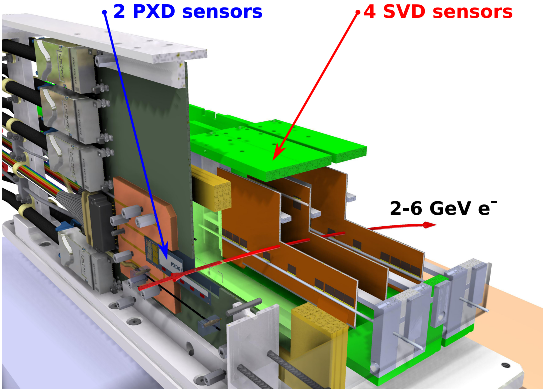


Content

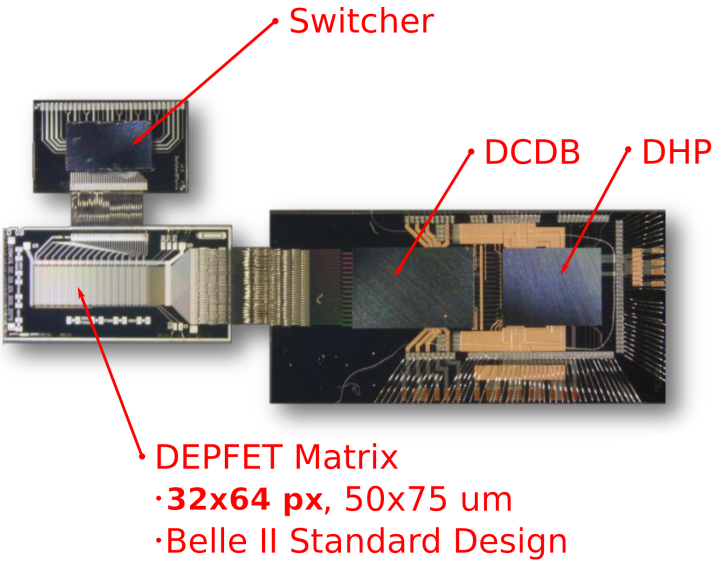
DESY Testbeam Setup (Jan. 2014)

- Common PXD and SVD beam test in January 2014 at DESY with an up to 1 T magnet field
- One sensor representing one layer
- Prototype of every DAQ components involved in the later data chain



- CO_2 cooling, slow control and environmental sensors
- Goal: Overall concept operation

Former Testbeam Setup: From This...



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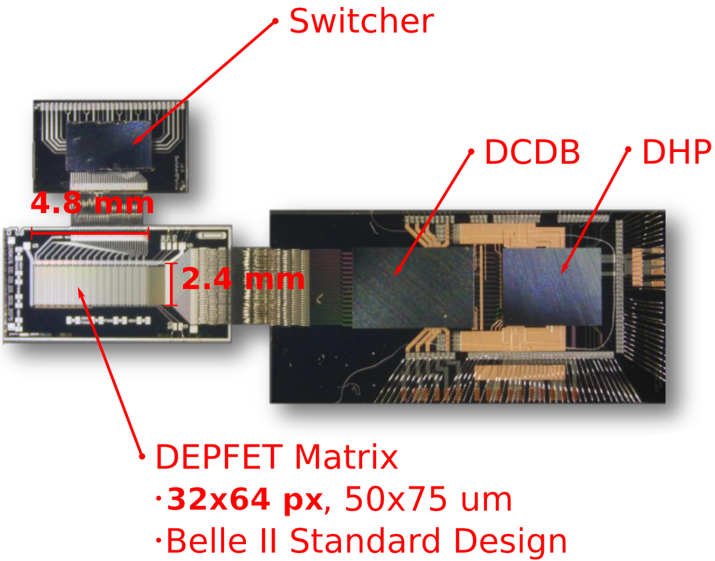

New Testbeam Setup: To This!

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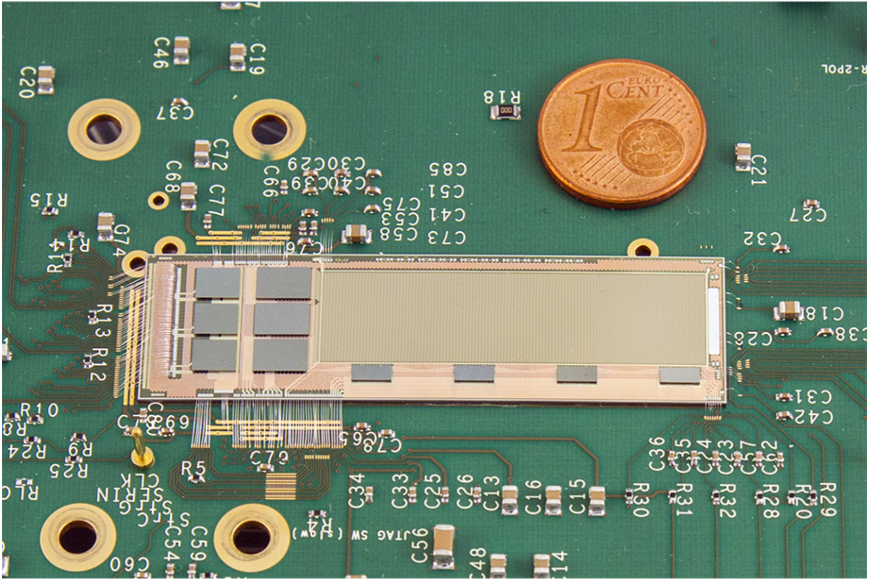

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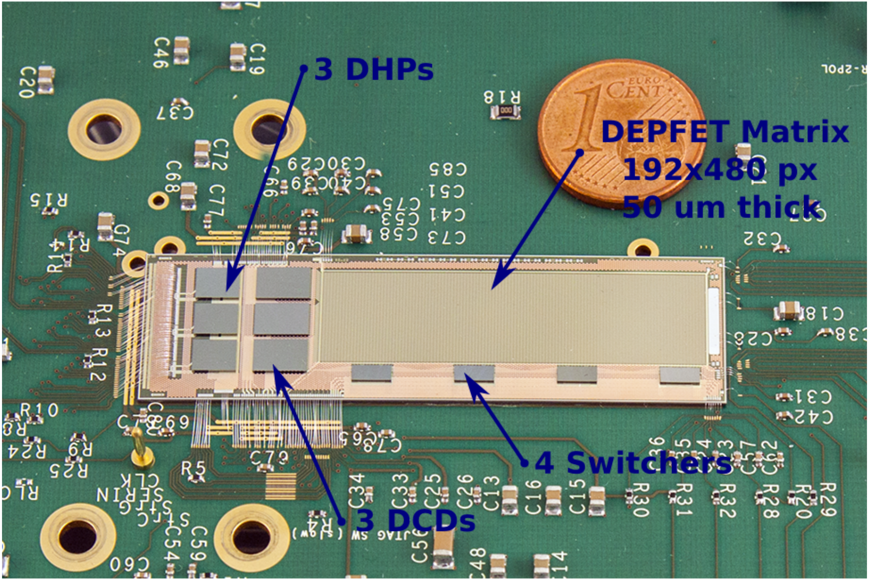
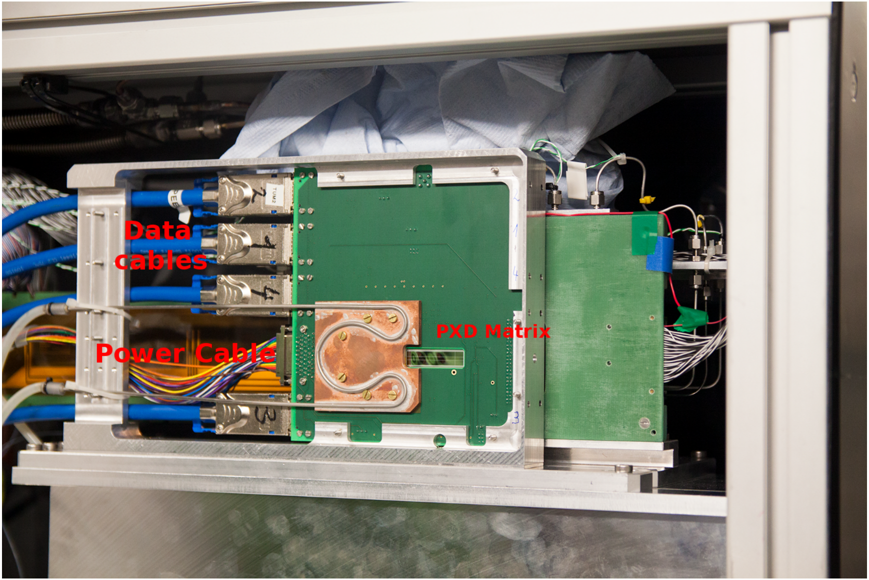
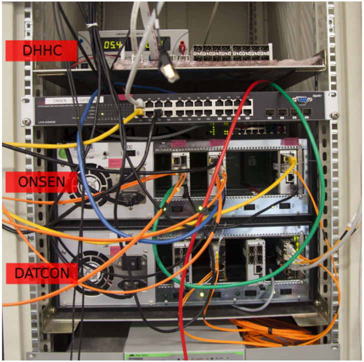


Installed PXD

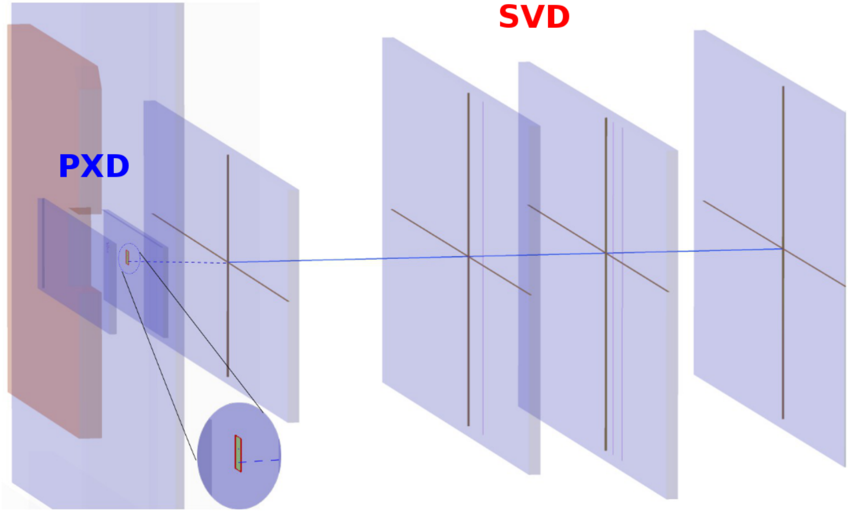


DAQ System

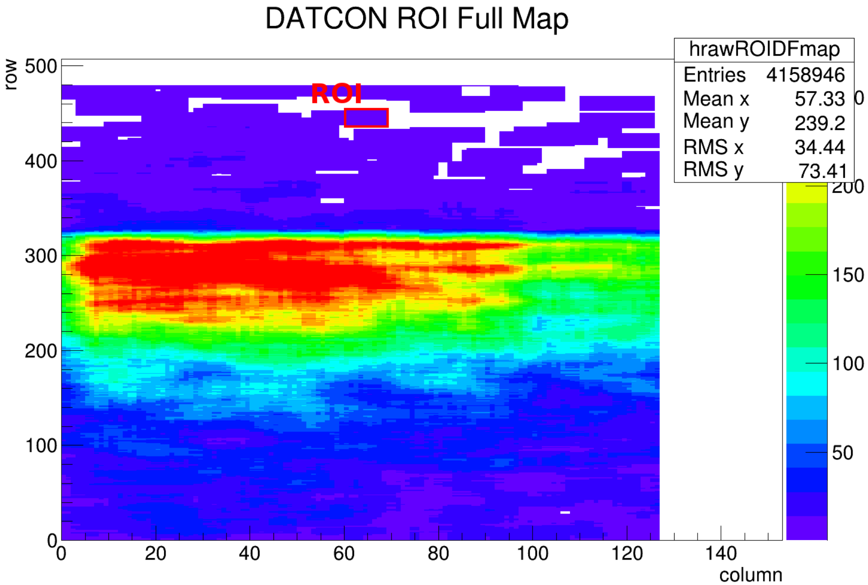
- Prototype of every DAQ components involved in the later data chain: DHH, DHHC, ONSEN, HLT, DATCON
- Testing of clustering and Region of Interests scheme
- Trigger distribution (over TLU) successfully tested
- Tested up to (random) trigger rates of 1.5 kHz



Example Event from Testbeam



Accumulated Region of Interests Map



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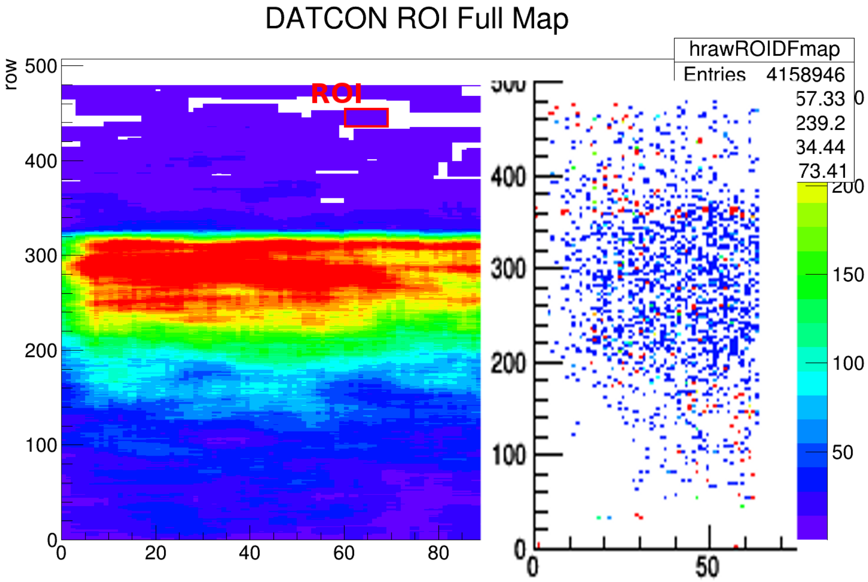
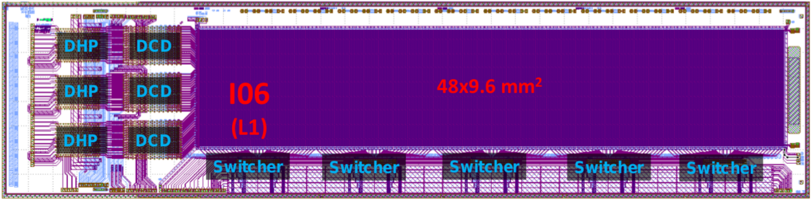


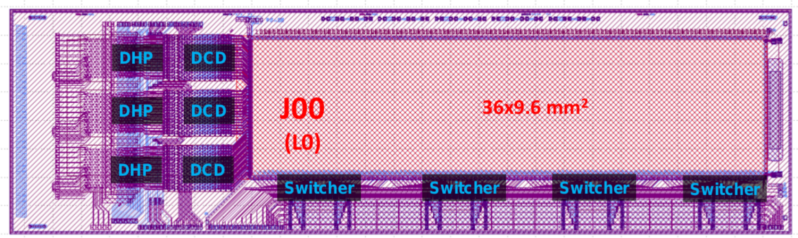
Conclusion

- Belle II requires a new inner Vertex detector to cope with increased luminosity and higher vertex reconstruction demands
- The DEPFET technology comply with all these demands
- DESY testbeam proved the principle working conditions of all involved parts: sensors, DAQ system and software/algorithms
- Lessons learned from "real" long-term operation at DESY for the final detector
- Final sensor production started

Thank you for your attention!

Two Devices Under Test





Sensor Description

- IO6
  - Represents layer 2
  - 50x75 μm
  - 640 drain lines (3 DCDs, DHPs)
  - 160 gate/clear lines (5 Switchers)
- J00
  - Represents layer 1
  - 50x75 μm
  - 480 drain lines (3 DCDs, DHPs)
  - 120 gate/clear lines (4 Switchers)