Overview of HV-CMOS devices

Daniel Muenstermann

with material from the ATLAS HV/HR-CMOS and RD50 collaborations

“Original” ATLAS HV/HR-CMOS collaboration

- University of Bonn
  - L. Gonella, T. Hemperek, F. Hügging, H. Krüger, T. Obermann, N. Wermes
- LBNL
  - M. Garcia-Sciveres
- CERN
  - M. Backhaus, M. Capeans, S. Feigl, S. Fernandez Perez, M. Nessi, H. Pernegger, B. Ristic
- University of Geneva
  - S. Gonzalez-Sevilla, D. Ferrere, G. Iacobucci, A. Miucci, D. Muenstermann, A. La Rosa
- University of Goettingen
  - M. George, J. Große-Knetter, A. Quadt, J. Rieger, J. Weingarten
- University of Glasgow
  - R. Bates, A. Blue, C. Buttar, D. Hynds
- University of Heidelberg
  - C. Kreidl, I. Peric
- CPPM
  - P. Breugnon, P. Pangaud, D. Fougeron, F. Bompard, J.C. Clemens, J. Liu, M. Barbero, A.Rozanov

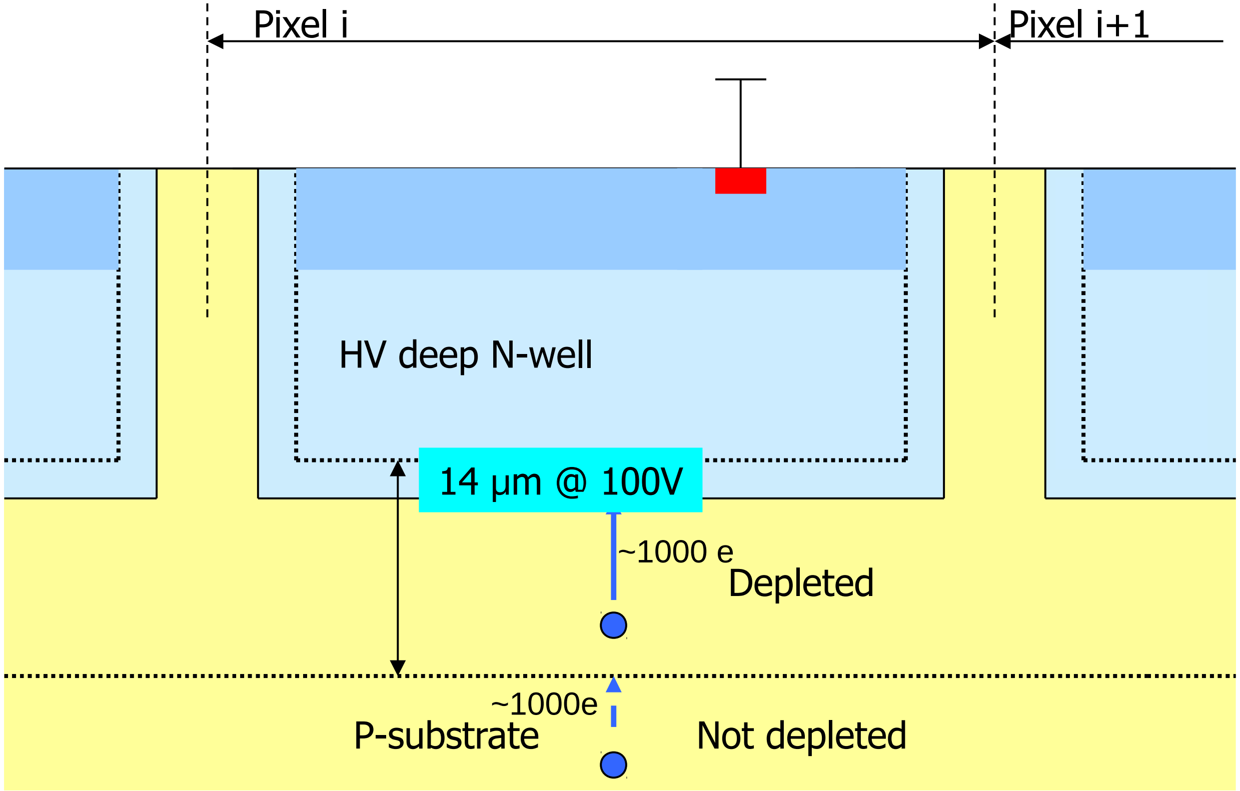
“Original” collaboration largely based on institutes with expertise in pixel readout chips, recently also much interest from strip upgrade community...

Overview of HV-CMOS devices

What is HV-CMOS? An HV-CMOS sensor...

... is essentially a standard n-in-p sensor fabricated by a CMOS foundry

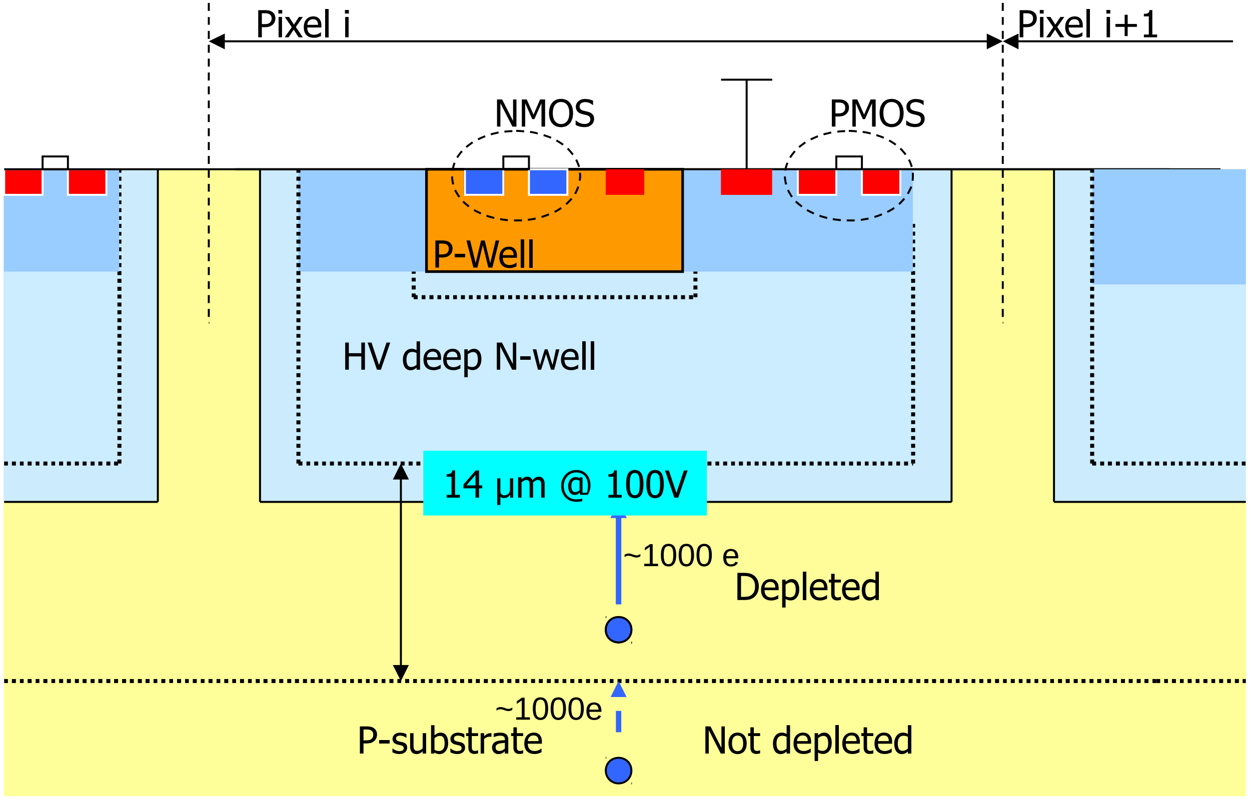
- usually rather low-resistive substrates: 10-20 Ohm*cm, rarely more
- CMOS process allows for “HV”, hence breakdown voltage ~30-120V
  - → depletion zone ~10 µm: signal in the order of 1-2ke$^-$
    - challenging for hybrid pixel readout electronics
  - disclaimer: “HV-CMOS” allows to switch “high” voltages, we don't even use this
- But it's a CMOS process, therefore we can...



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

...include active circuits: *smart diode array (SDA)*

- implementation of
  - first amplifier stages
  - additional cuircuits: discriminators, impedance converters, logic, …
    - careful: In its original form, no triple wells are used → PMOS only partially usable to avoid crosstalk
- deep sub-micron technology intrinsically rad-hard, but design needs to be specific, too



CMOS electronics placed inside the diode (inside the n-well)

Why HV-CMOS? Rad-hard **and** cheap sensors

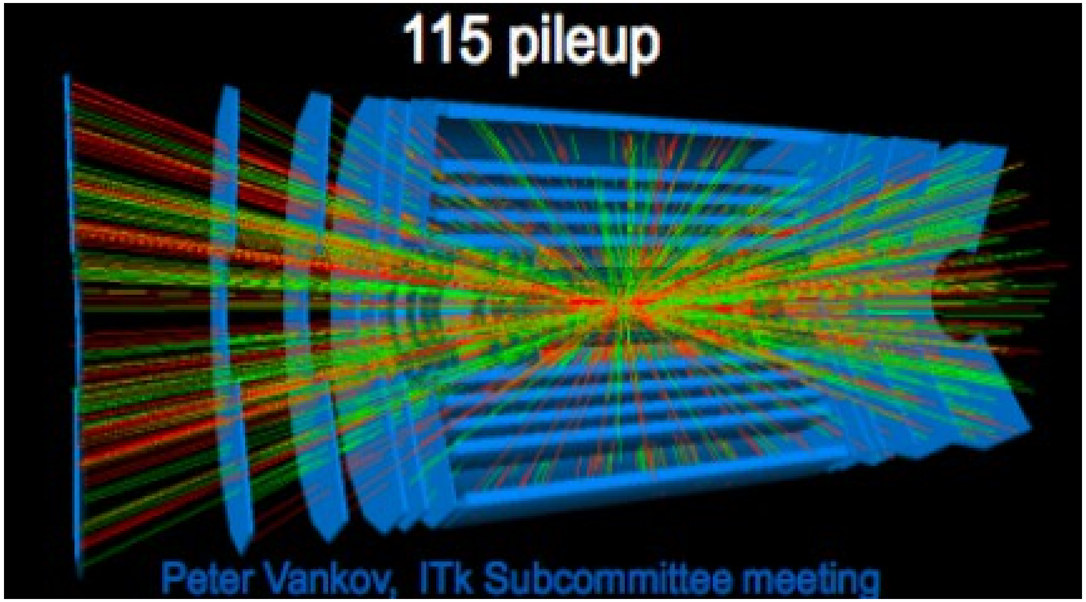
- Large efforts to assess and demonstrate superior rad-hardness using refined hybrid detectors
  - go to electron collection (n-in-n or n-in-p)
  - reduce drift distance (3D, thin silicon)
  - reduce/eliminate leakage current (CO2 cooling, diamond)
  - use deep-submicron rad-hard readout chips (130nm, 65nm)

→ in short: Hybrid detectors are rad-hard enough. Lots of experience with them. Could be used. The end?

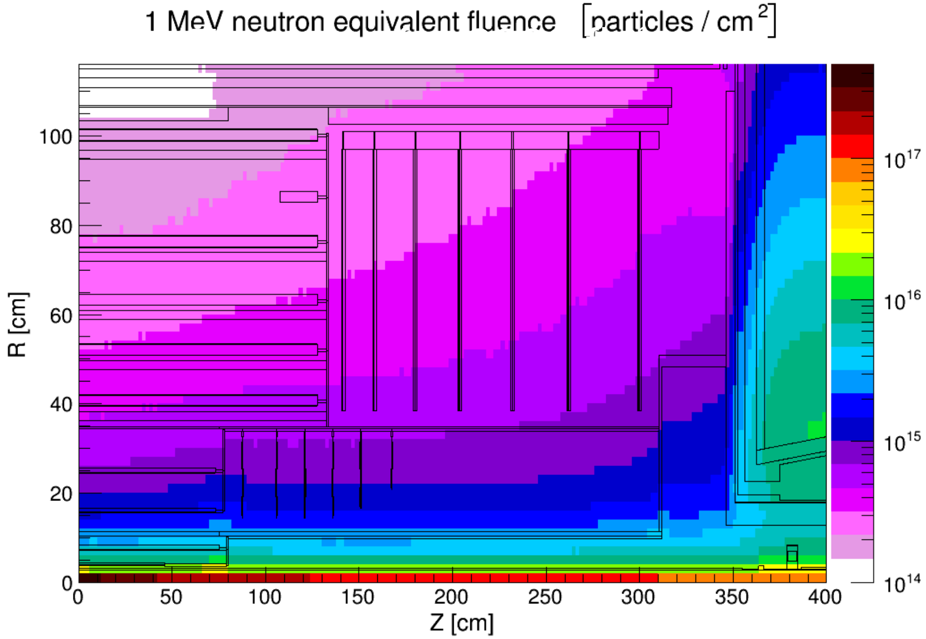
- Main drawback: Price
  - hybridisation expensive, small pitches require special processes
  - sensor processes non-standard and on small wafers, hence more costly
  - new trackers require ~200m^2 of silicon, price is important for the financial feasibility of the upgrade

Why new sensors anyway? HL-LHC and ATLAS

- At LHC, the Higgs was found, but many processes require huge amount of integrated luminosity → High-Luminosity LHC (HL-LHC)
    - integrated luminosity: 300 fb^{-1} → 3000 fb^{-1}
- What does this mean for the experiments?
    - higher occupancy: ~25 events/BC → 140-200 events/BC
    - more data rate → new readout electronics, rad-hard high-speed links
    - more radiation damage:
        - at 5 cm radius: ~$2 \cdot 10^{16}$ n_{eq} cm^{-2}, ~1500 MRad
        - at 25 cm radius: up to 10^{15} n_{eq} cm^{-2}, ~100 MRad, several m^2 of silicon
        - strip region: many 10^{14} n_{eq} cm^{-2}, up to 60 MRad, up to ~200 m^2 of silicon



Peter Vankov, ITk Subcommittee meeting

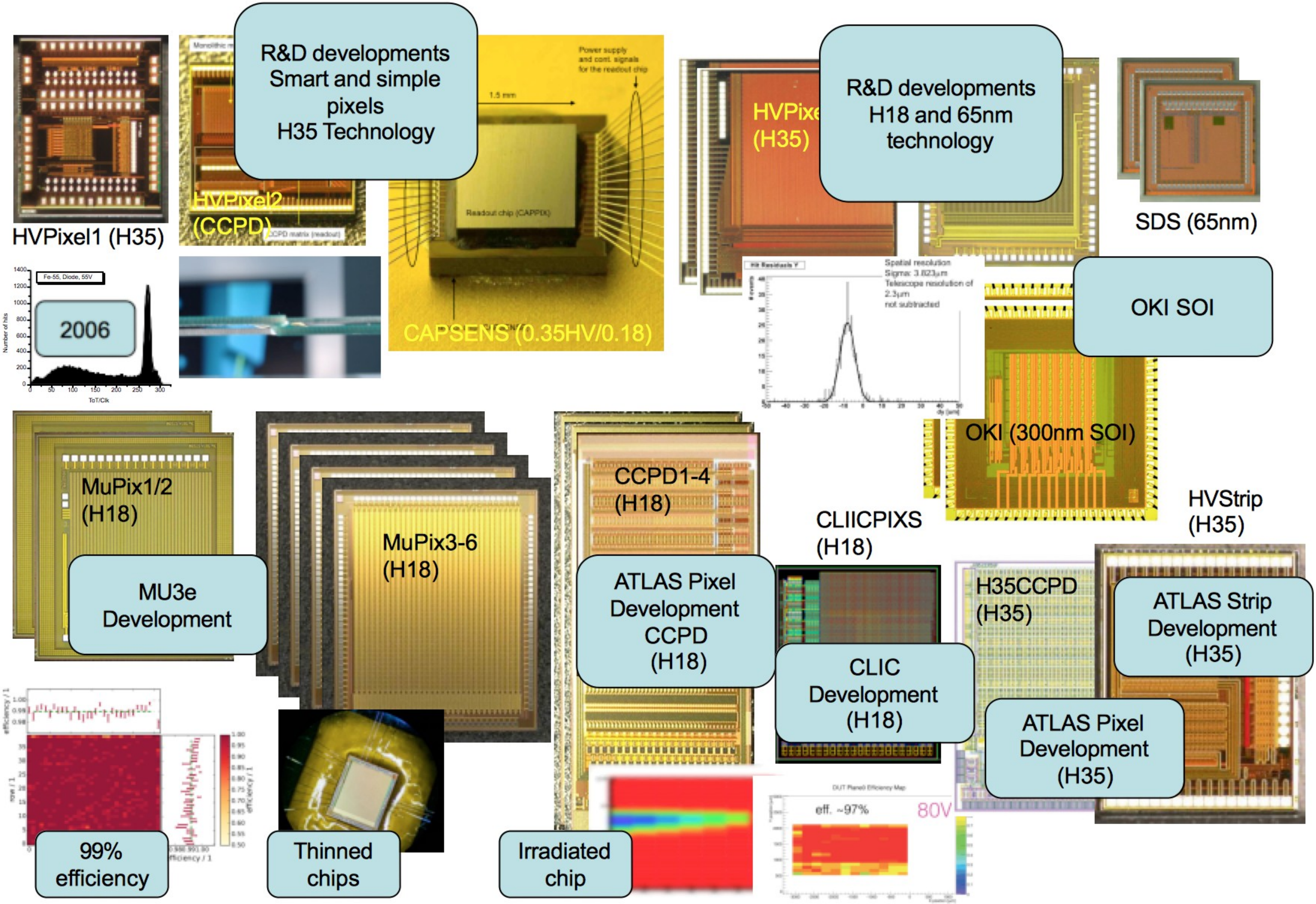


How to stay rad-hard, but get cheaper?

- Ways to reduce cost: use
  - industrialised processes
  - large wafer sizes
  - cheap interconnection technologies
- **Idea: explore industry standard CMOS processes as sensors**
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
    - but: application of **drift field** required for sufficient rad-hardness
      ➔ requires careful choice of process and design
  - 8” to 12” wafers
    - low cost per area: “as cheap as chips” for large volumes
    - wafer thinning quite standard
  - usually p-type Cz silicon
    - thin active layer, helpful to disentangle tracks in boosted jets and at high eta
      - requires low capacitance → small pixel
- Basic requirement: Deep n-well (→ allows high(er) substrate bias)
  - existing in many processes, e.g. even 65nm (!)
  - usually deepest in HV-CMOS → highest possible bias
  - also existing in specialised imaging processes → HR-CMOS

Overview of HV-CMOS devices

Too many chips, just a sample...



R&D developments
Smart and simple pixels
H35 Technology

R&D developments
H18 and 65nm technology

OKI SOI

2006

MU3e Development

ATLAS Pixel Development CCPD (H18)

CLIC Development (H18)

ATLAS Strip Development (H35)

ATLAS Pixel Development (H35)

99% efficiency

Thinned chips

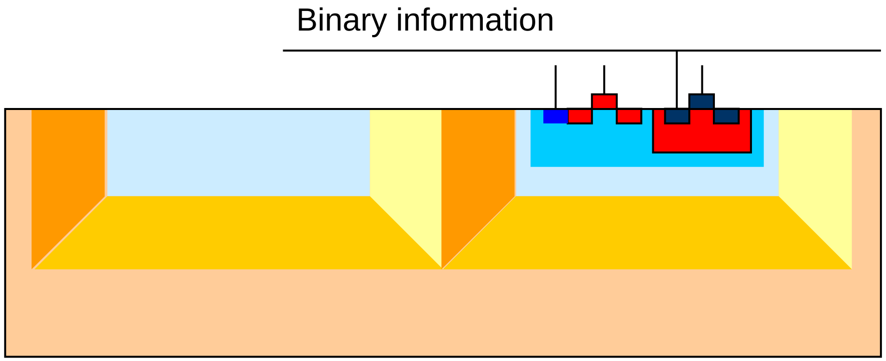
Irradiated chip

The beginning: proof of concept prototypes

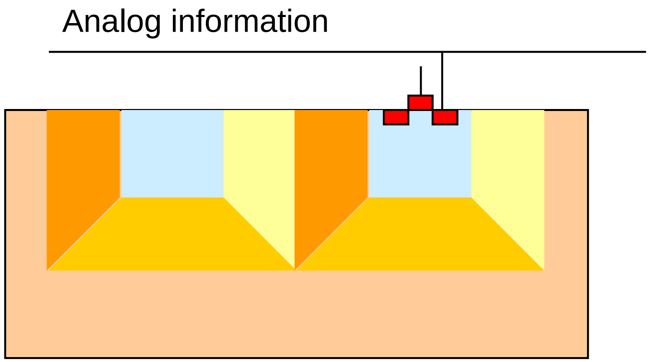
- Several early test-chips by Ivan Peric (many in AMS 350 nm HV-CMOS process)

SDA with sparse readout
(“intelligent” CMOS pixels)
HV2/MuPixel chip

→ baseline for µ3e experiment at PSI

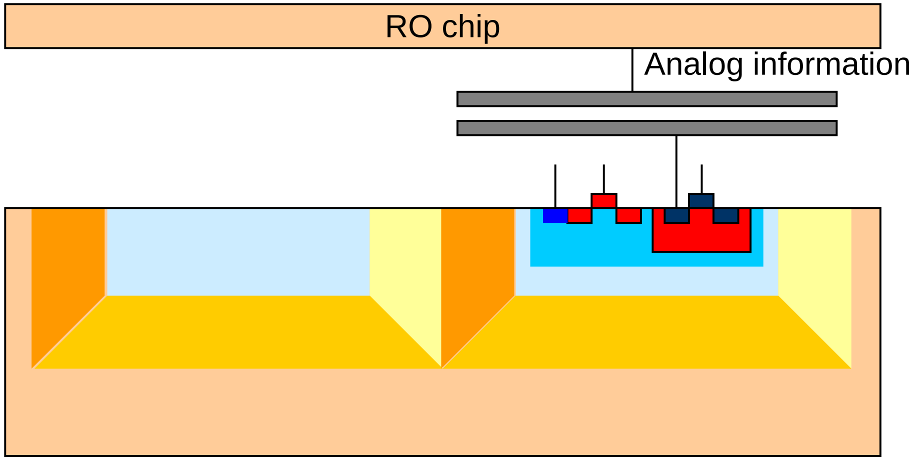


SDA with frame readout
(simple PMOS pixels)
HVM chip



SDA with capacitive readout
(“intelligent” pixels)
Capacitive coupled pixel detectors
CCPD1 and CCPD2 detectors

→ ATLAS and CLIC

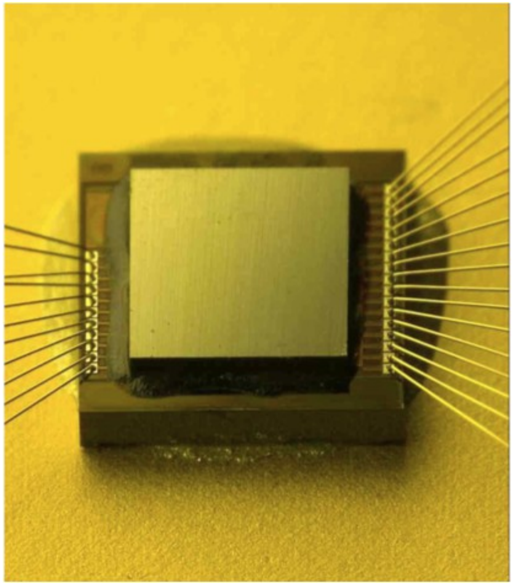


Prototype summaries

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

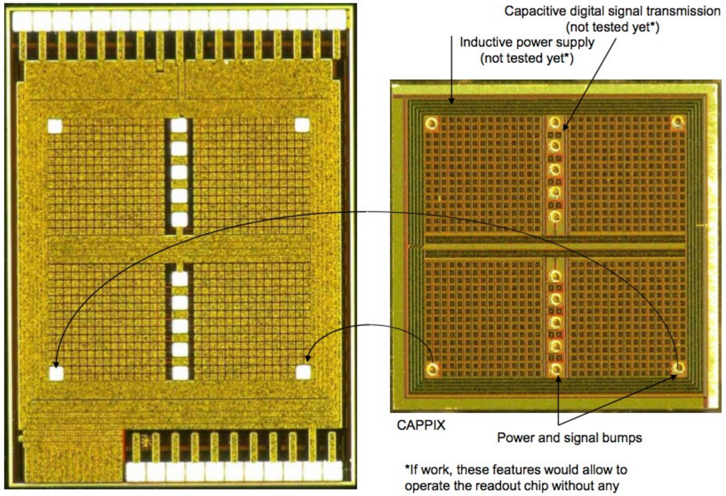
Bumpless hybrid detecto

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e



CCPD2 Chip
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)

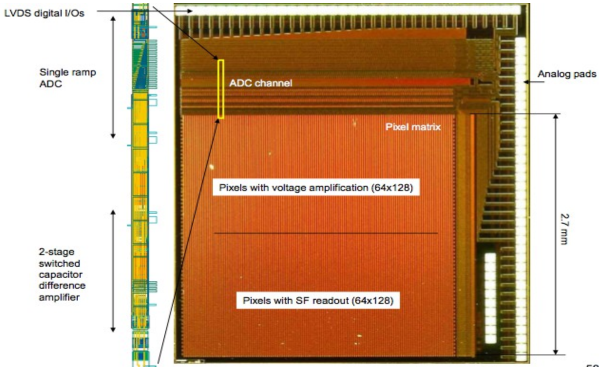


*If work, these features would allow to operate the readout chip without any mechanical contact

Frame readout - monolithic

PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

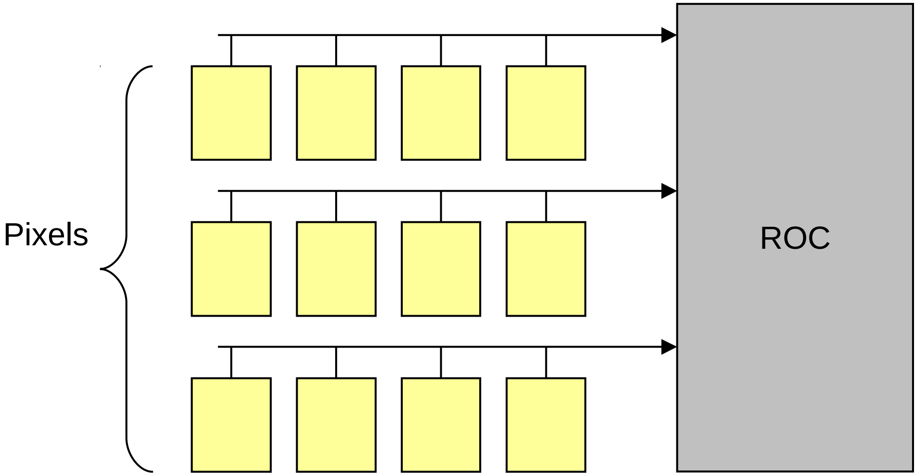
PM2 Chip
Noise: 21e (lab) - 44e (test beam)
Test beam: Detection efficiency 98%
Seed Pixel SNR ~ 27
Cluster Signal/Seed Pixel Noise ~ 47
Spatial resolution ~ 3.8 µm



I. Peric

From MAPS to active sensors

- Existing prototypes were not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits might affect noise performance
- Idea: use HV-CMOS as active sensor in combination with a (possibly modified) existing fast/”LHC” readout chip
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to optimise readout granularity, e.g.
    - (larger) pixels
    - strips

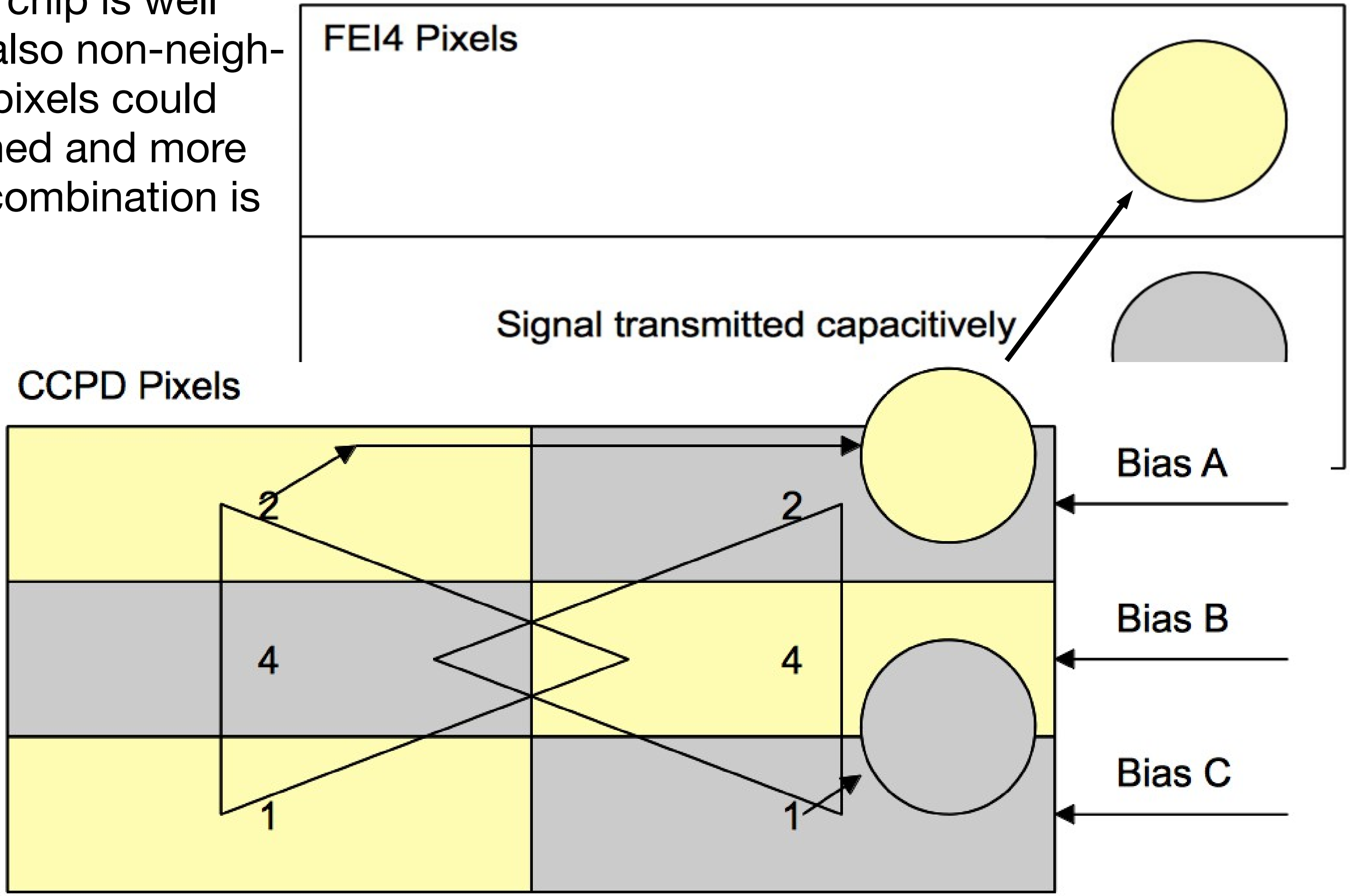


ATLAS: AMS H18 HV-CMOS

- Project initiated by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 180 nm feature size in cooperation with IBM
- "HV2FEI4"-chip:
  - biasing of substrate to ~60-100V possible
  - substrate resistivity ~10 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced N_{eff} insignificant even for innermost layers
  - depletion depth theoretically in the order of 10 μm
    → drift signal ~1 ke^-
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk → avoid clocked circuits
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - "digital" area at the expense of significant inactive edge/balcony
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first

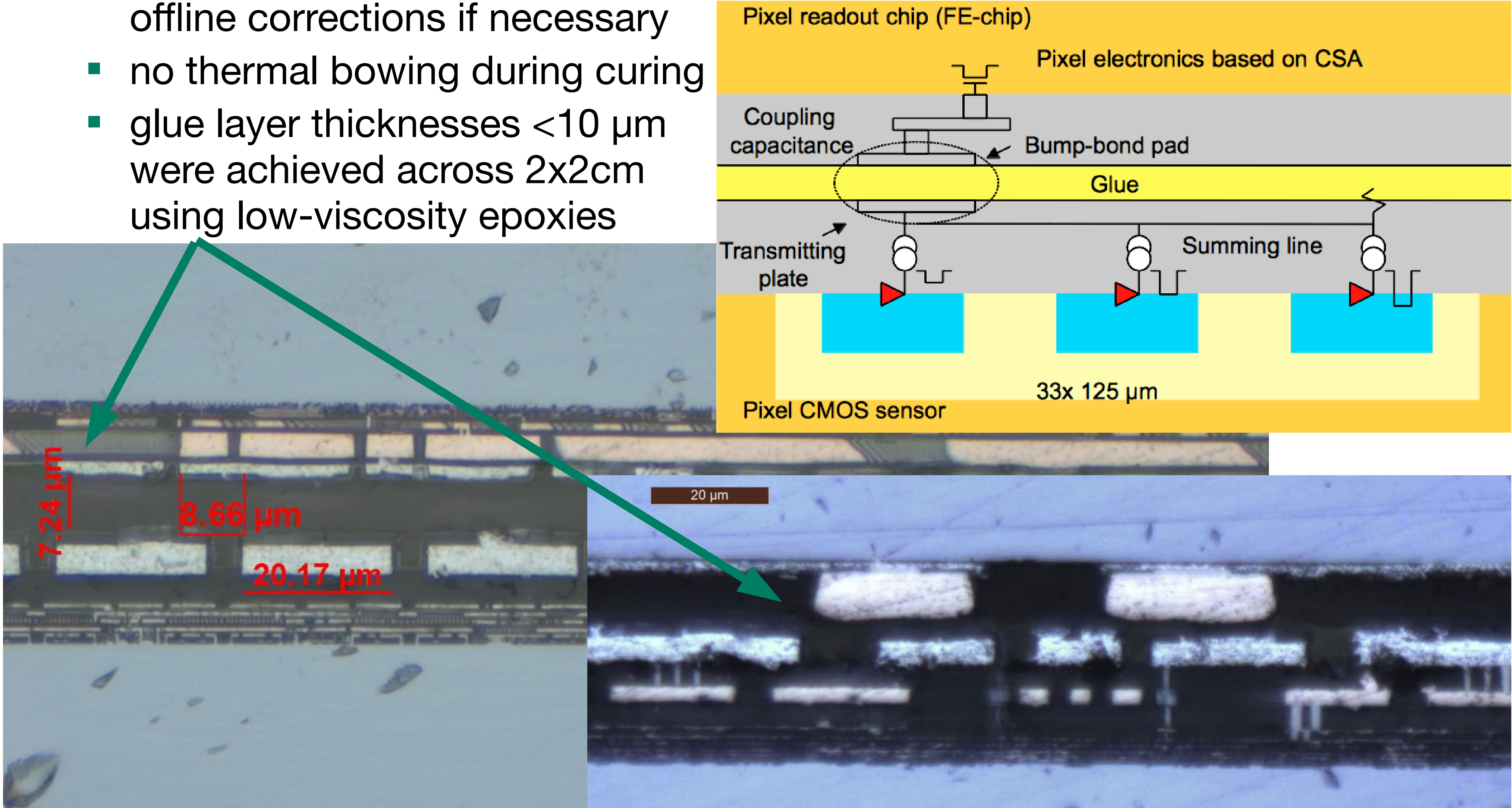
Pixels: sizes and combinations

- Possible/sensible pixel sizes: 20x20 to at most 25x250 µm
  - 50x250 µm (current ATLAS FE-I4 chip) too large
  - combine several sensor “sub-pixels” to one ROC-pixel
    - sub-Pixels encode their address/position into the signal as pulse-height-information instead of signal proportional to collected charge
    - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



Pixels: bonding?

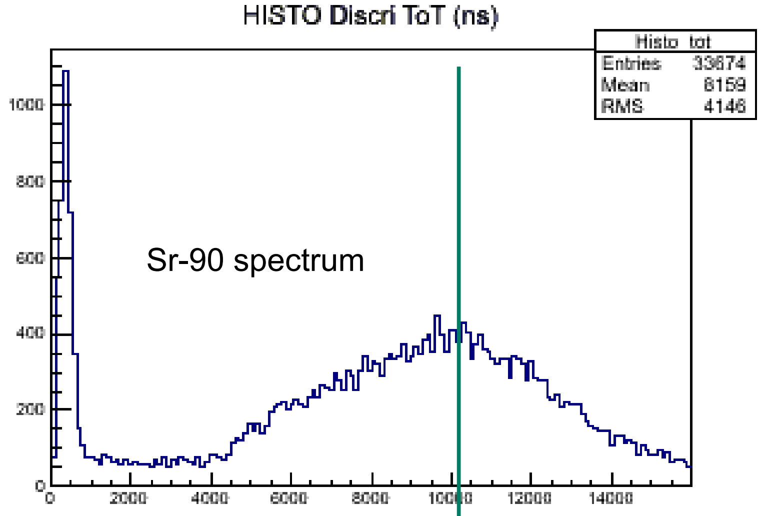
- Bump-bonding expensive and difficult for thin assemblies (bow)
- Alternatives: wafer-to-wafer bonding, gluing
  - amplification possible, hence AC transmission not a problem at all
  - variations in glue thickness can be handled by tuning procedures and offline corrections if necessary
  - no thermal bowing during curing
  - glue layer thicknesses <10 µm were achieved across 2x2cm using low-viscosity epoxies



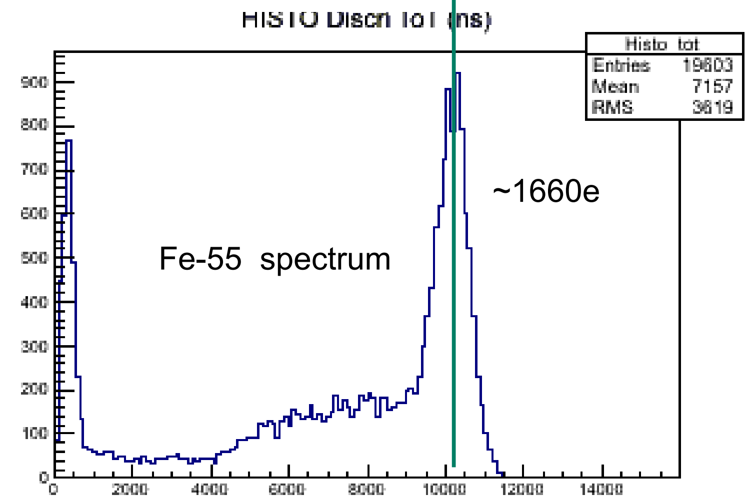
HV2FEI4: standalone characterisation

- Irradiations at CERN/PS, with reactor neutrons and with x-rays
  - on special PCB allowing for remote operation, HV2FEI4 powered and read-out during irradiation

un-irradiated device


HISTO Discri ToT (ns)

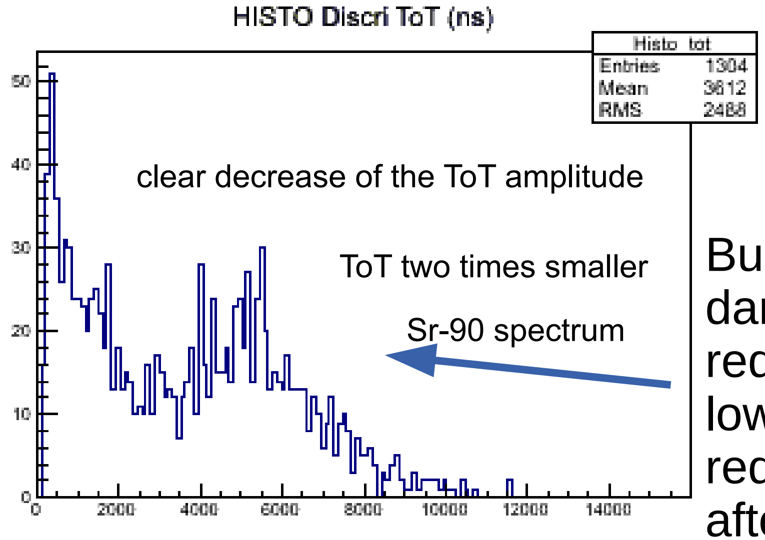
Sr-90 spectrum


HISTO Discri ToT (ns)

Fe-55 spectrum

~1660e

CCPD9 irradiated at 80 MRad

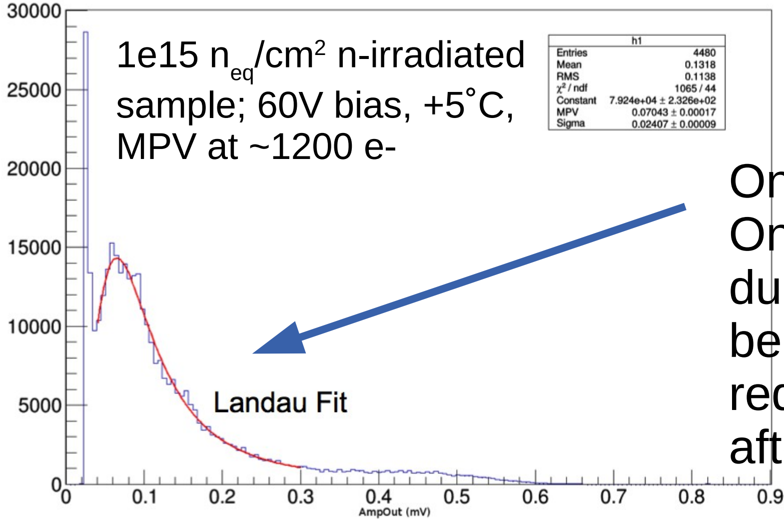

HISTO Discri ToT (ns)

clear decrease of the ToT amplitude

ToT two times smaller

Sr-90 spectrum

Bulk and ionisation damage: mix of reduced signal and lower amplification: reduced to ~50% after irrad


1e15 n_{eq}/cm^2 n-irradiated sample; 60V bias, +5˚C, MPV at ~1200 e-

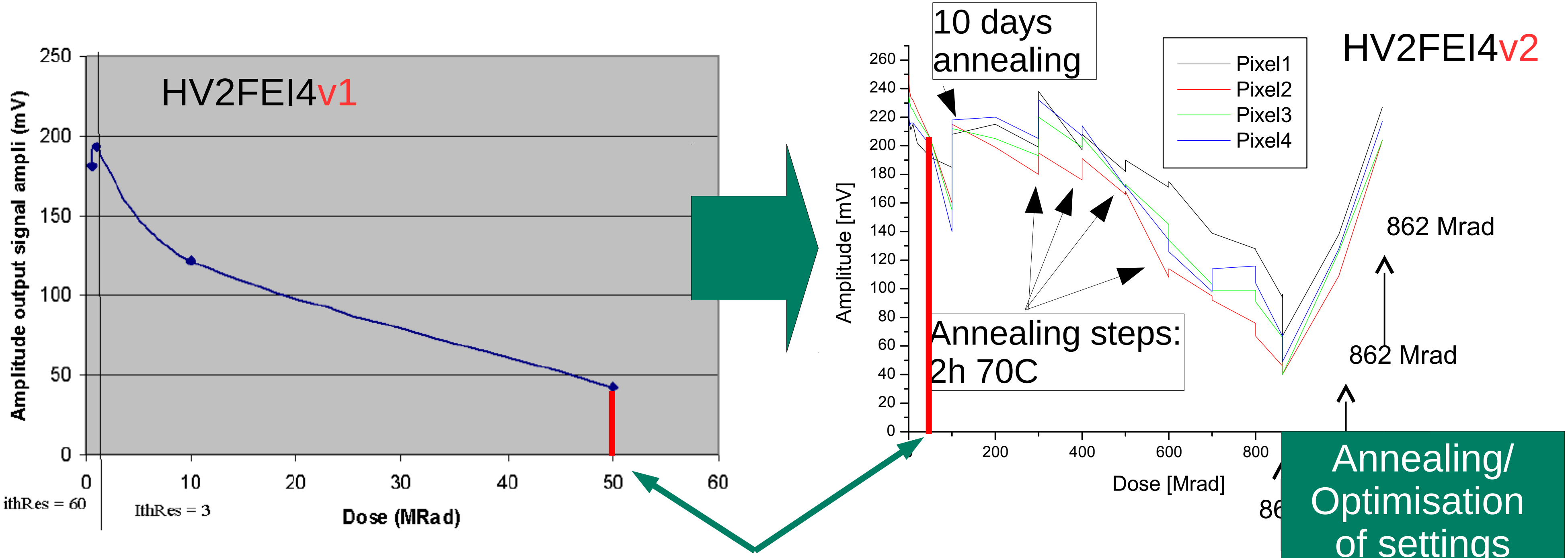
Landau Fit

Only bulk damage: Only loss of signal due to diffusion being eliminated: reduced to ~70% after irrad

HV2FEI4 irradiation: dose effects

- Radiation effects due to dose, could be reproduced by x-ray irradiation
  - HV2FEI4v1: deliberately rad-soft/standard design to see how far it lasts
  - HV2FEI4v2: different rad-hard designs (guard rings, circular transistors, ...)
- Signal amplitude clearly much more stable
  - irradiated up to 862 Mrad (!), drop visible after ~500 MRad
    - dose rate effect, annealing brings signal back to ~100%

→ rad-hardness significantly improved, hadron irradiations to follow



10 days annealing

Annealing steps: 2h 70C

862 Mrad

862 Mrad

Annealing/ Optimisation of settings

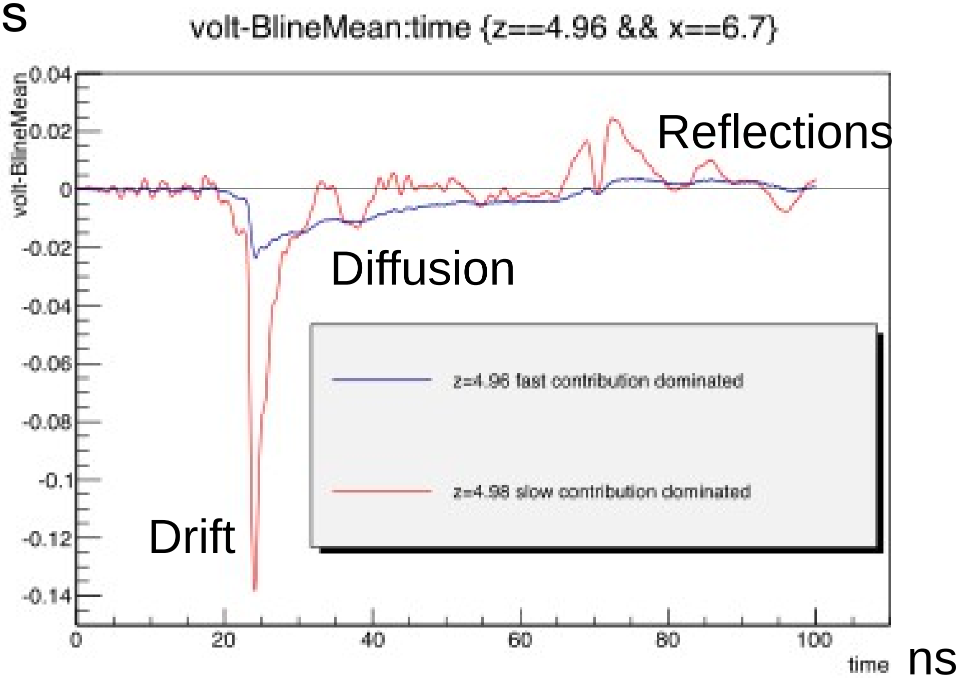
50MRad

HV2FEI4v1 irradiated with x-rays
Amplifier gain loss

HV2FEI4v2 irradiated with x-rays
Amplifier gain loss
Rad hard pixels

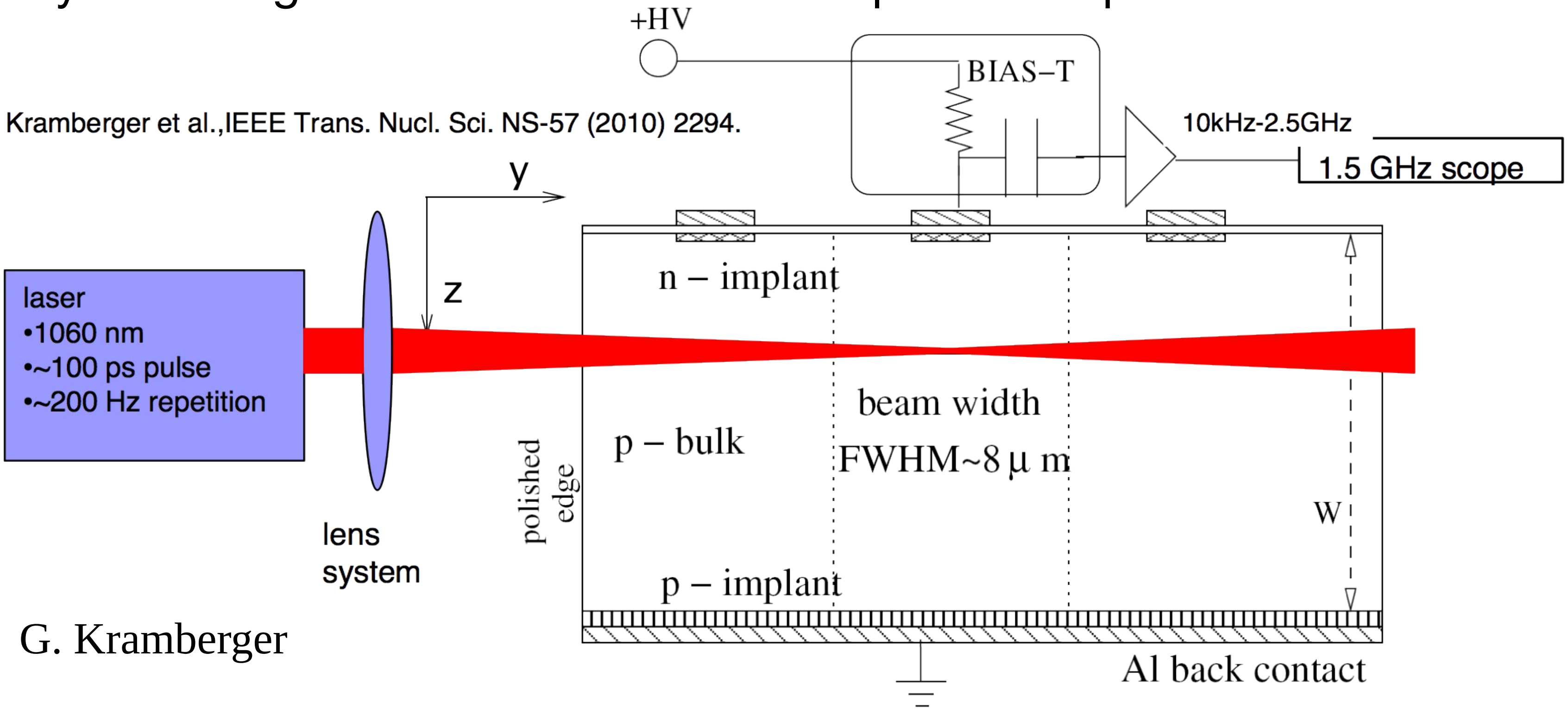
HV2FEI4 irradiation: fluence effects

- Numerically, depletion depth for 10 Ohm*cm substrate is about 10 µm at 100V of bias
  - Classically, this should yield less than 800 electrons of collected charge
  - We observe ~1500-1900 e⁻ before irradiation – large diffusion component?
  - Still ~1200 e⁻ after irradiation to 1e15 neq/cm2 using (slow) in-pixel charge-sensitive amplifiers
    - Diffusion should be ruled out at that fluence, other effects?
- → Edge-TCT
  - can distinguish (fast) drift from (slow) diffusion
  - can measure charge collection zones
- Variables
  - Transients (Current vs. time)
  - Integrals (Charge vs. position)



What is edge-TCT? → see G. Kramberger's talk

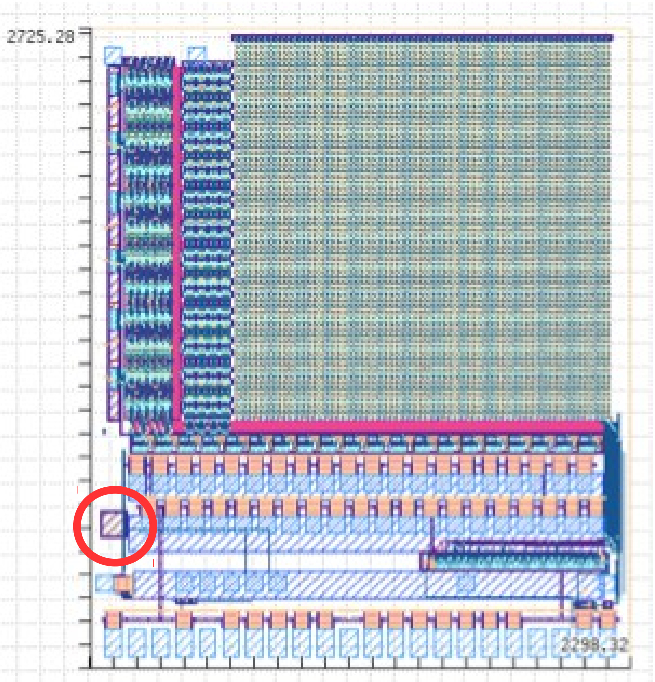
- TCT: Transient Current Technique, i.e. observe the time-resolved charge collection generated by MIP, alpha or laser pulse
  - usually lasers are used because of their constant charge deposition per pulse → can average many samplings, get rid of noise
  - can scan the sensor to study inter-pixel boundary efficiencies etc.
  - short signals, so charge-sensitive preamps usually too slow, need fast current-based amplifiers → external, discrete, specialised amps
- edge: shooting in through the side-wall of the sensor with a IR laser
  - can study the charge collection at different depths → depletion?

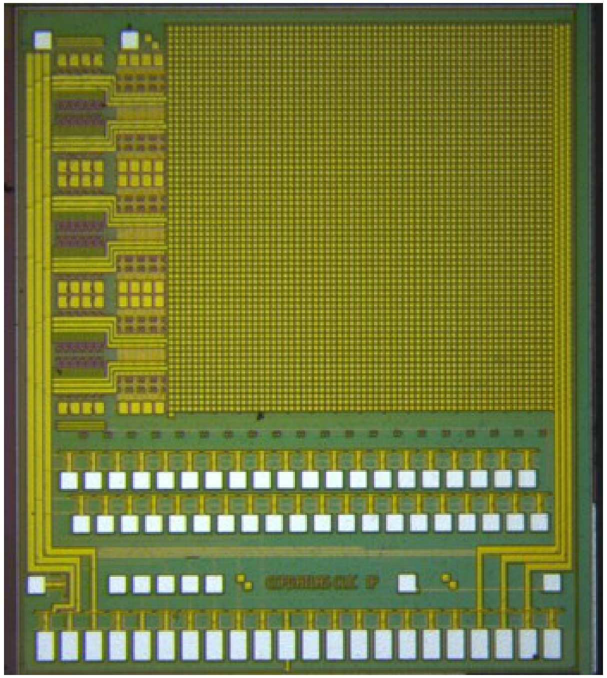


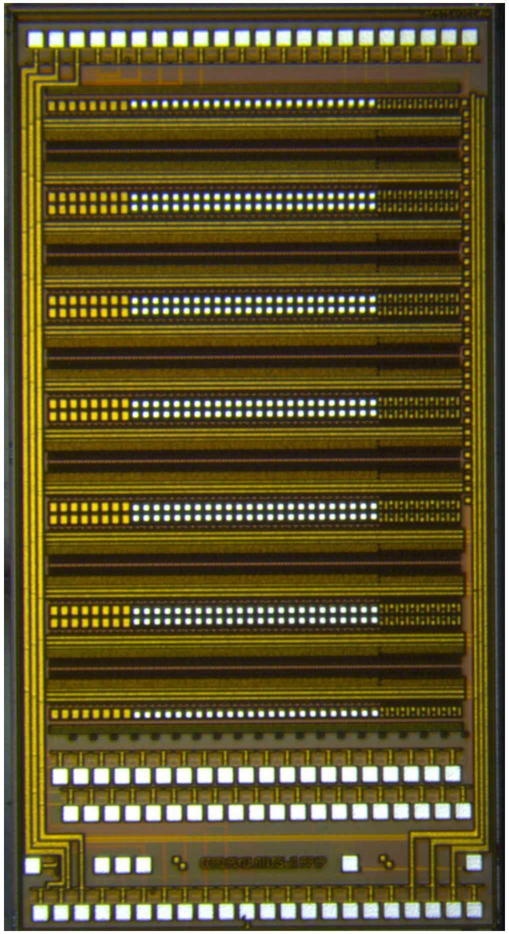
G. Kramberger et al.,IEEE Trans. Nucl. Sci. NS-57 (2010) 2294.

Samples

- Measurements on AMS H18 HV2FEI4 v2 and v3
  - v2: Only charge-sensitive preamplifier output accessible
    - 33 x 125 µm pixel with full electronics
    - very slow risetime compared to expected signal collection time
    - difficult assessment of drift/diffusion contribution
  - v3: one dedicated passive 100 x 100 µm diode accessible
    - no neighbours, so beware of edge effects
    - also irradiated samples available, for today: 1e15 neq/cm2

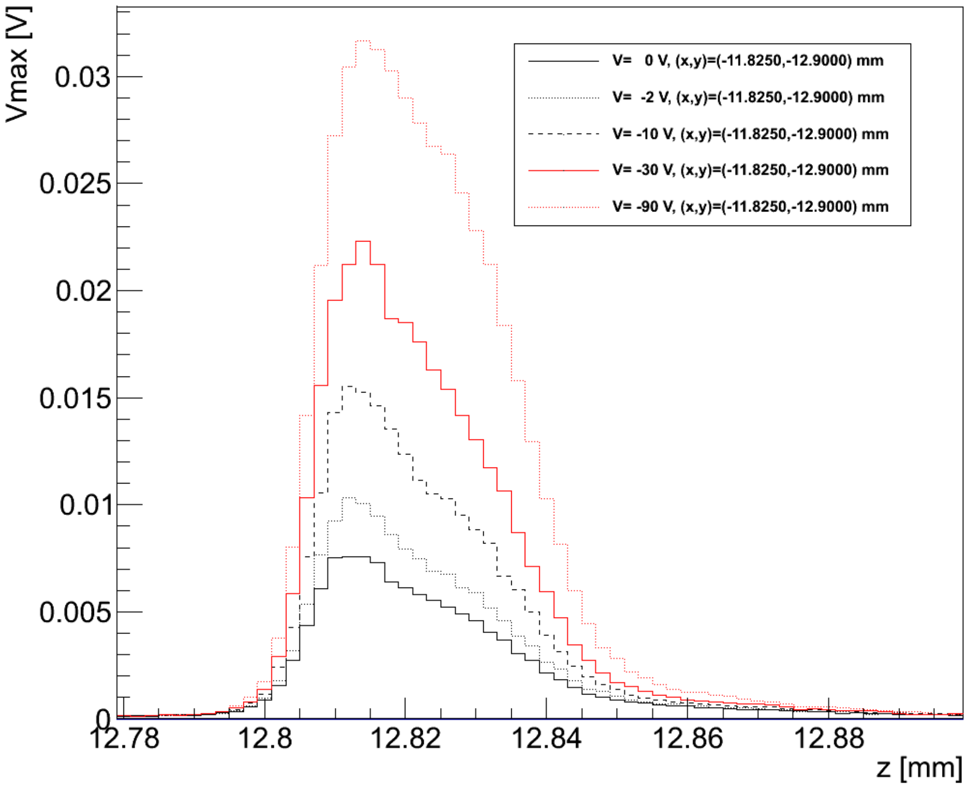


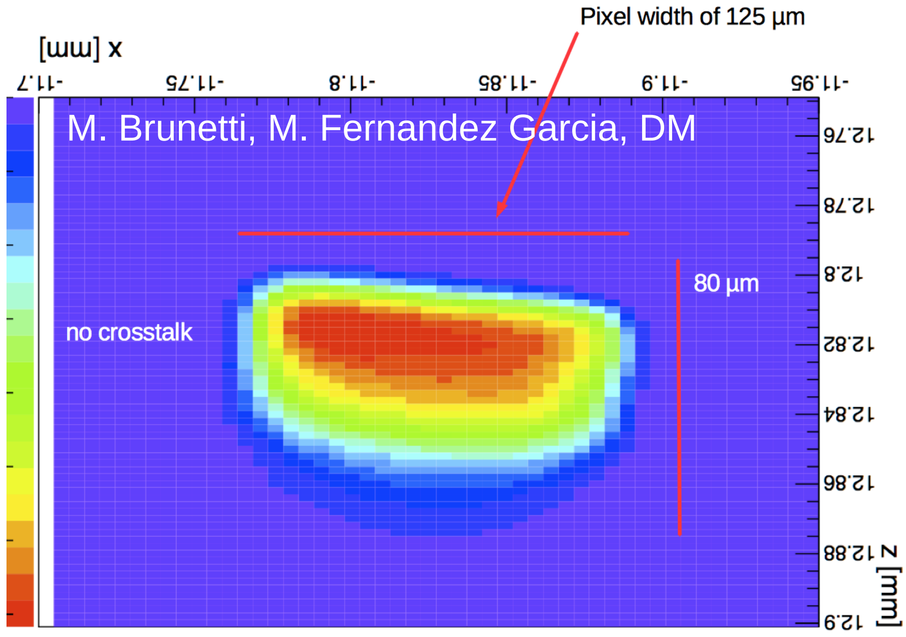




v2 results: CERN/UniGe

- First measurements in 2013
- Find full pixel length, extension of charge collection zone up to almost 80 µm depth with significant contributions to 20-30 µm
- Were not able to determine any significant change in signal risetime to distinguish between drift and diffusion





Pixel width of 125 µm

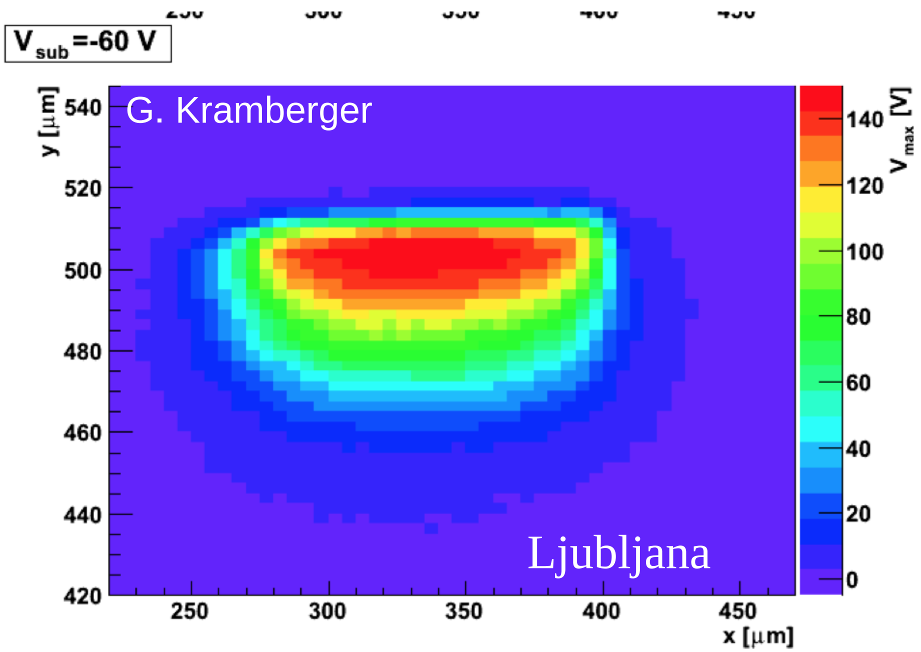
M. Brunetti, M. Fernandez Garcia, DM

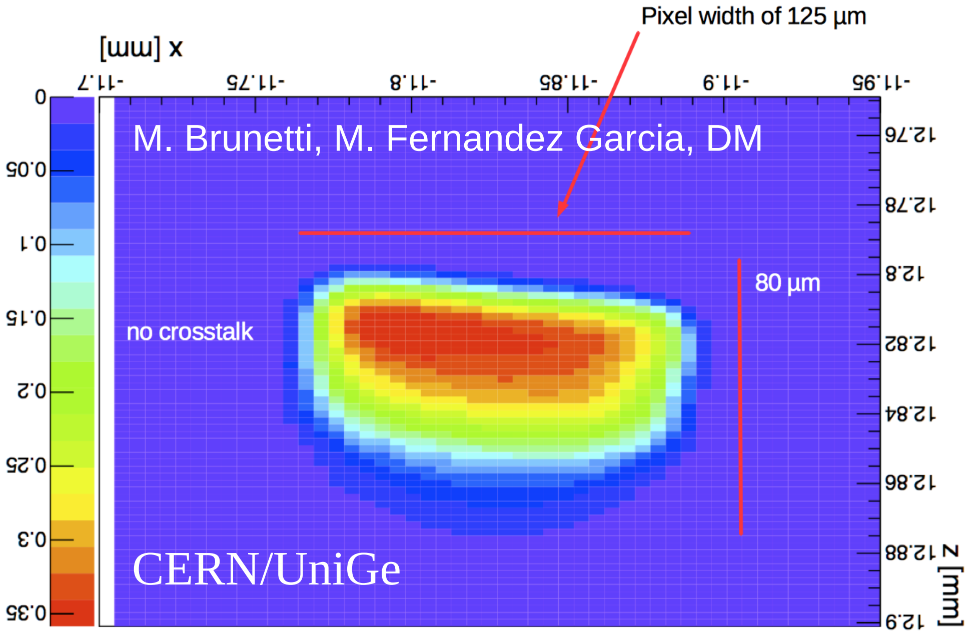
no crosstalk

80 µm

v2: Ljubljana

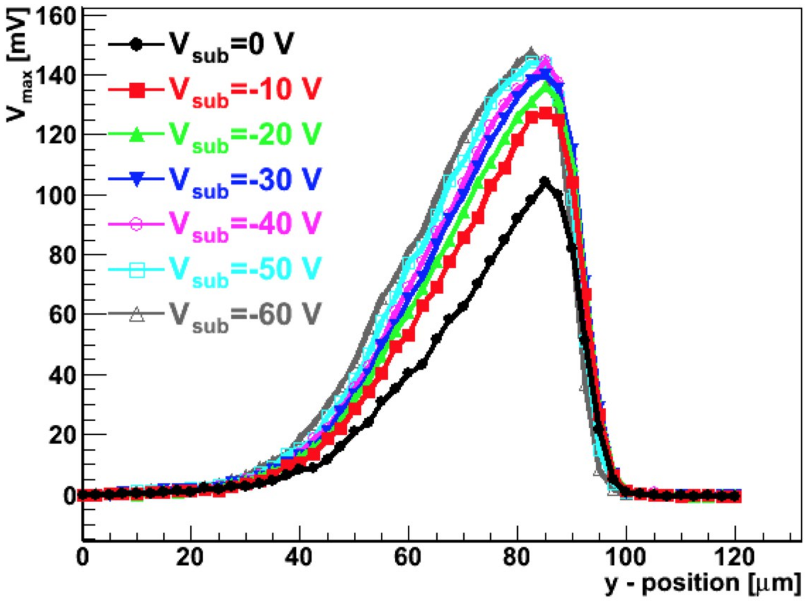
- Gregor Kramberger repeated the measurement, additional analysis effort

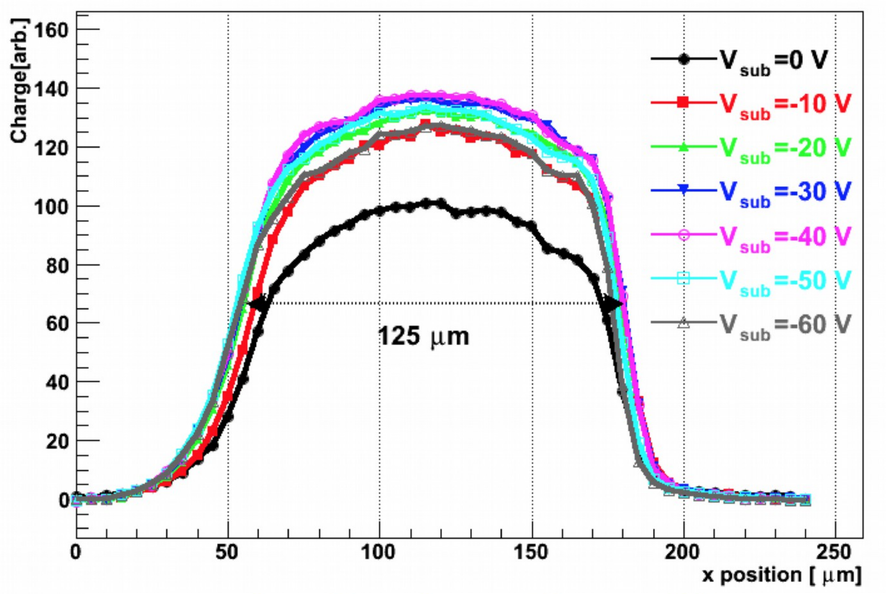


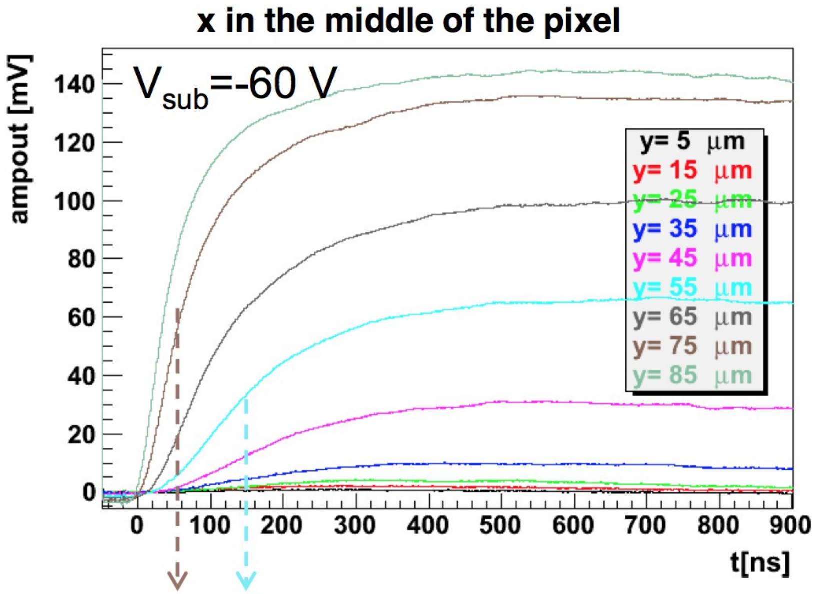


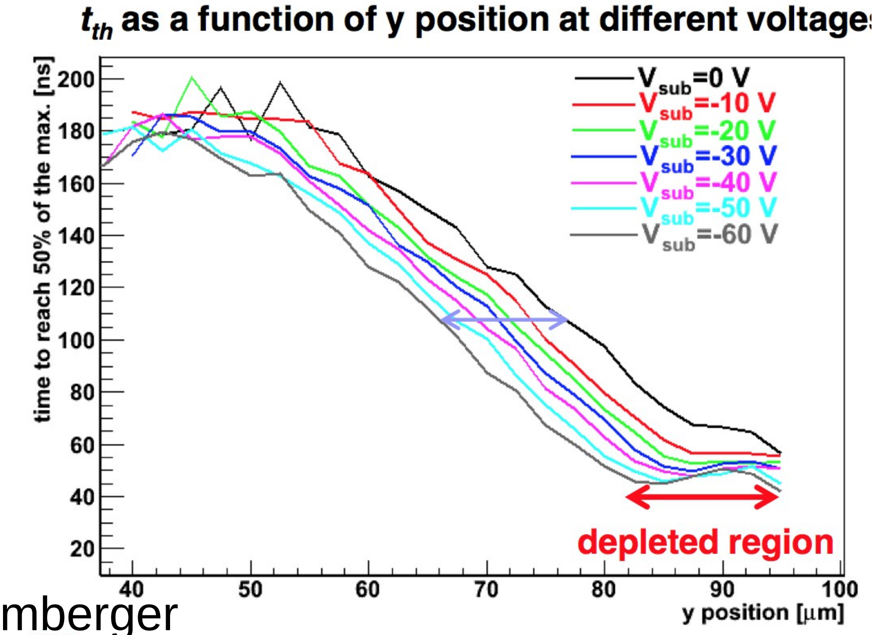
v2: Ljubljana

- Improved analysis effort: time to reach 50% of the charge





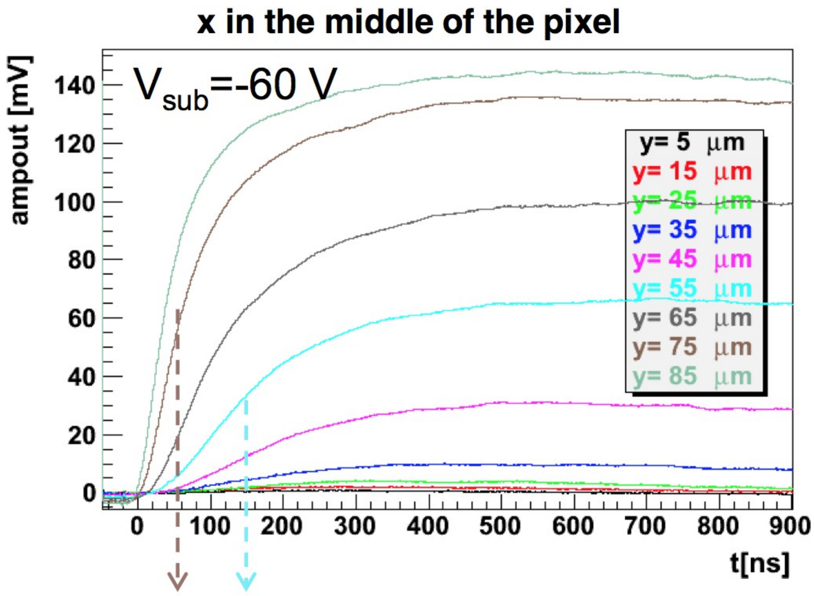

x in the middle of the pixel

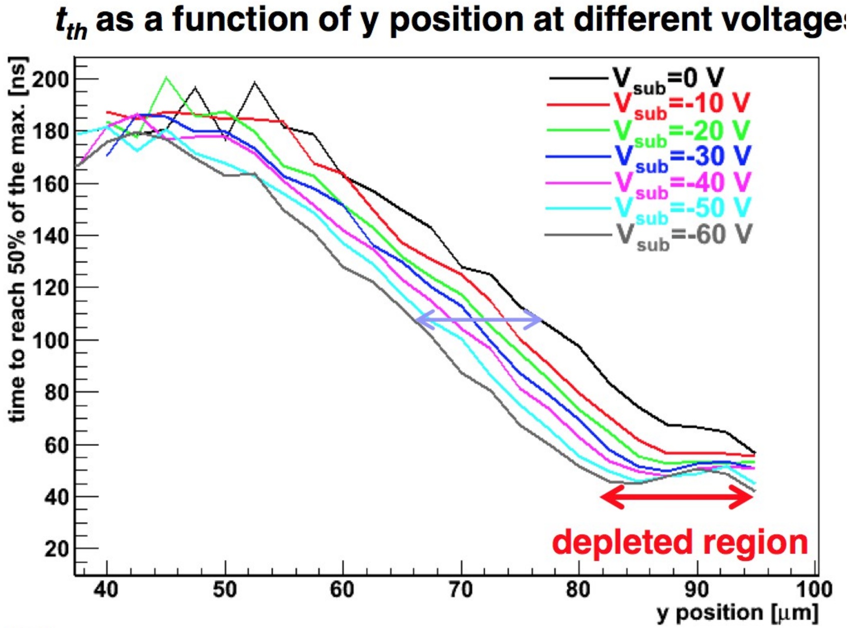

t_{th} as a function of y position at different voltage

G. Kramberger

v2: Ljubljana

- Repeated measurement, but additional analysis effort: time to reach 50% of the charge
- Conclusions:
  - ~7µm depletion zone
  - 35% of signal due to drift at -60V
- Rather indirect way of measurement, so…

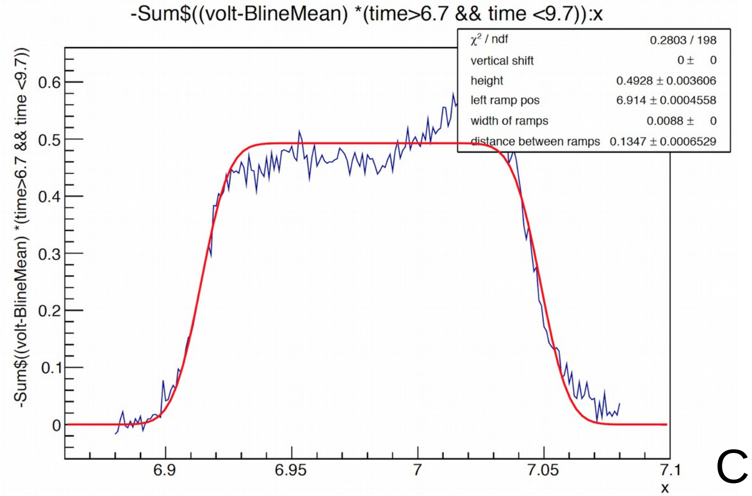




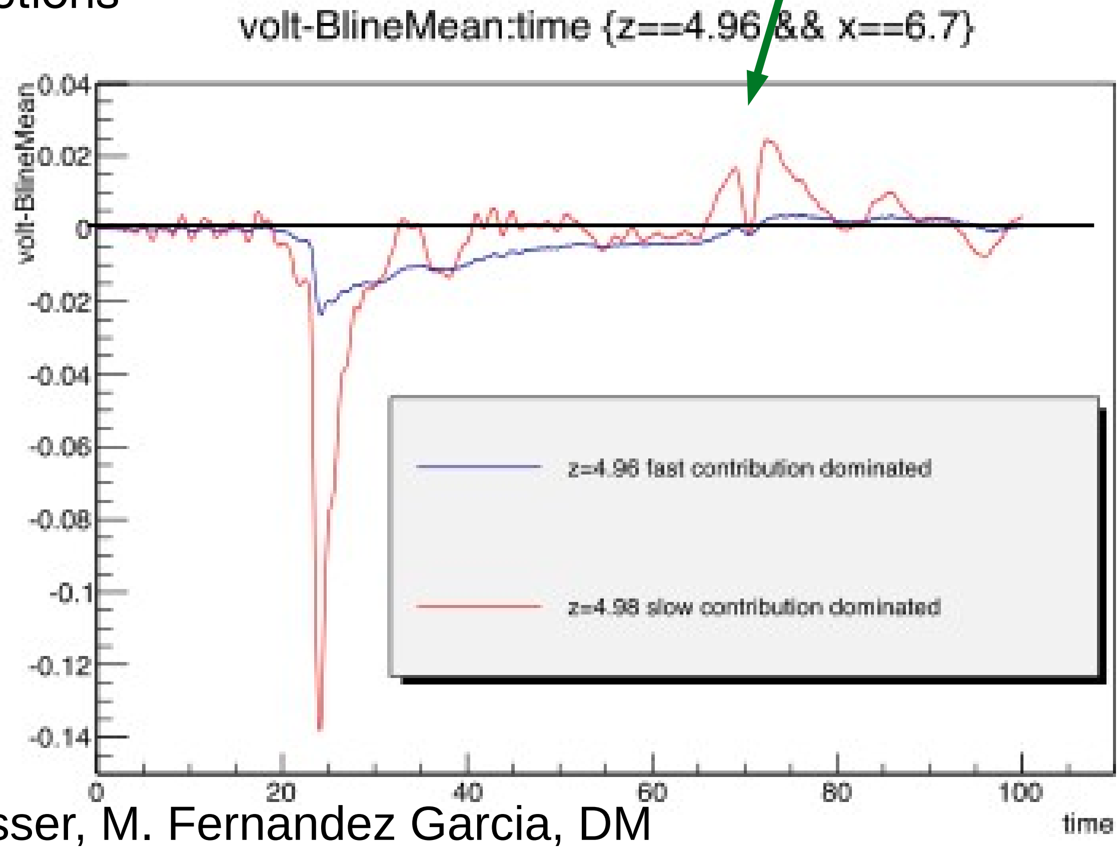
G. Kramberger

v3

- Direct access to 100 x 100 µm passive diode, outside of matrix, no direct neighbours
- used different high-bandwidth (GHz) current-sensitive amplifiers
  - keep in mind that now the transient is current, integral is charge
  - do suffer from non-matched impedaces → many reflections
    - working on an improved PCB, put 5m cable in between → big reflection after 50ns
    - diffusion slow, not many reflections
- Divided contributions:
  - fast: <~ 3ns
  - slow: 3-~70ns
- Laser width: ~9 µm (x-scan)



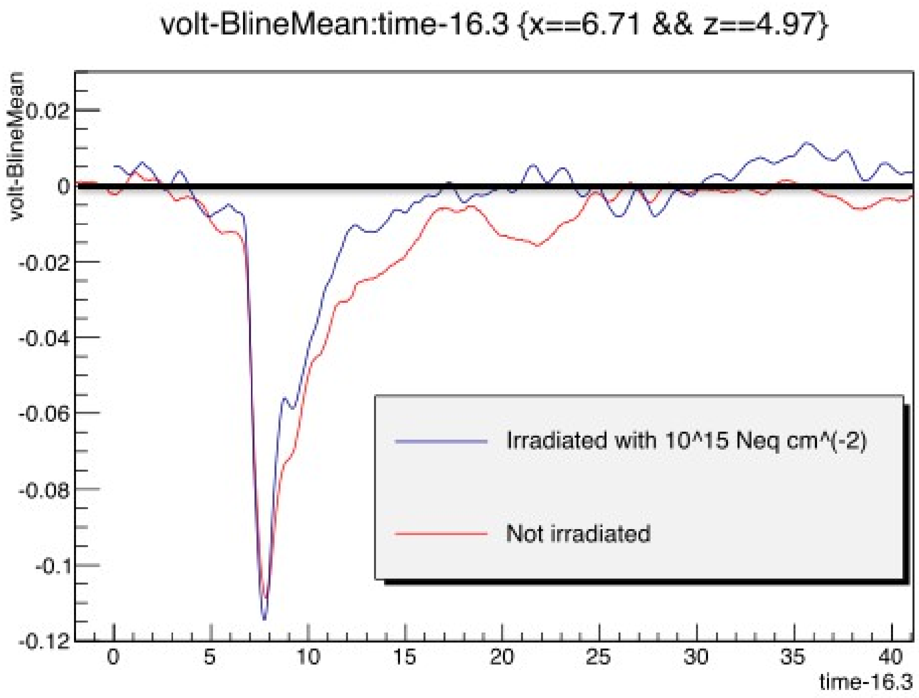
χ^2 / ndf	0.2803 / 198
vertical shift	0 ± 0
height	0.4928 ± 0.003606
left ramp pos	6.914 ± 0.0004558
width of ramps	0.0088 ± 0
distance between ramps	0.1347 ± 0.0006529

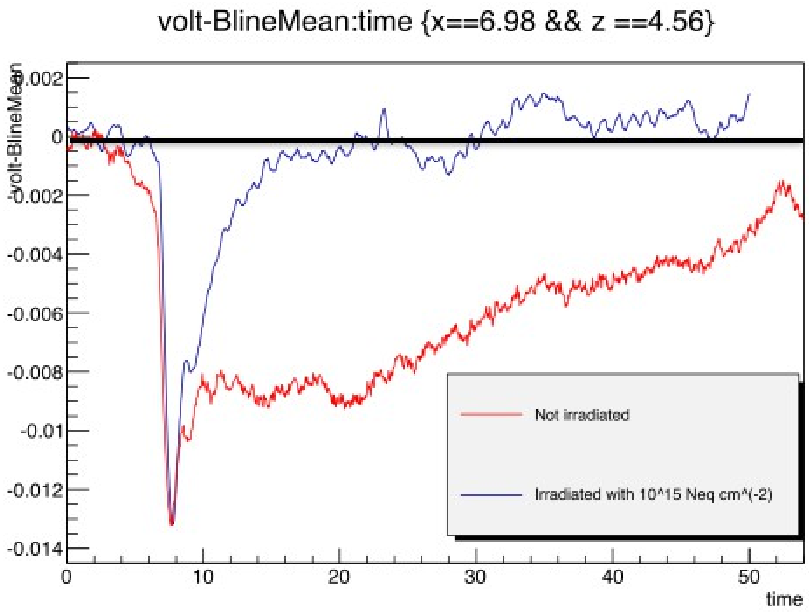


C. Weisser, M. Fernandez Garcia, DM

v3

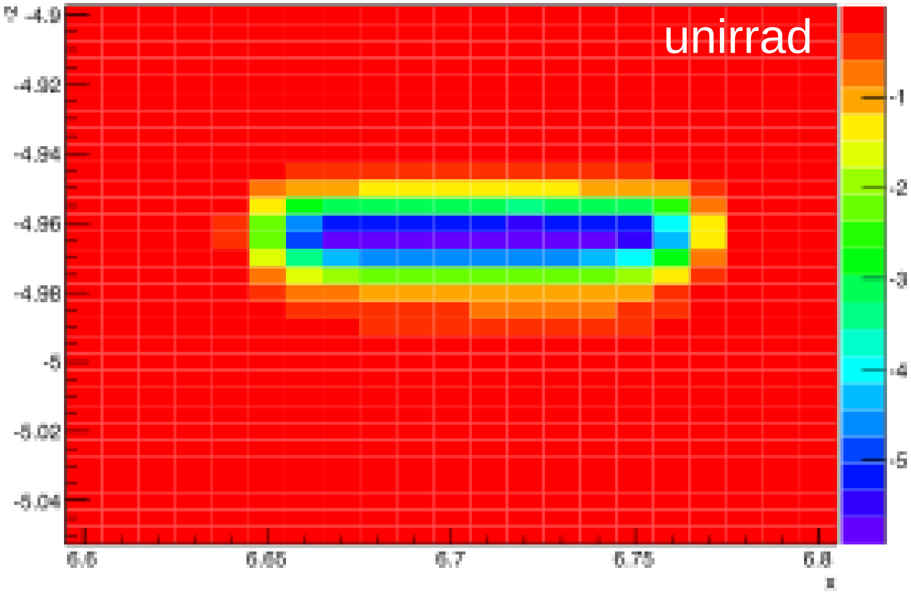
- Comparing transients
- Top: inside drift zone
  - similar, irradiated returns to baseline faster → less signal? Small diffusion component from lateral diffusion?
- Bottom: inside diffusion zone
  - smaller absolute scale!
  - lots of slow diffusion before irradiation, only some drift after irradiation

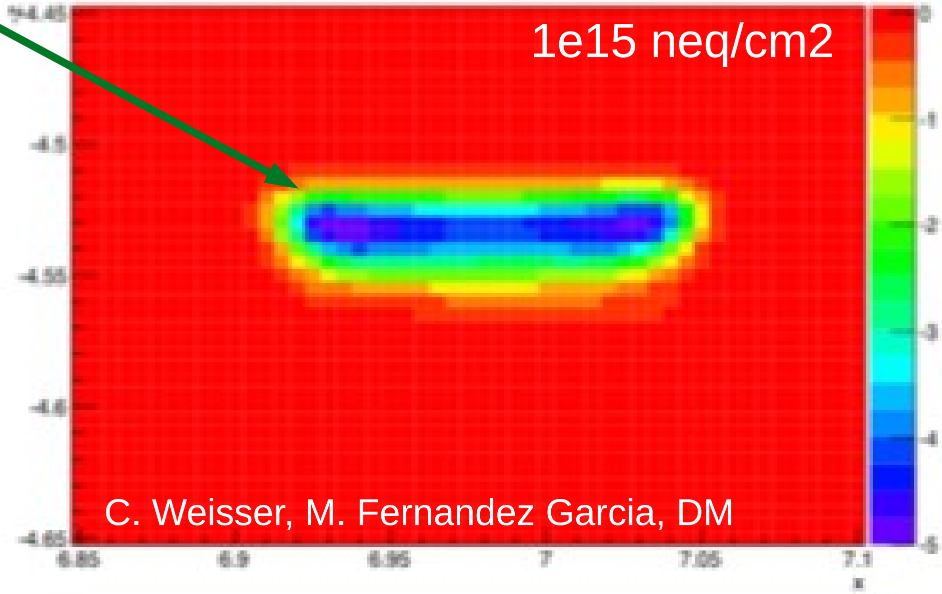




v3

- XZ-scans:
  - **Fast signal** integral as color
  - both at -60V and at room temperature
- Top: unirradiated
- Bottom: 1e15 neq/cm2 n-irrad
- Key observations
  - look very similar
  - no significant reduction
  - post-irrad shows “hotspots”
    - peaks in electric field? Charge amplification?





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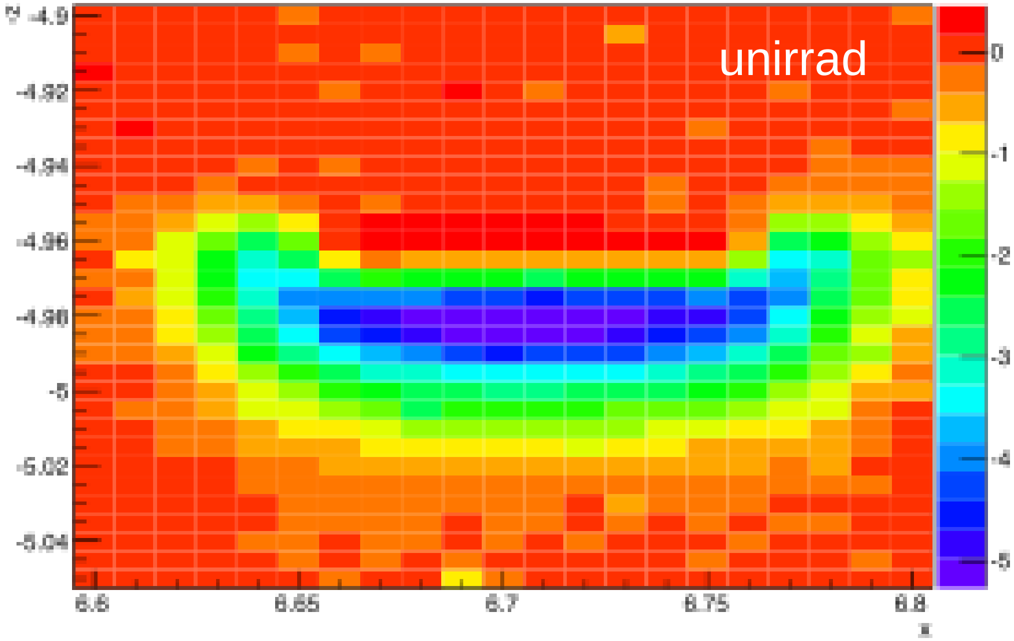
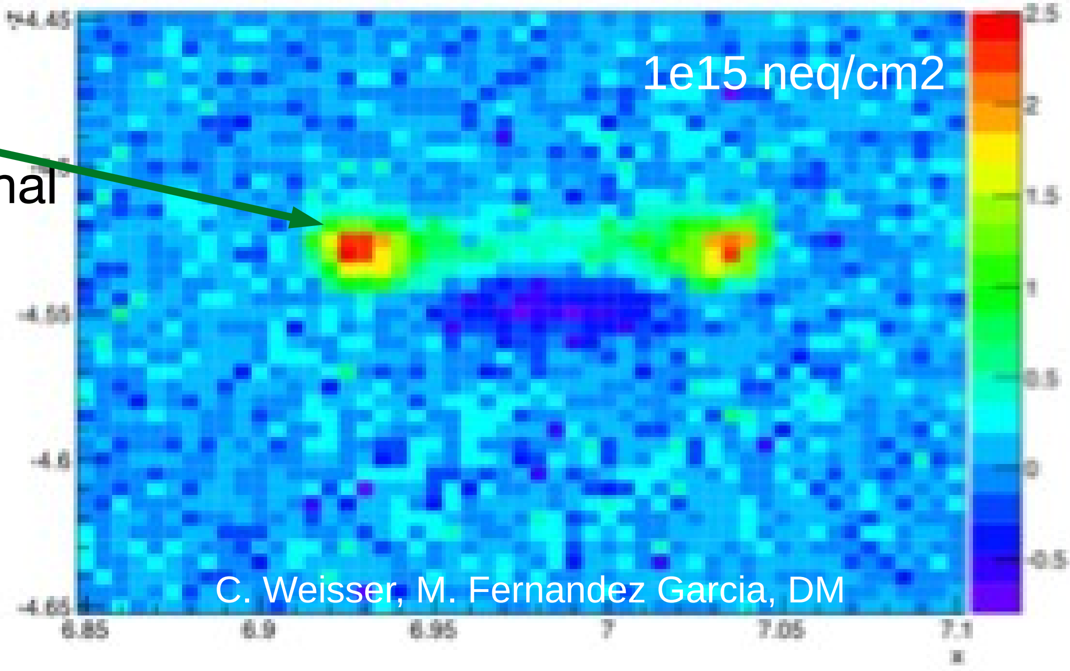
v3

- XZ-scans:
  - **Slow** integral as color
  - both at -60V and at room temperature
- Top: unirradiated
- Bottom: 1e15 neq/cm2 n-irrad
- Key observations
  - extended diffusion zone underneath and laterally of drift zone before irradiation
  - diffusion (almost) gone after irradiation, red spots are undershoots from fast drift signal → artifacts





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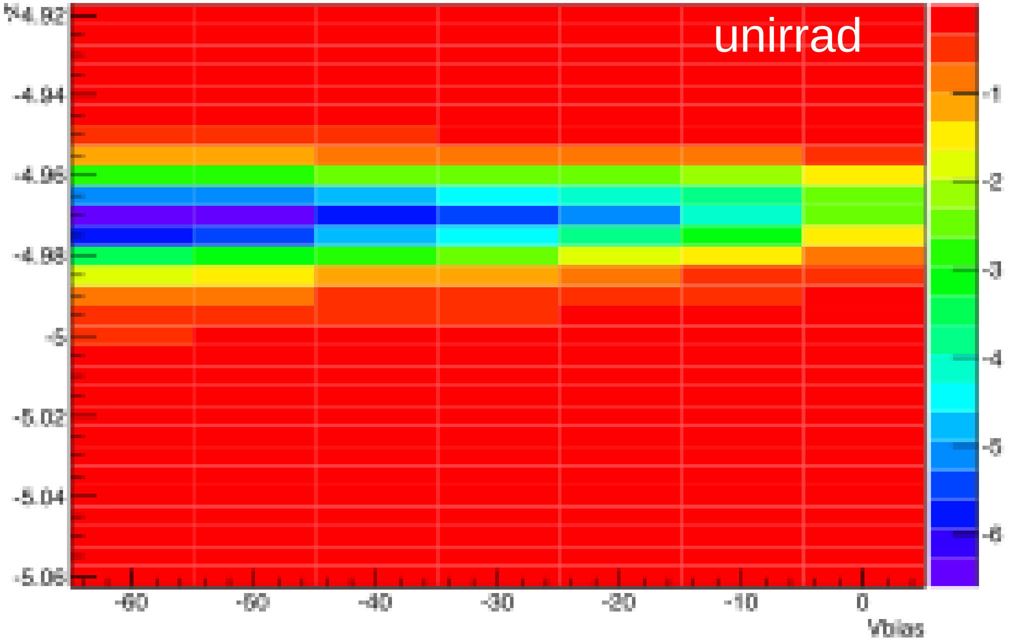
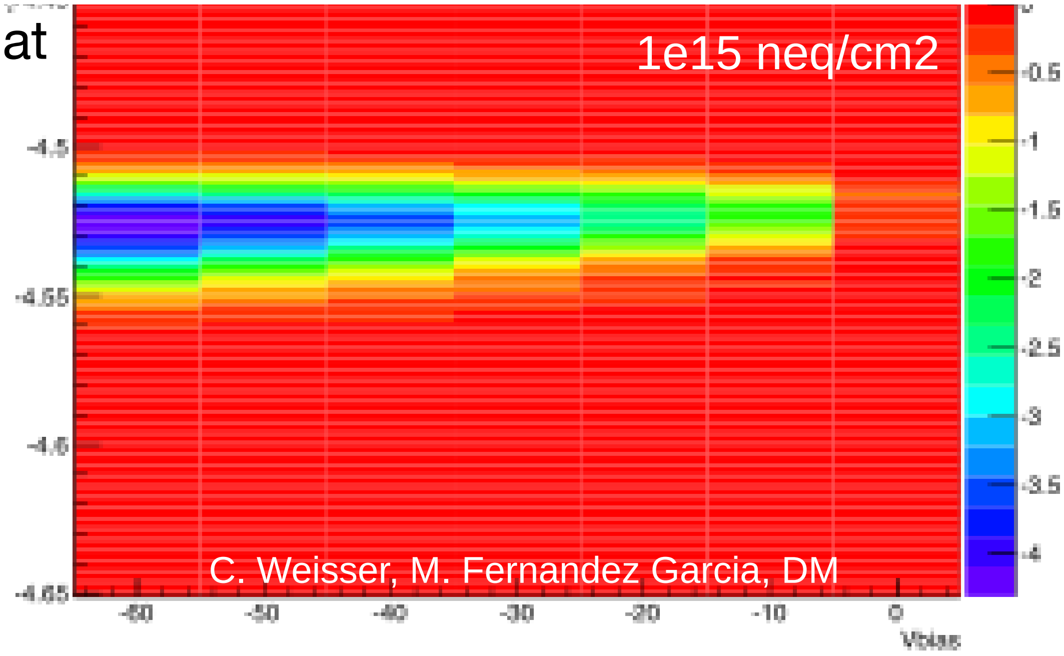
v3

- ZV-scans:
  - **Fast** integral as color
  - between 0V and -60V
- Top: unirradiated
- Bottom: 1e15 neq/cm2 n-irrad
- Key observations
  - zone of large drift signal extends
    - to be convoluted with the 9 μm sigma of the laser!
    - working on deconvolution
  - afer irradiation very little signal at 0V – otherwise very similar...
    - rad-hard?





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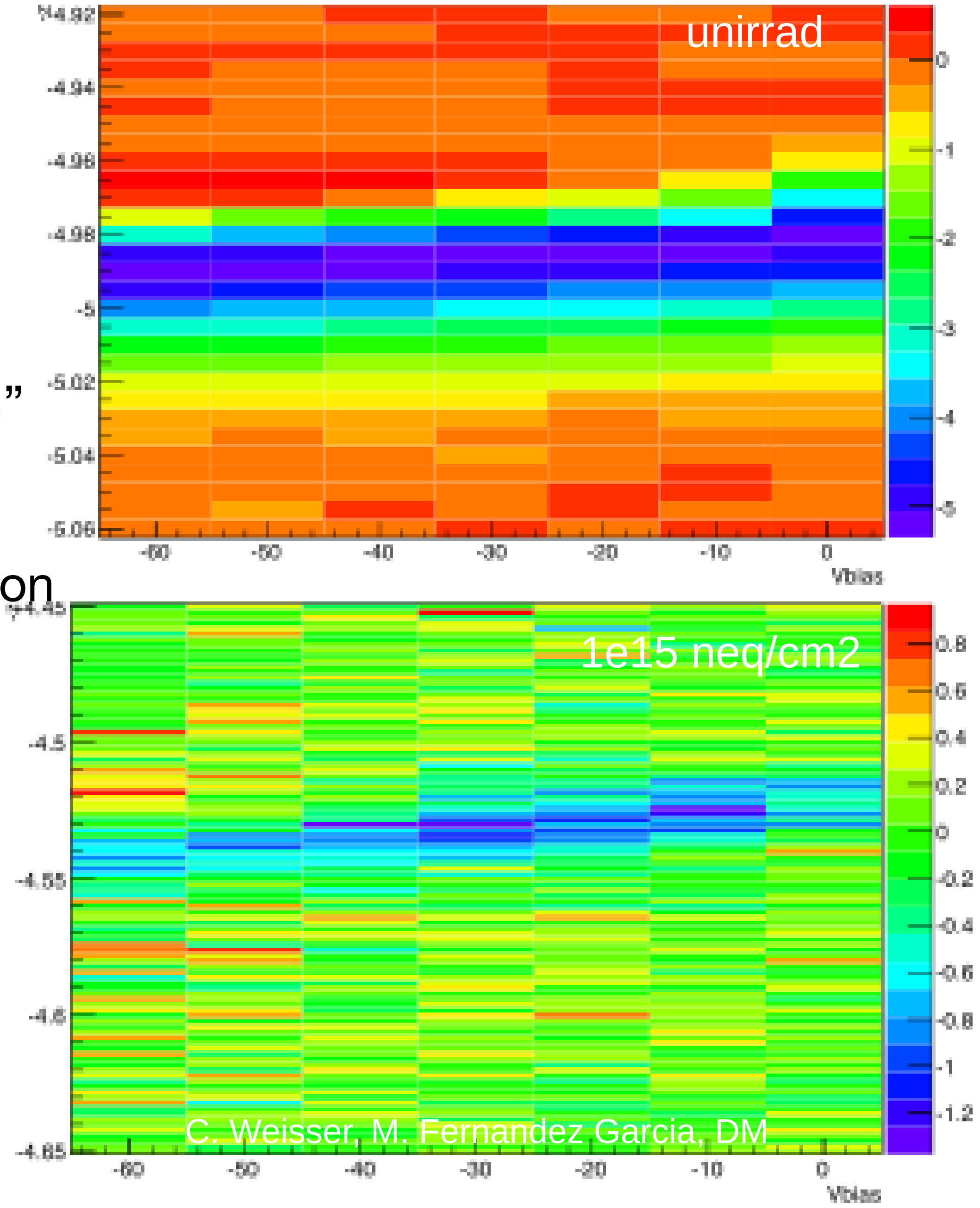
v3

- ZV-scans:
  - **Slow** integral as color
  - between 0V and -60V
- Top: unirradiated
- Bottom: 1e15 neq/cm2 n-irrad
- Key observations
  - diffusion zone is “pushed down” from growing drift zone, but thickness stays ~constant
  - very little diffusion after irradiation (different color code!)



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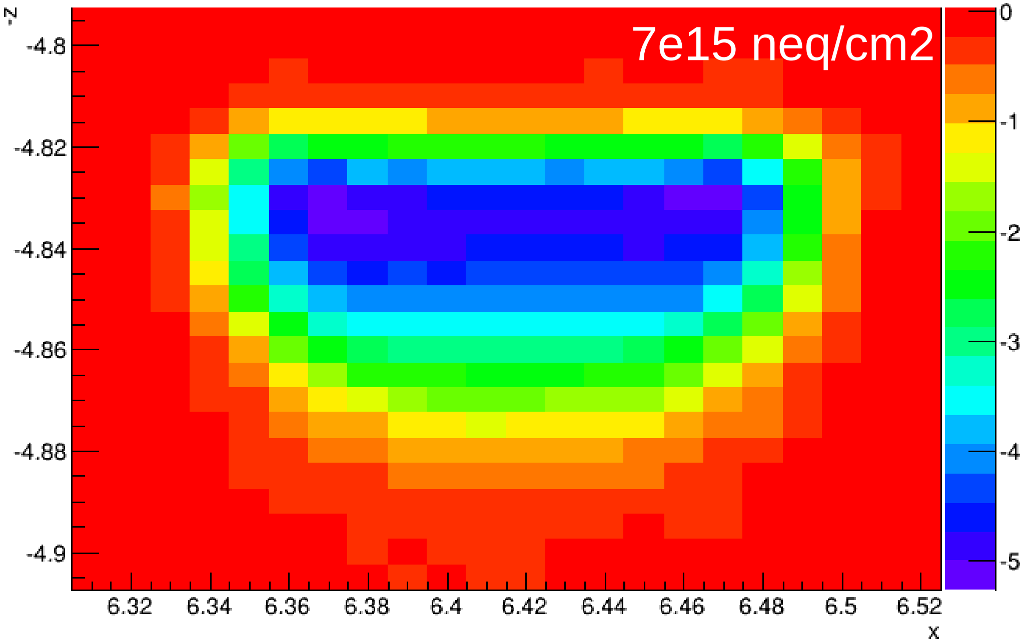
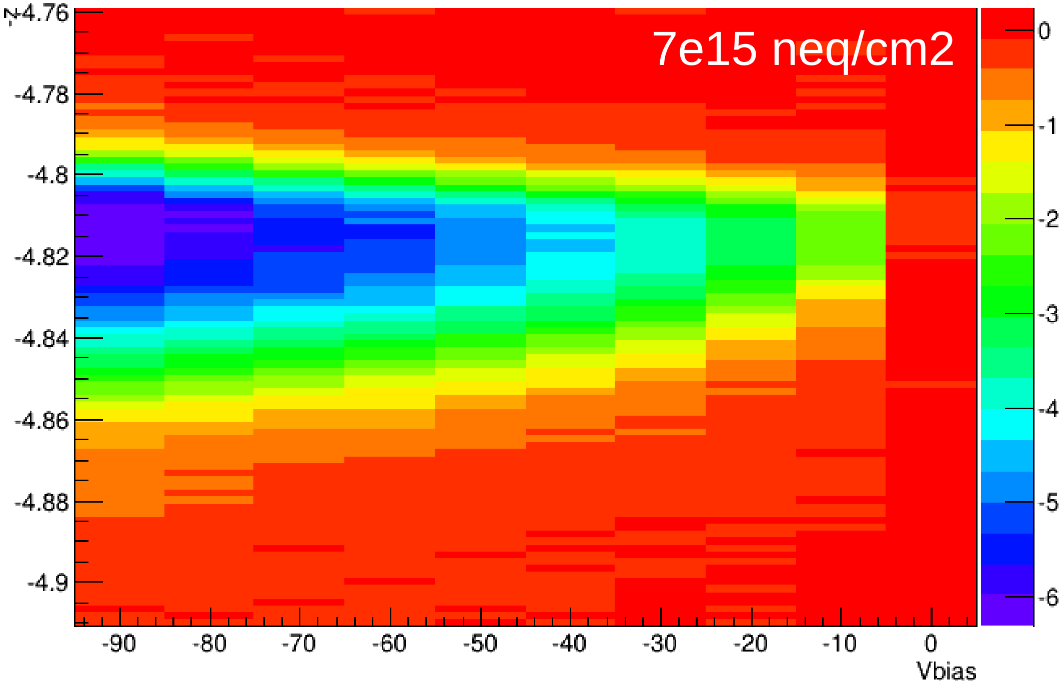
v3 – higher fluences

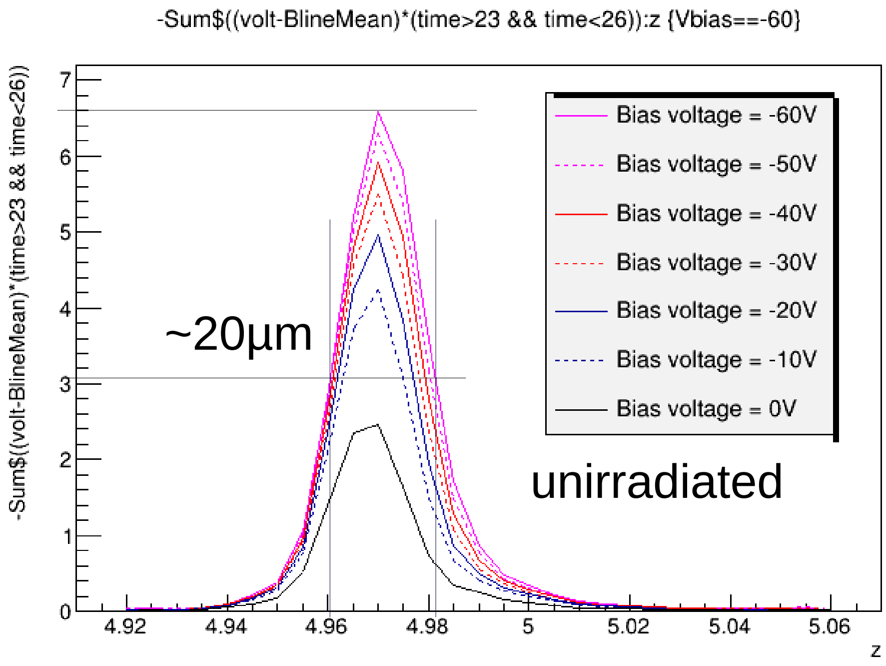
- 1e15 neq/cm2 measurements still done at RT w/o cooling
- 7e15 neq/cm2 only stable until ~25V, then cooling required
  - also reaches “defined” breakdown voltage of ~93V, no change
  - 3ns integral charge ~unchanged wrt to 1e15 neq/cm2 sample
  - peaks in collected charge at edges of implant – high field regions?
- 2e16 neq/cm2 sample next

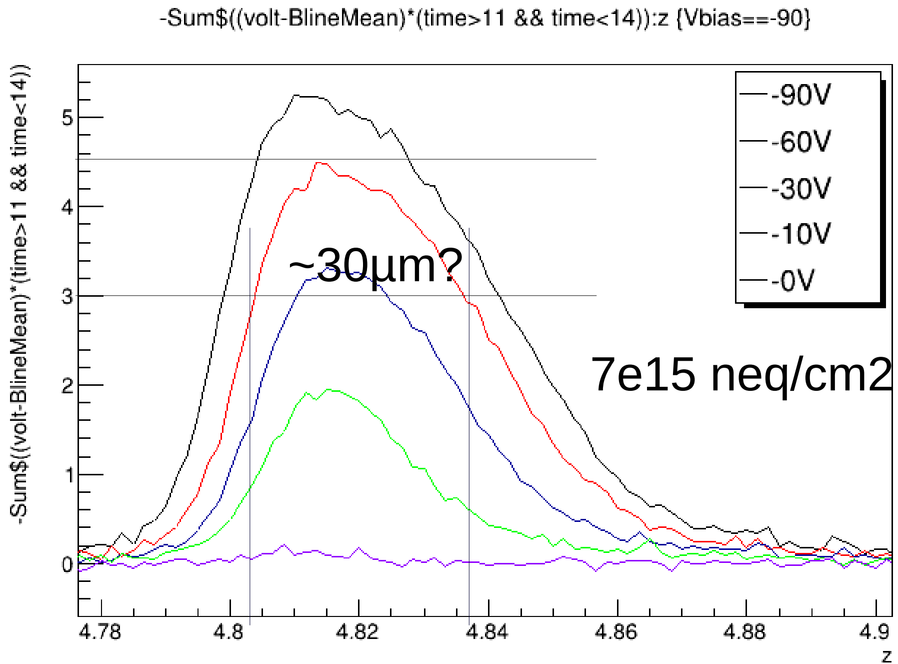


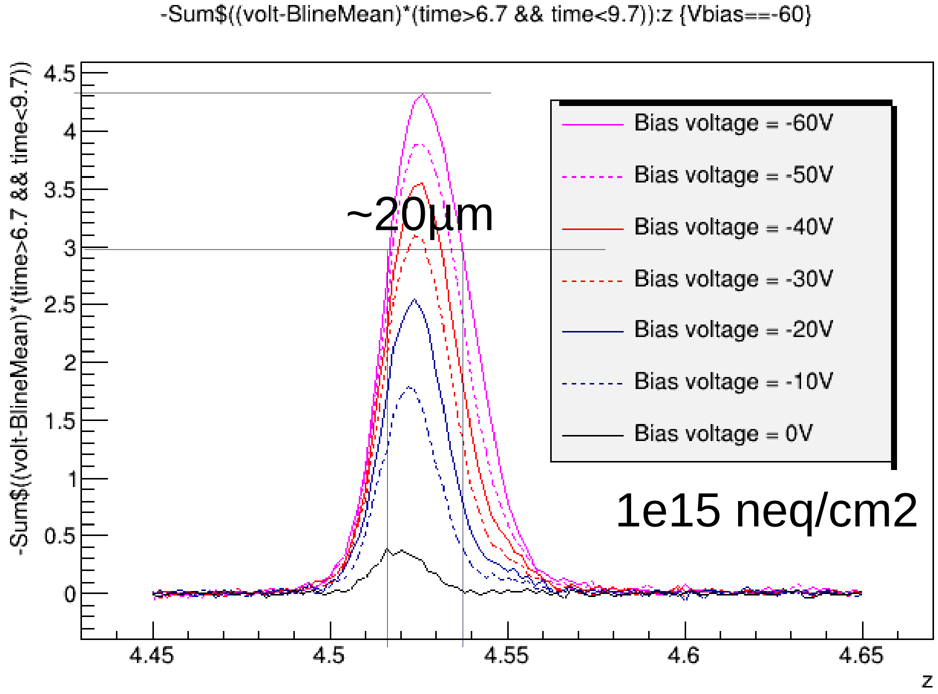


v3 – comparison of regions of fast charge collection

- Measurements still ongoing, **very preliminary**
  - maximum collected charge stays similar to 1e15 sample
    - ~expected: short drift distance, Neff change still insignificant
  - width of charge collection zone larger?
    - also non-symmetric → trapping? E-Field at 7e15?
    - TCAD simulations starting

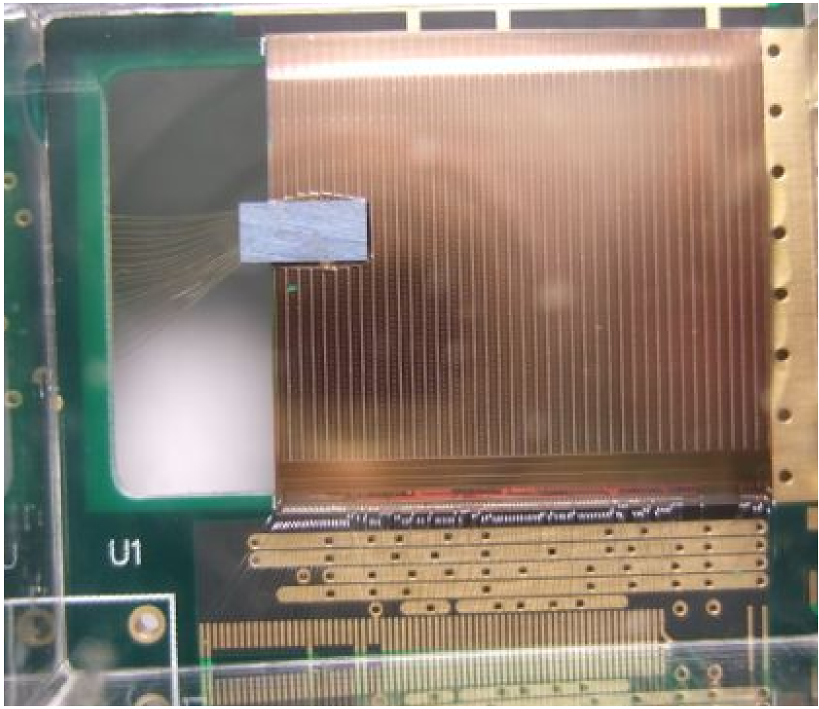


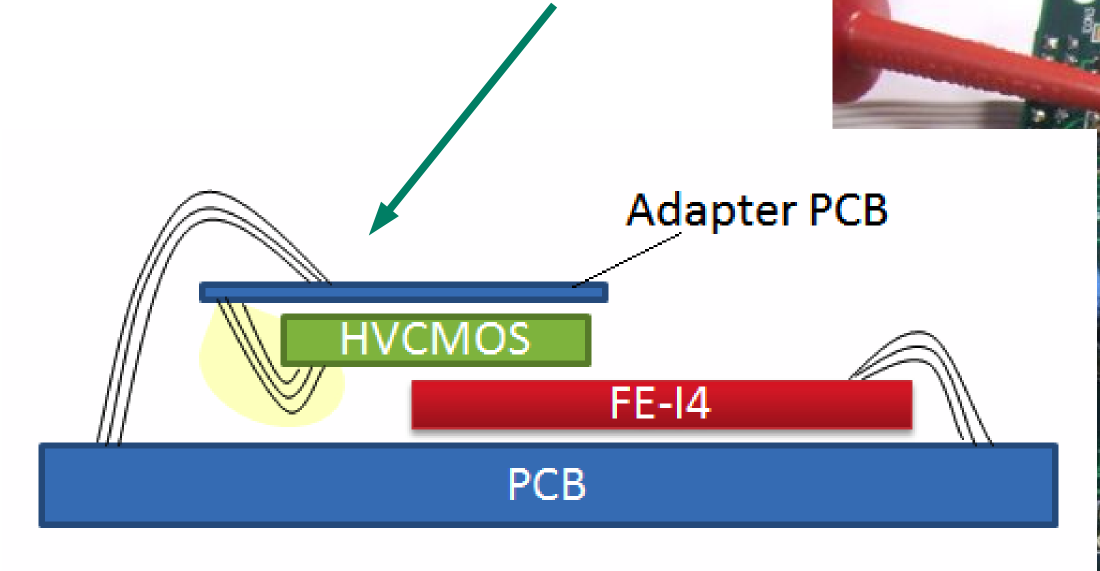




HV2FEI4: Pixel readout

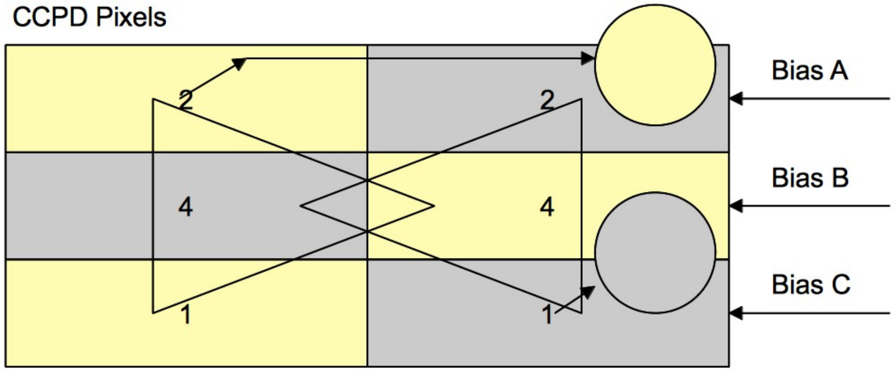
- Several (>20) HV2FEI4s glued to FE-I4 pixel readout chips
  - using pick+place machines, precision requirement estimated to <5 µm for current bump-pads
- HV2FEI4 wirebonds done through hole in PCB
  - could be bumps or TSVs later
  - unidirectional glues under study
  - adapter PCB in production allowing for single-sided wirebonding afte

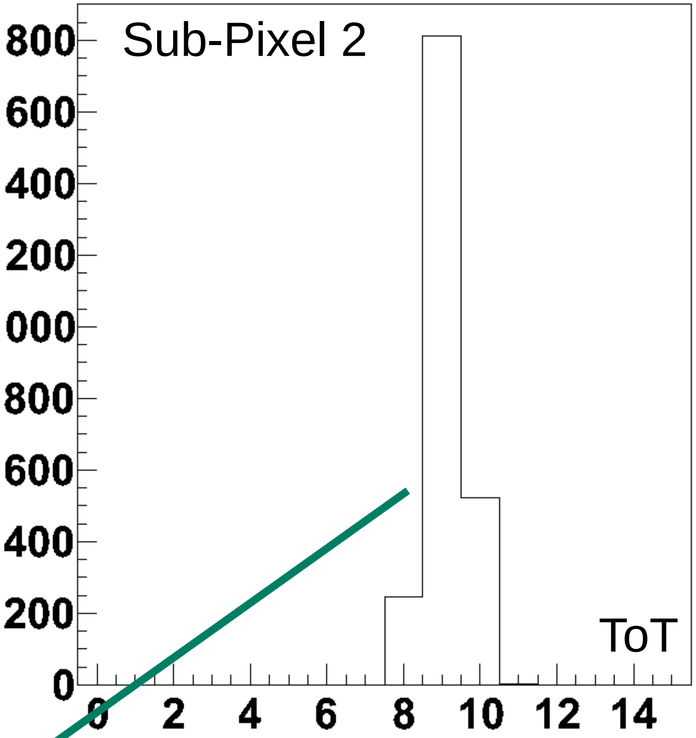


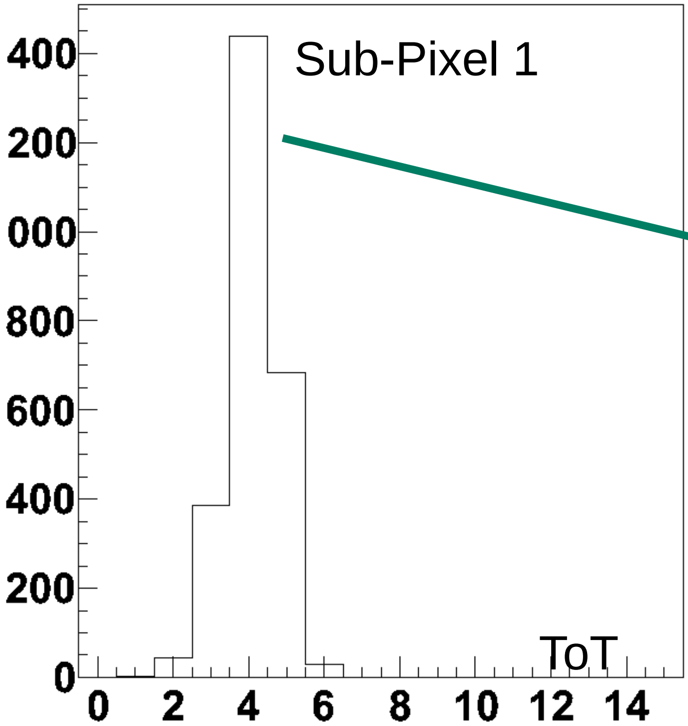


HV2FEI4: Pixel readout

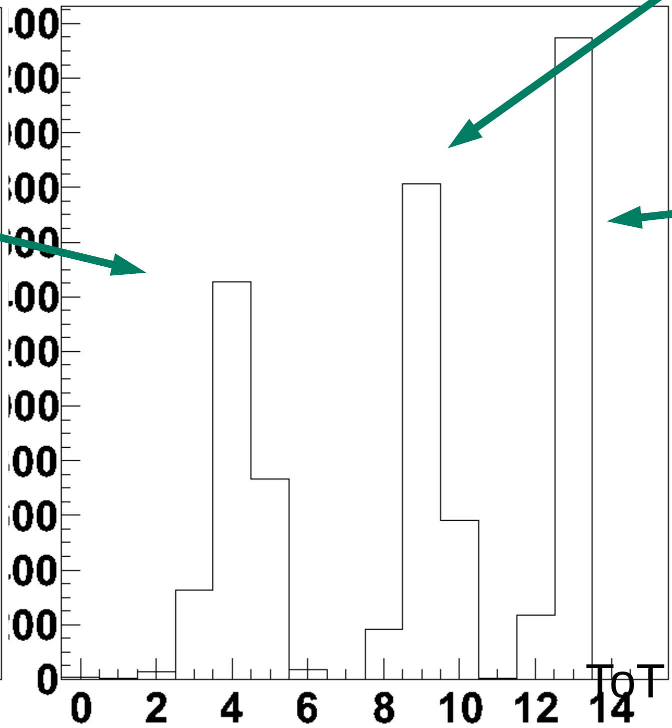
- ToT encoding:
    - 3 sub-pixels clearly distinguishable
      → sub-pixel encoding works!
    - to do: dynamic range matching, array tuning

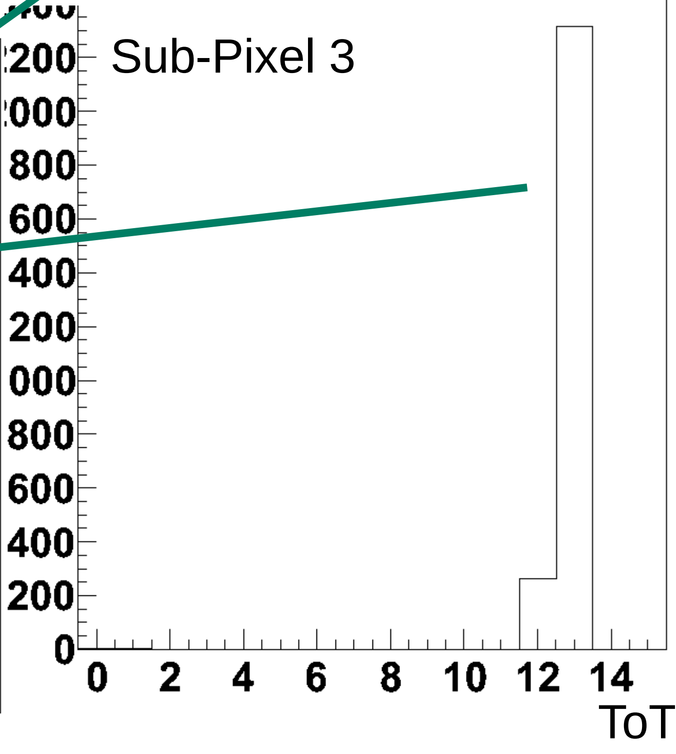






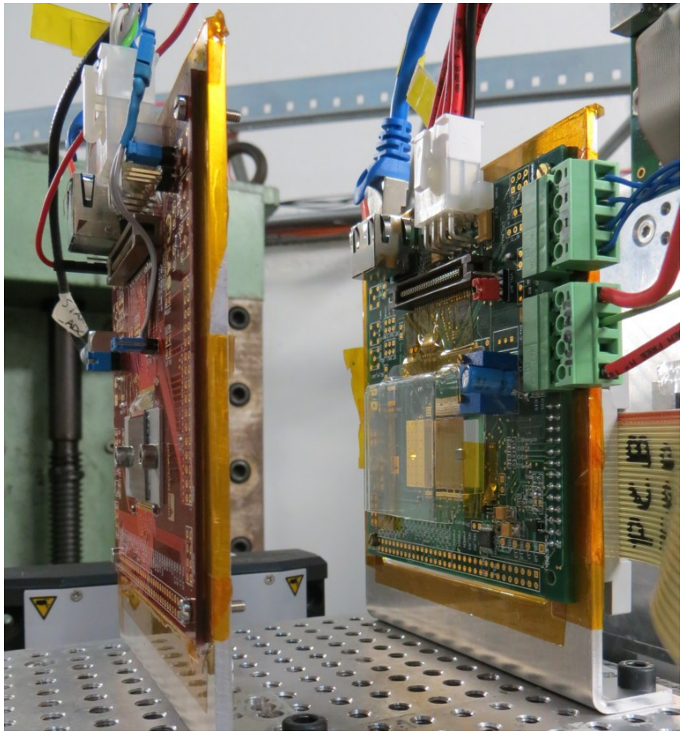
All on

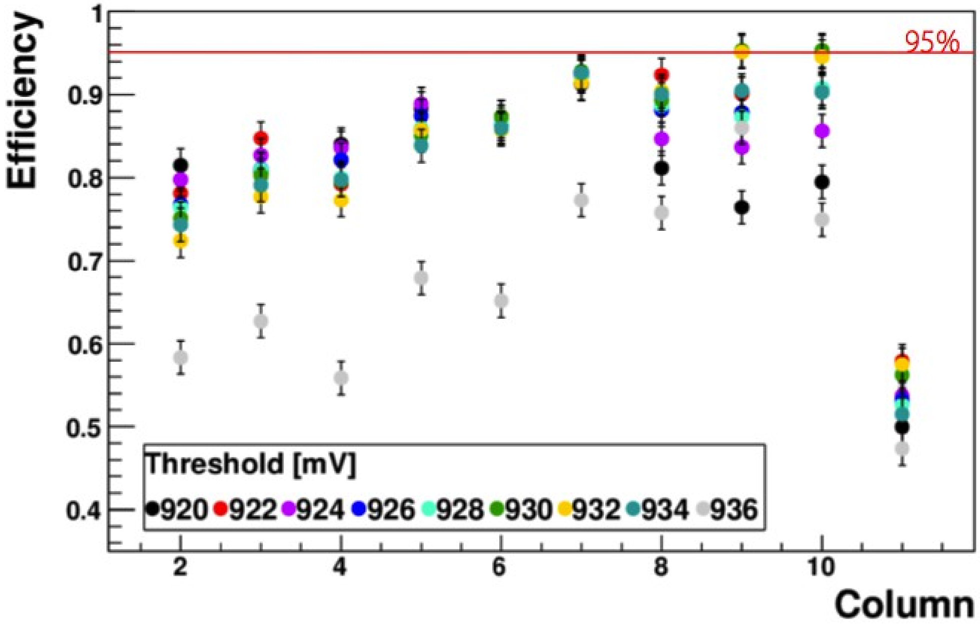


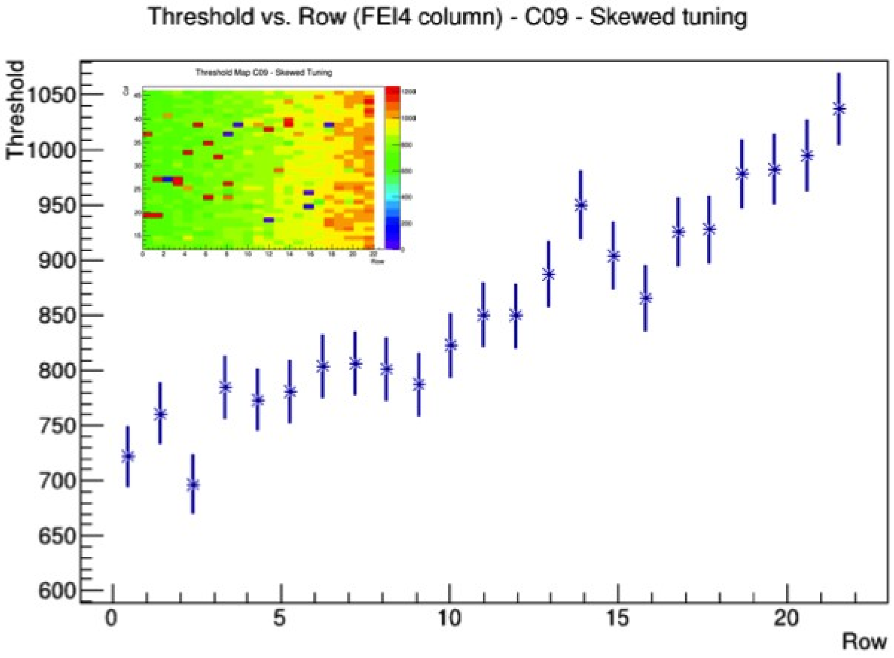


HV2FEI4: Pixel readout in testbeam

- First data taken at 2013 DESY testbeams
  - unirradiated and reactor neutron (JSI) irradiated devices: 1e15 neq/cm2
  - complex geometry complicates alignment
  - non-optimal tunings lead to less efficiency
    - tuning procedures quite fresh at time of testbeam
    - unintentional “skewed” tuning: ~700-1000 e-
    - resulting efficiency unirradiated: ~95-80%



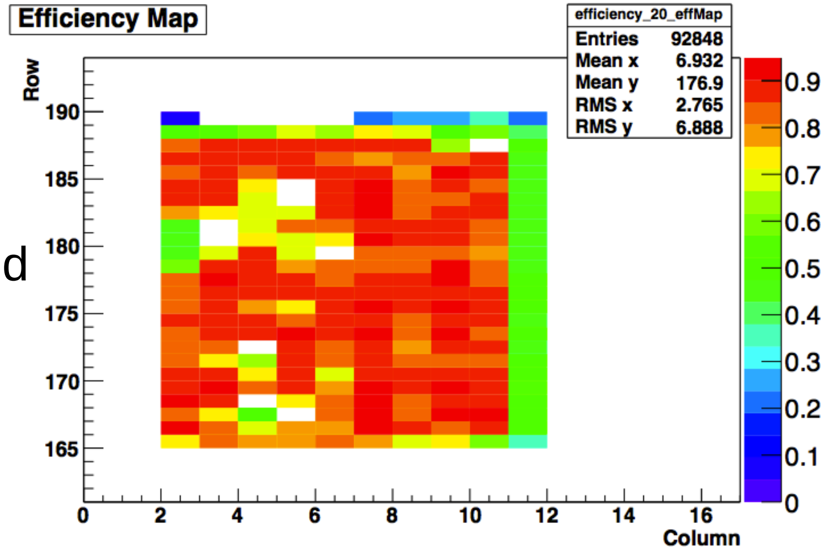


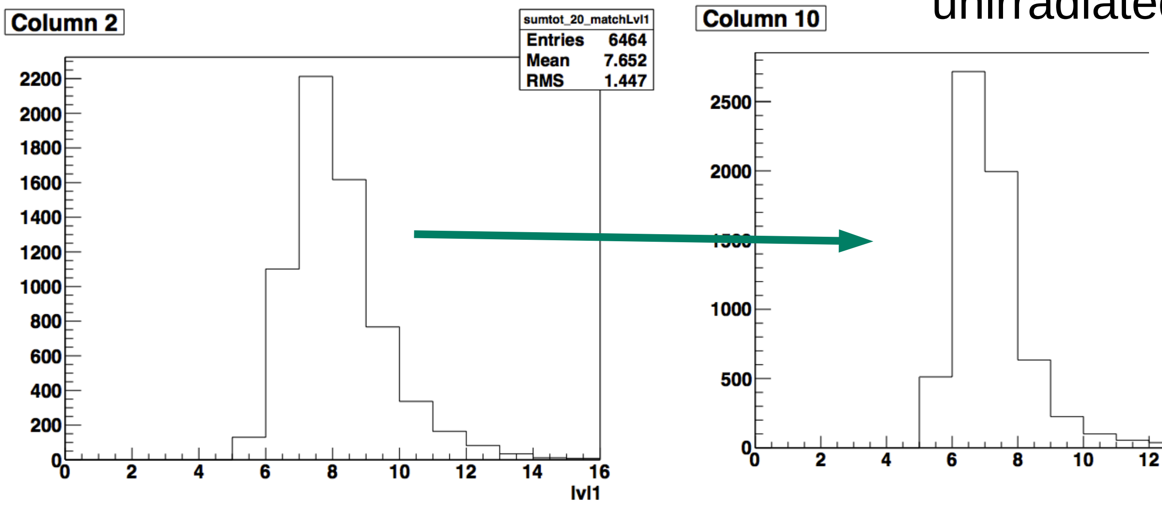

Threshold vs. Row (FEI4 column) - C09 - Skewed tuning

HV2FEI4: Pixel readout in testbeam

- First data taken at 2013 DESY testbeams
  - time-walk depending on threshold – low threshold → better timing

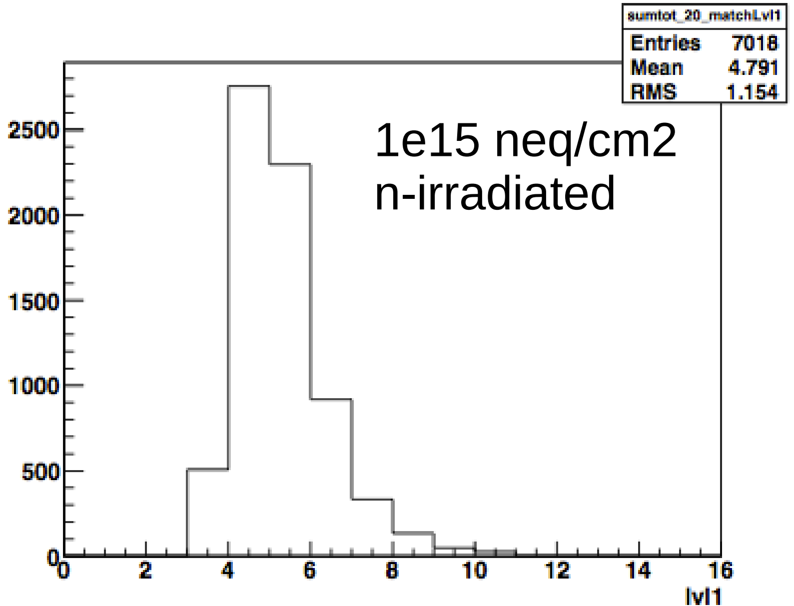
unirradiated





- irradiated sample shows strong HV-dependence of efficiency, timing similar

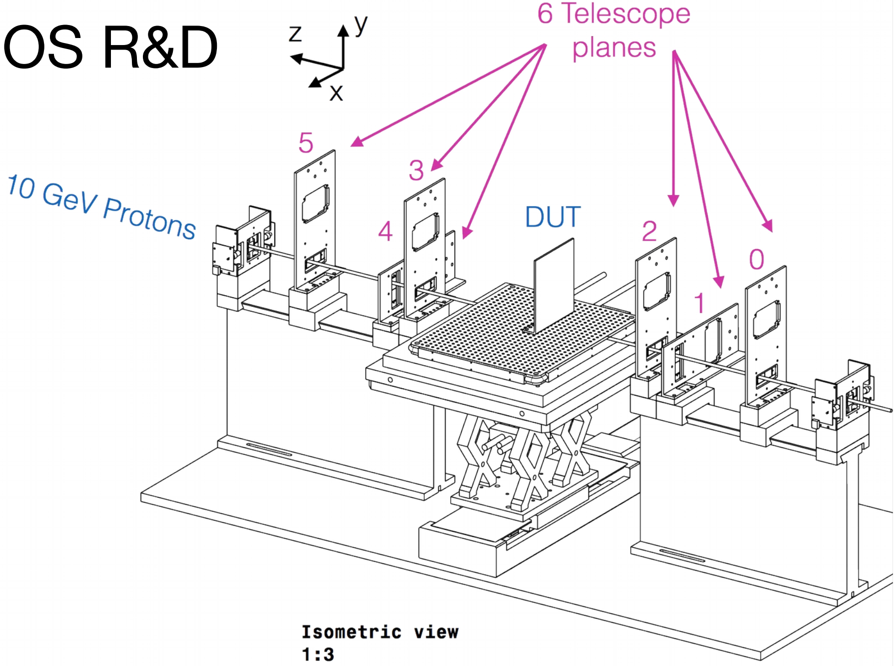
Runs	HV [V]	Trigger	Tracks	Eff
230-232	-57.6	566k	6011	62.9%
224-225	-48.0	517k	10993	54.8%
233-235	-38.4	551k	9783	64.0%
236-238	-28.8	543k	437	51.7%
239-241	-19.2	543k	2590	38.2%
242-244	-9.6	587k	6804	28.2%
245-247	0.0	553k	8969	12.5%



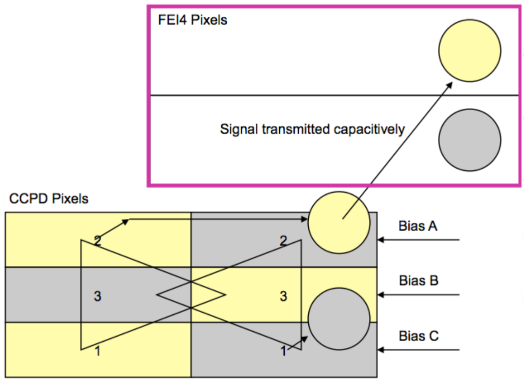
1e15 neq/cm2 n-irradiated

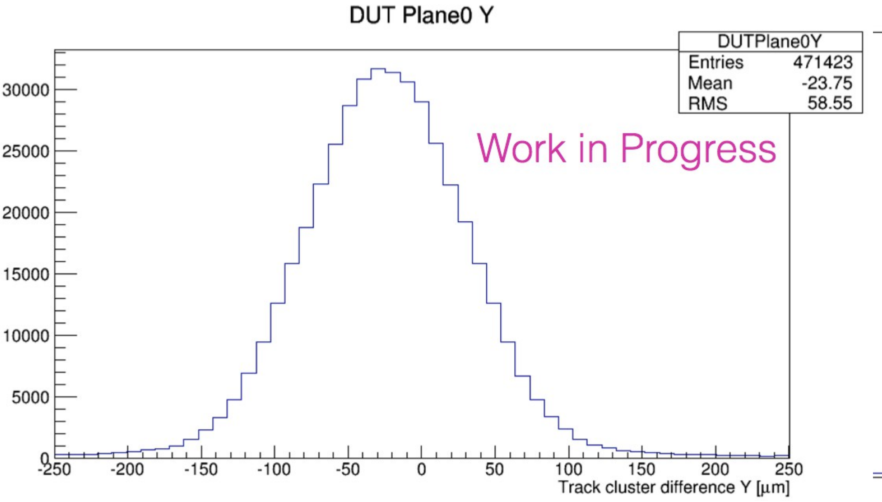
New tuning implemented, new telescope 2014

- Due to some issues with desynchronisation and the very small DUT area, a new FE-I4-based telescope was built and commissionedat CERN PS with special focus on HV-CMOS R&D
- Low energy beam (10 GeV) in combination with large DUT distance (~25 cm) lead to rather large residuals/pointing uncertainty
  - will hopefully run at SPS soon
- No sub-pixel encoding this time, merged pixels to avoid ambiguities



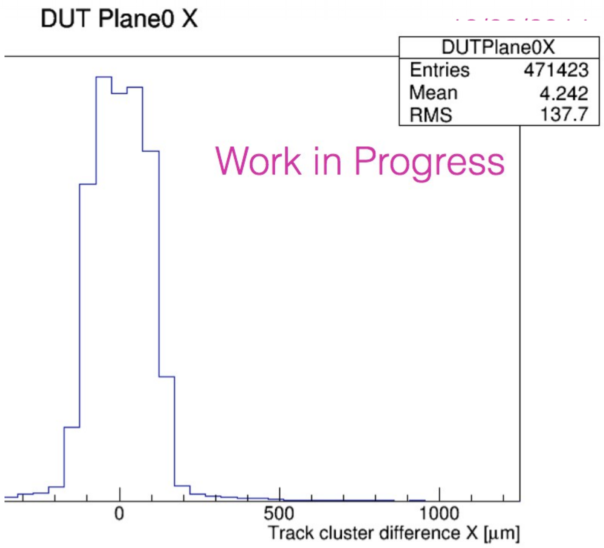
Pixels of 100 x 250 Unit cell




DUT Plane0 Y

DUTPlane0Y	
Entries	471423
Mean	-23.75
RMS	58.55

Work in Progress

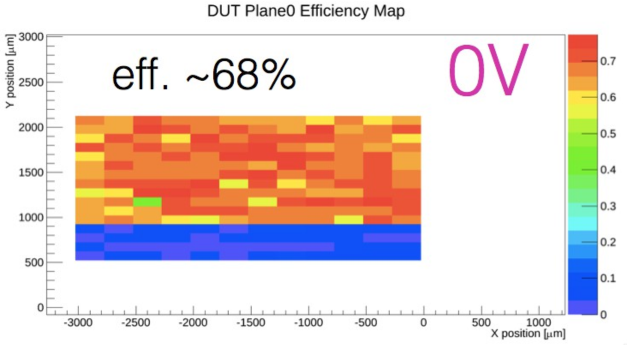

DUT Plane0 X

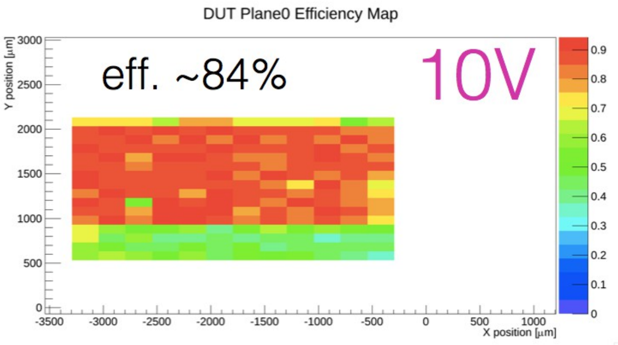
DUTPlane0X	
Entries	471423
Mean	4.242
RMS	137.7

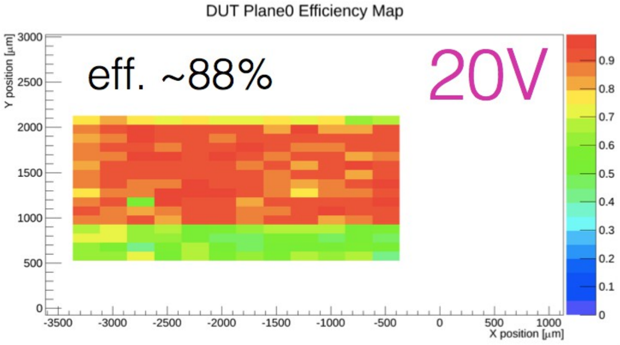
Work in Progress

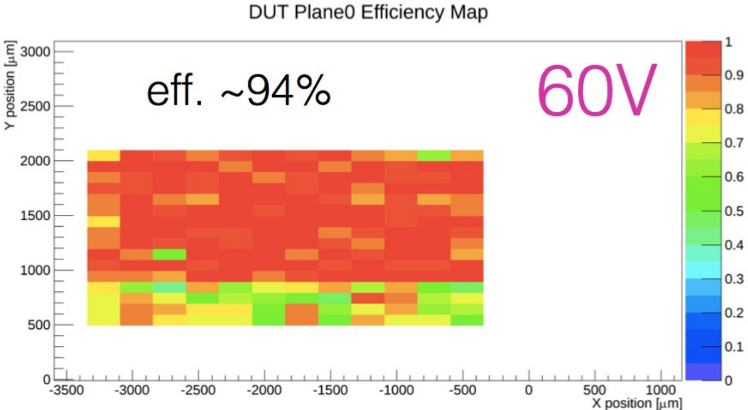
New tuning implemented, new telescope 2014

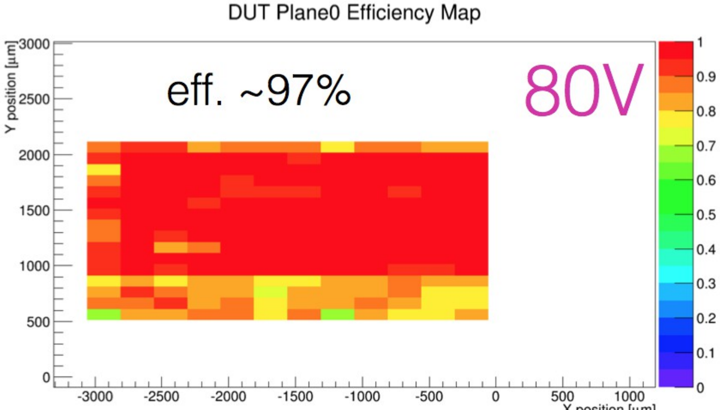
- New noise tuning was implemented aiming to tune every pixel as low as noise occupancy allows
  - works in principle, matrix effects still to be studied
- With unirradiated sample sees clear effect of bias voltage on efficiency
  - low efficiency region at bottom are “rad-hard” pixels with higher threshold setting → understood
  - need to understand where/if ~3% efficiency are lost: multiple scattering, interpixel field gaps, ...


DUT Plane0 Efficiency Map

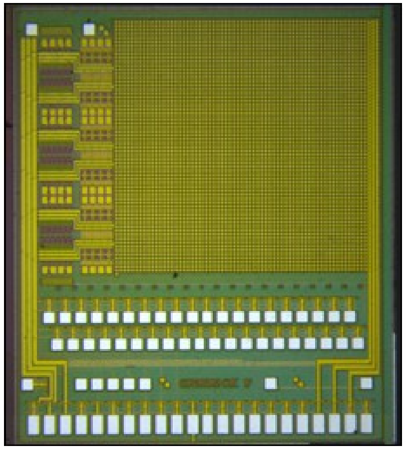

DUT Plane0 Efficiency Map


DUT Plane0 Efficiency Map

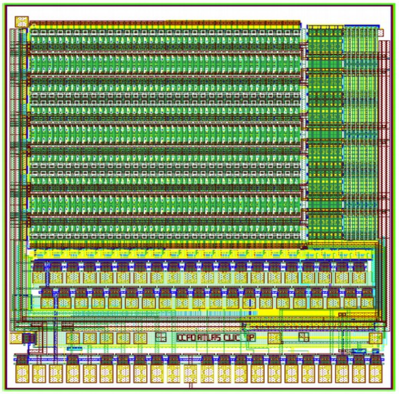

DUT Plane0 Efficiency Map


DUT Plane0 Efficiency Map

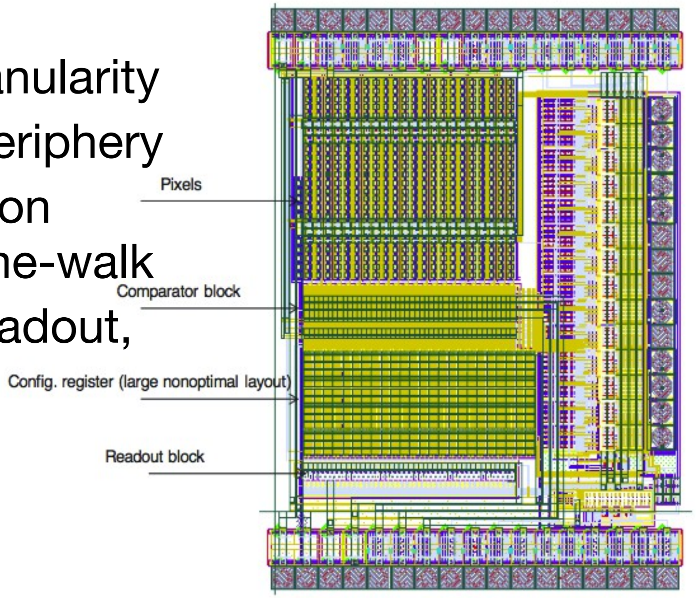
Further prototypes



- H18_v3
  - shared with CLIC, contains Amplifier-only 25x25µm pixels and some ATLAS test pixels
  - first measurements indicate good noise behaviour in particular of CLIC-pixels
  - dedicated passive eTCT-diode and test structures, measurements being prepared



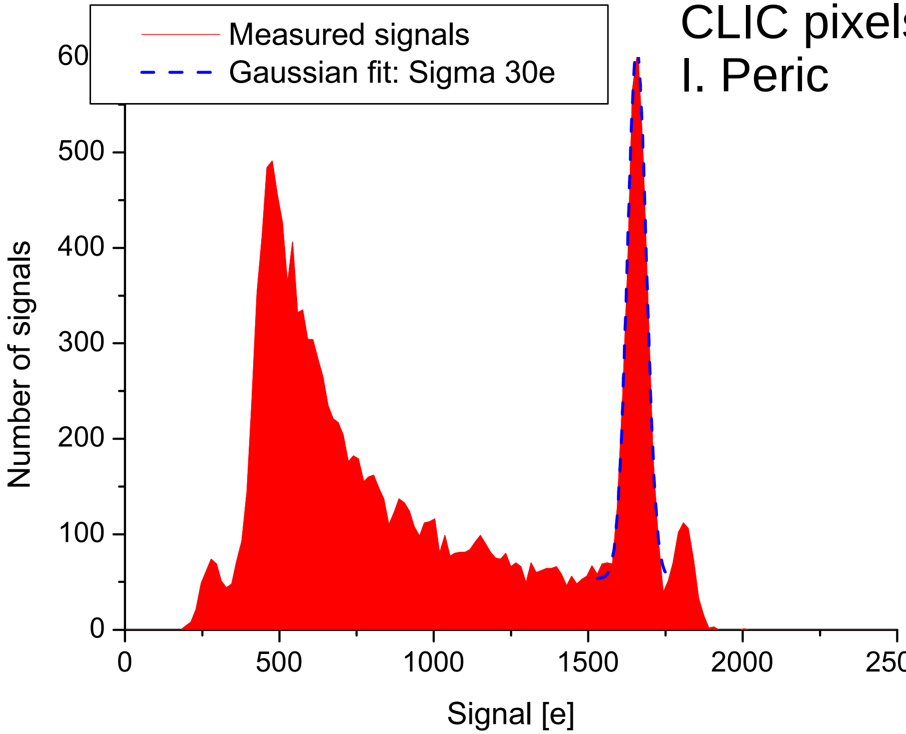
- H18_v4
  - focused on ATLAS-pixel readout, several noise improvements, segmented pixels, analogue pixels (25x250µm), pulse-width encoding of sub-pixel address promising better ToT encoding



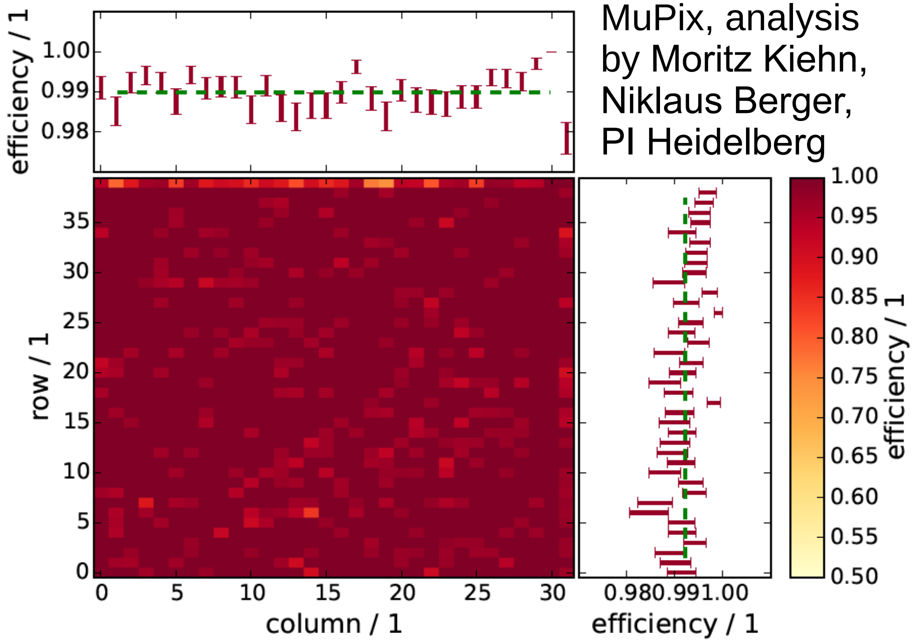
- H35_v1
  - intended for strip region: lower fluence, larger granularity
  - analogue 40 x 400 µm pixels with traces to the periphery
  - discriminator block contains also “constant fraction discriminator”-like circuits aiming for improved time-walk
  - digital encoding, followed by 320 MBit/s LVDS readout, two concurrent hits can be read out
  - several test structures for rad-hardness testing

A glimpse beyond ATLAS

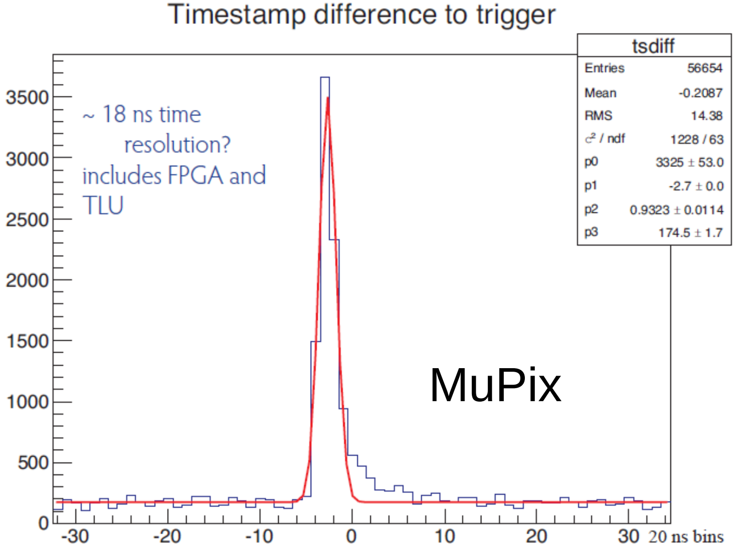
- H18_v3: CLIC usage with 25x25 µm purely analogue pixels
    - no digital activity in pixels, good noise behaviour
    - has been implemented in H18_v4 for ATLAS-size pixels as well
- mu3e experiment at PSI: MuPix chip
    - monolithic, only analogue pixel cell amplifier
    - ~99% efficiency measured in test beam, also timing looked good



CLIC pixels, I. Peric

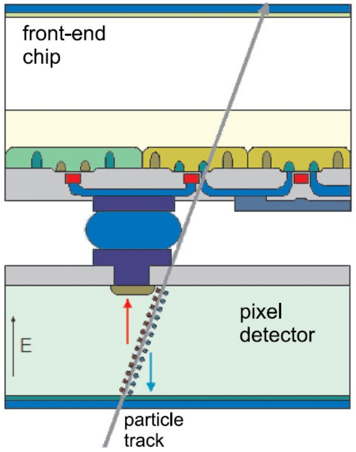


MuPix, analysis by Moritz Kiehn, Niklaus Berger, PI Heidelberg

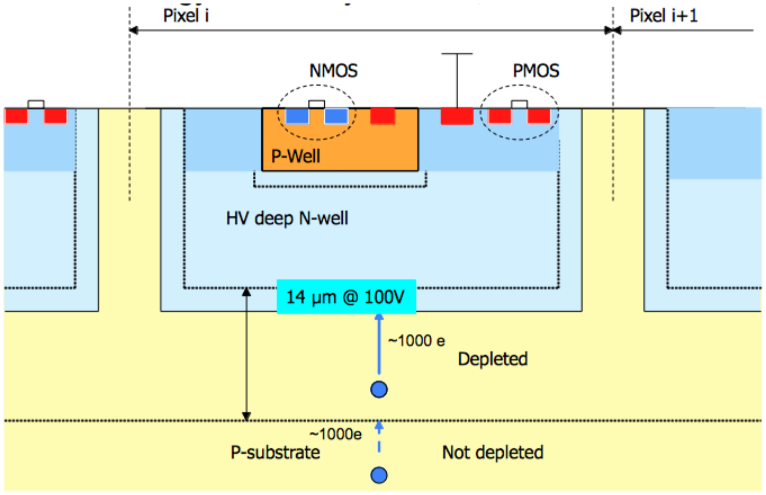


HR-CMOS

- Main requirement for drift-based CMOS sensor is a deep n-well
  - also present in CIS (CMOS Image Sensor) processes with high-resistive substrate or epi layer → larger depletion depth
    - certainly larger initial signal, reduction of depletion depth to be studied
    - charge sharing possible again allowing to higher resolution at low fluences
- Several CMOS imaging processes available from different foundries
  - back-side illumination requires full depletion and thin sensors
  - high-resistivity FZ base material available in an industrialised process
- HV-CMOS appears to be "on the edge" wrt to Signal/Threshold
  - increase signal by more depletion? How much? Equally radiation-hard?
  - 2 directions: "moderate" (100 Ohm*cm) vs. "high" (kOhm*cm) resistivity

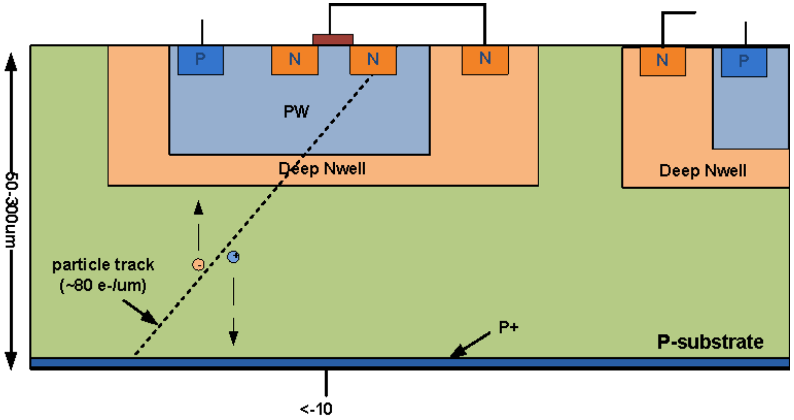


Hybrid



CMOS electronics placed inside the diode (inside the n-well)

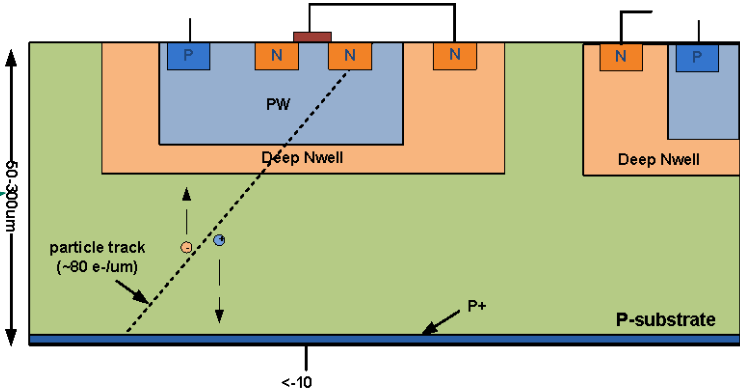
HV-CMOS

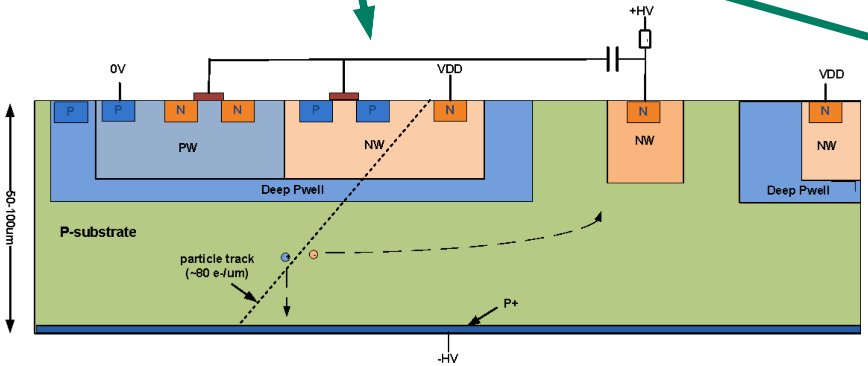


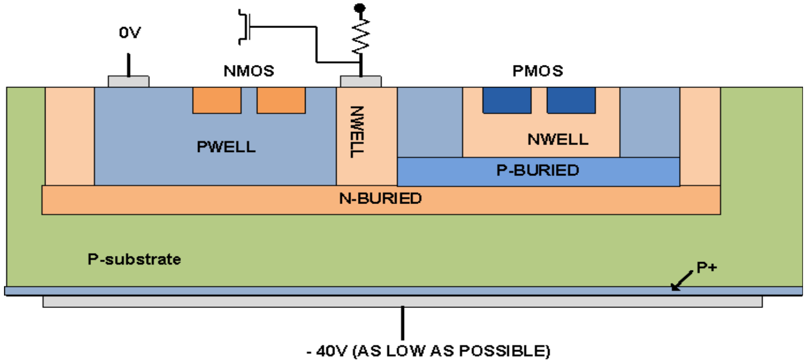
HR-CMOS

HR-CMOS

- Many different designs possible:
    - HV-CMOS like (deep n-well, no triple-well)
    - triple-well
    - Alice-like



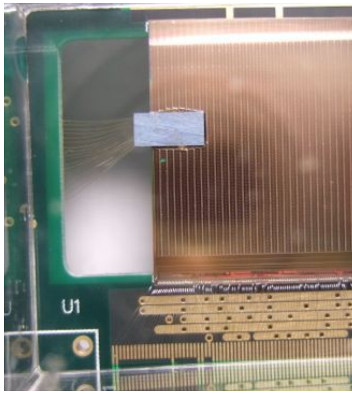


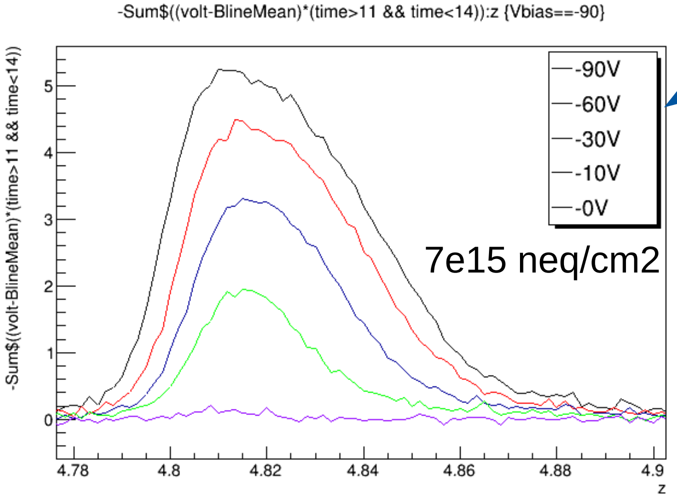


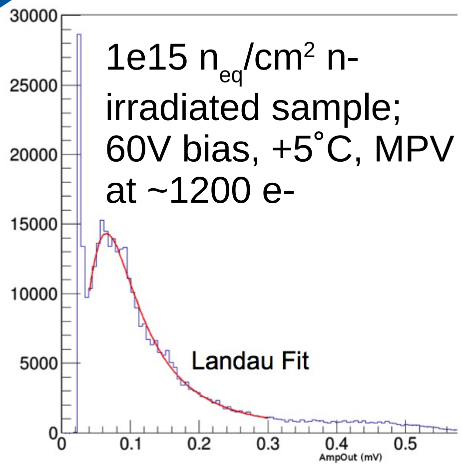
- First prototypes have been produced within ATLAS
    - characterisation, irradiations ongoing
    - no time to go into detail
- “Moderate” resistivity submissions of “HV-CMOS” designs planned for early 2015
    - expect signal incrase of a factor 2-5 while still

Conclusions

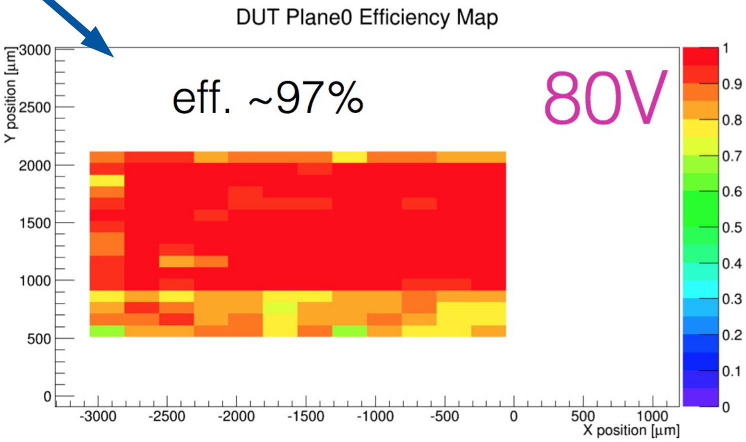
- HV/HR-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage, low-mass sensors
- Process can be used for
  - 'active' n-in-p sensors (with capacitive coupling)
  - drift-based close-to-MAPS chips (digitally encoded strips)
- First prototypes being explored within ATLAS
  - Irradiated samples show radiation hardness
  - results with capacitively coupled HV-CMOS pixel sensors look promising







1e15 n_{eq}/cm² n-irradiated sample; 60V bias, +5˚C, MPV at ~1200 e-



eff. ~97%

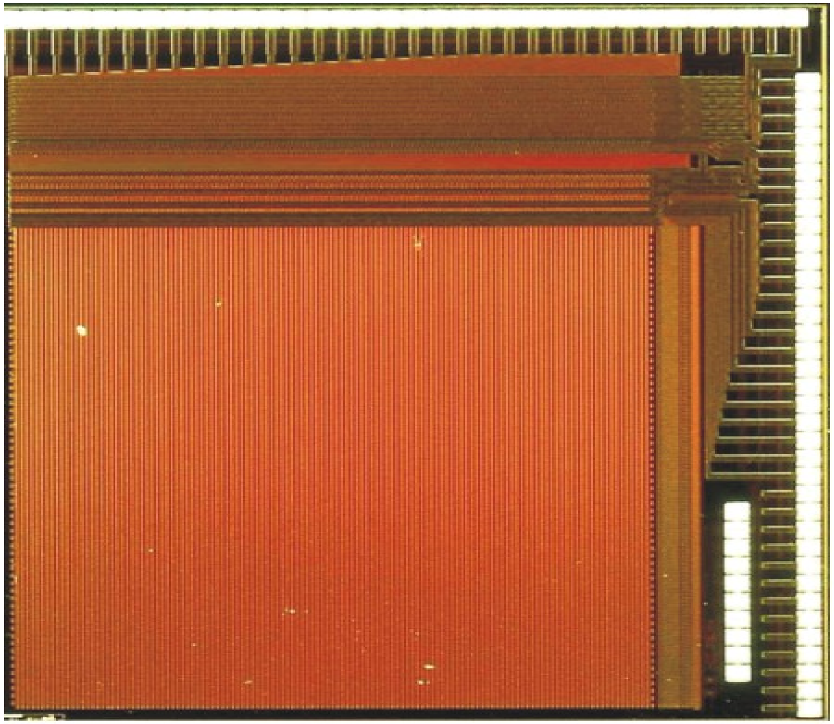
80V

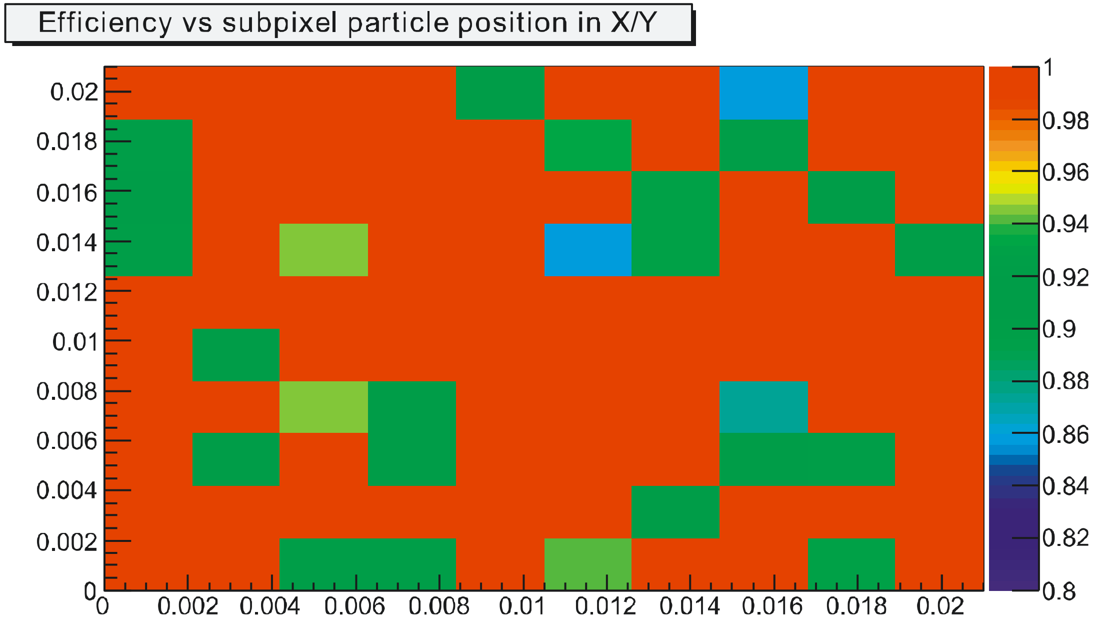
- Next step: Explore higher resistive substrates to increase signal
  - engineering run with large-scale sensor planned for early 2015
- (ATLAS) goal: Have “demonstrators” in hand by the end of 2015

Backup slides

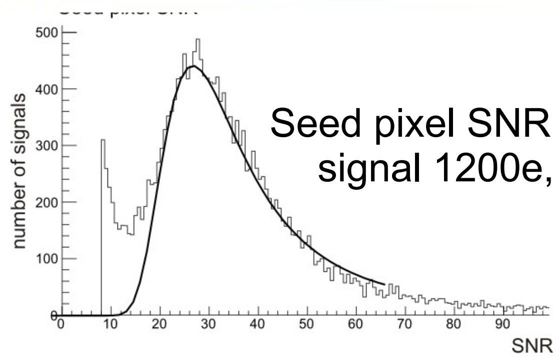
Test beam results: monolithic

- excellent resolution
- very good S/N ratio
- efficiency limited by readout artifacts:
  - column-based readout
  - row not active during readout
  - data analysis did not correct for this
  - very small chip → low statistics

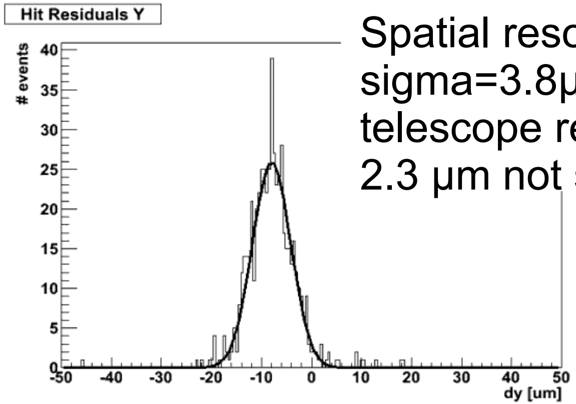




Efficiency vs. the in-pixel position of the fitted hit. Efficiency at TB: ~98% (probably due to a rolling shutter effect)



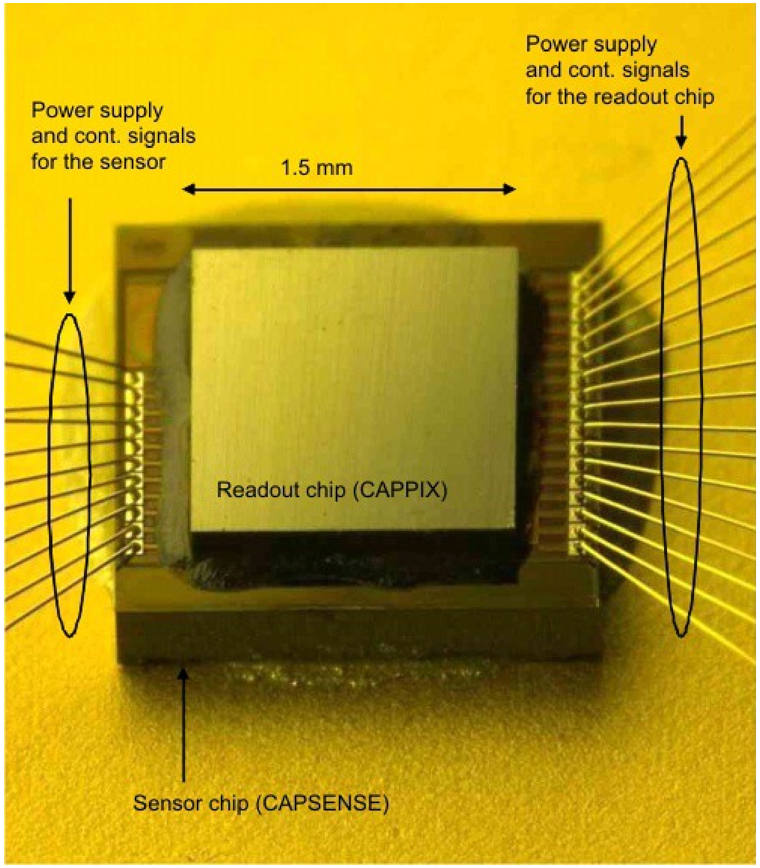
Seed pixel SNR 27, seed signal 1200e, cluster 2000e



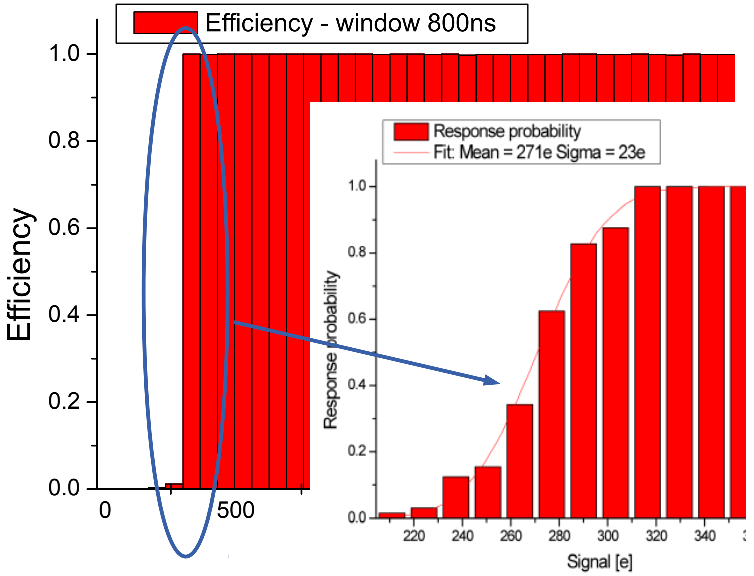
Spatial resolution: sigma=3.8µm, telescope resolution of 2.3 µm not subtracted

CPPD prototype results

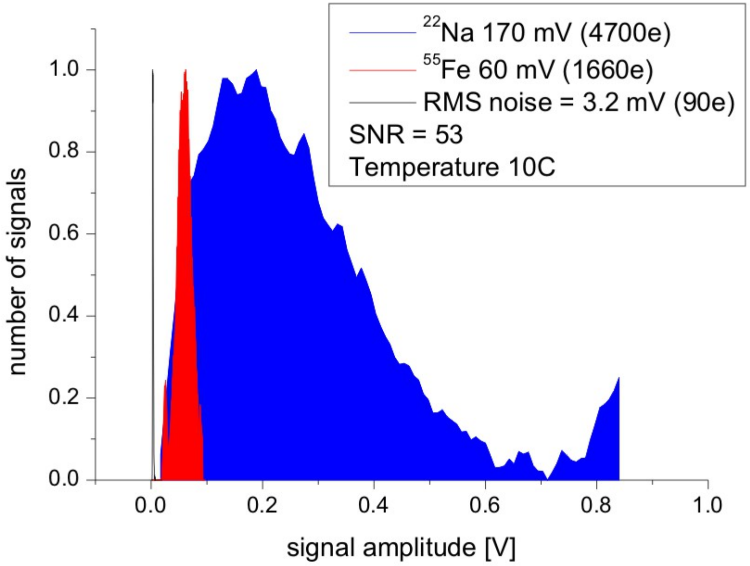
- excellent noise behaviour: stable threshold at ~330 electrons
- good performance also after irradiation



CAPPIX/CAPSENSE edgeless CCPD
50x50 μm pixel size



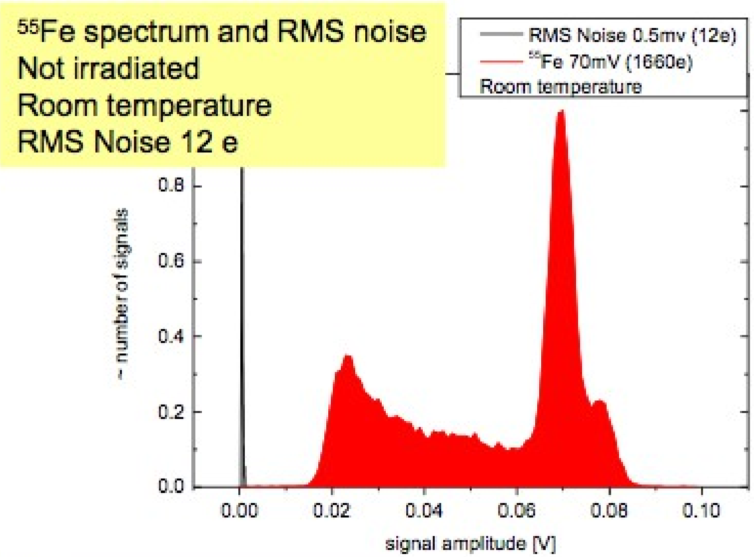
Detection efficiency vs. amplitude
Detection of signals above 330e possible with >99% efficiency.

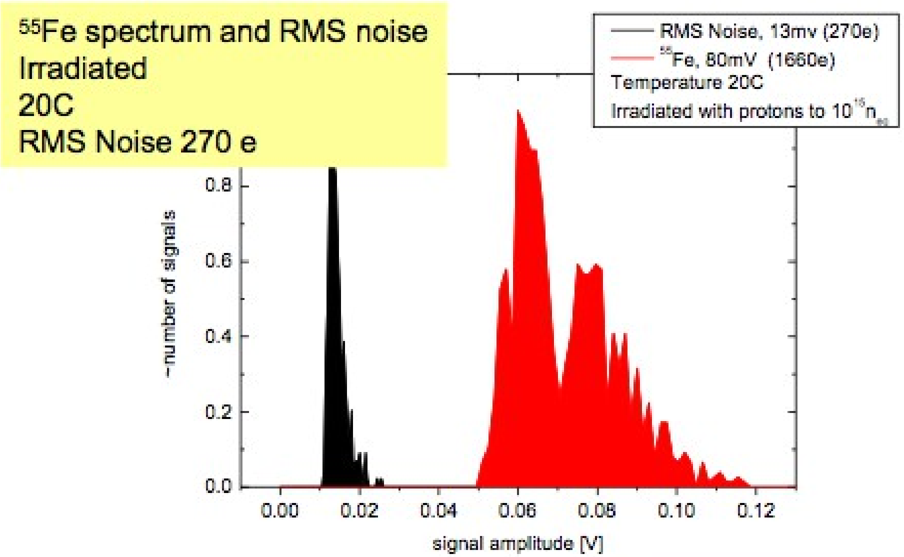


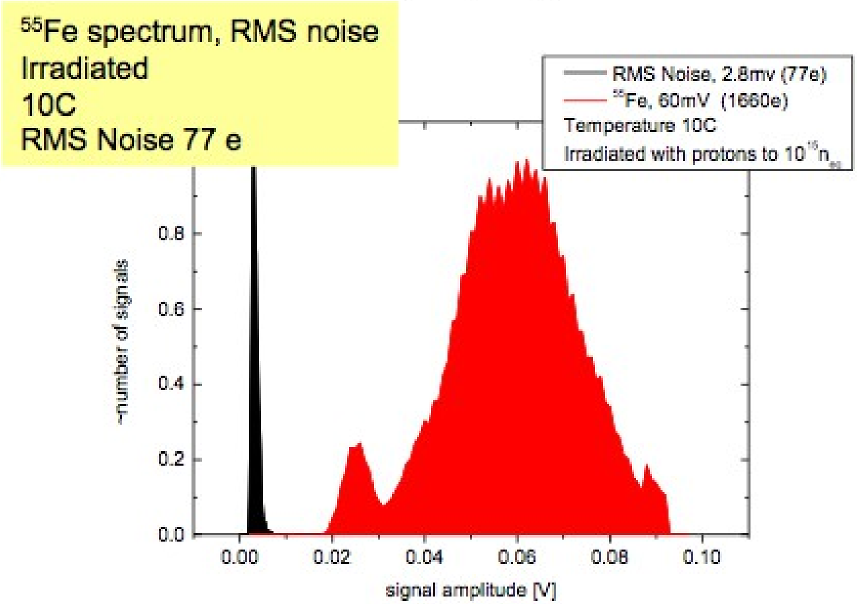
Signals and noise of a CAPSENSE pixel after $10^{15} n_{eq}/cm^2$

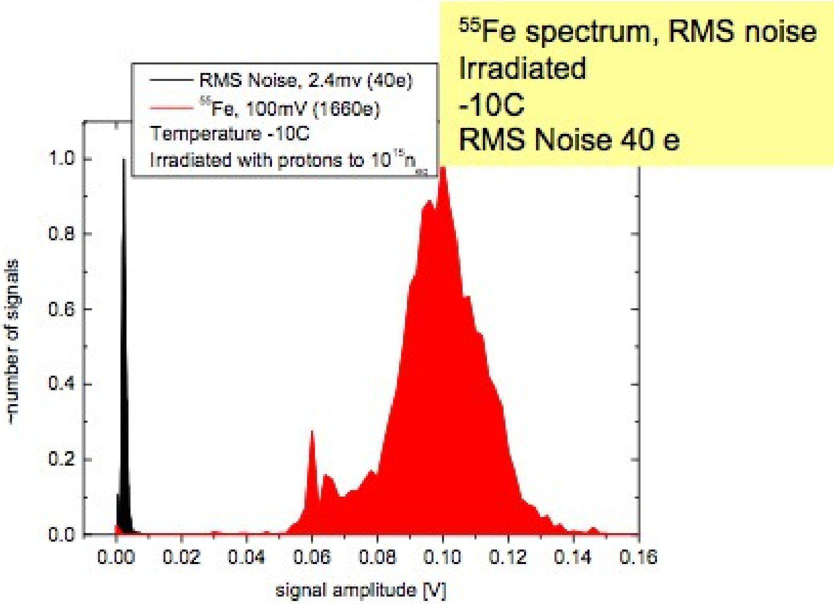
CPPD prototype results

- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling


^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e


^{55}Fe spectrum and RMS noise
Irradiated
20C
RMS Noise 270 e


^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e


^{55}Fe spectrum, RMS noise
Irradiated
-10C
RMS Noise 40 e