MTCA.4 at DESY.

Uroš Mavrič on behalf of the DESY MTCA.4 Development.

8th meeting of the xTCA interest group, CERN, 17.03.2014

HELMHOLTZ ASSOCIATION

DESY

Talk Overview.

- Hardware overview
- Organization of the FPGA functionalities
- Driver and software organization
- Management and interoperability
- Applications

COTS HW Components.

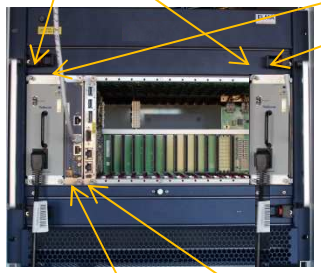
Typical MTCA.4 crate configuration used at DESY.

NAT, 600 W

Telkoor, 1kW, 600 W

Wiener, 1kW

2U Schroff



9U 12 slot ELMA

- LLRF AMC backplane
- PCIe gen. 3 (8 Gbps)
- PtP: <6 Gbps (to-be redesigned)

9U 12 slot Schroff

- LLRF AMC backplane
- PCIe gen. 3 (8 Gbps)
- PtP: 10 Gbps

NAT MCH-PHYS

- Host of the MCMC.
- Host of the PCIe switch : PCIe x4 Gen 3 for each slot.
- Centralized CLK distribution to all AMCs.
- Transition to rear over Z3 (COM Express, management module for the RF backplane).

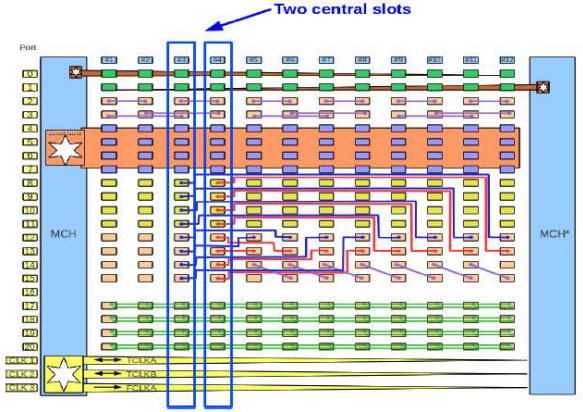
Concurrent AM 900/412

- 2-core 2.5 GHz Intel Core i7-3555LE processor
- 16 Gbytes of DDR3-1600
- X 8 PCIe Gen 3
- 2 x SATA interfaces for onboard storage
- 4 x Gigabit Ethernet interfaces
- 2 x USB 3.0 ports via front panel
- 3 serial port interfaces
- Display Port graphics interface via front panel
- Serial-over-LAN (SOL)
- Possibility to switch to a quad-core

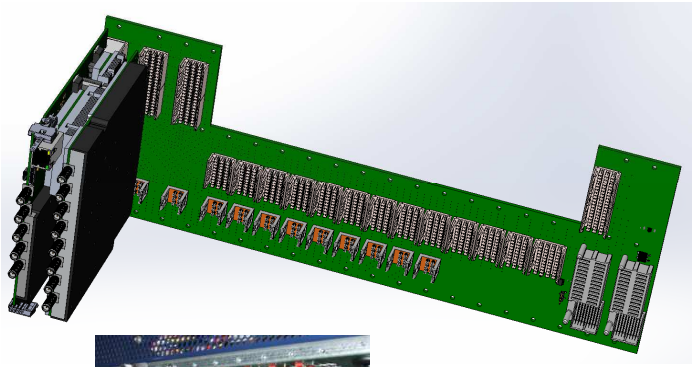
Specific DESY/XFEL HW Demands.

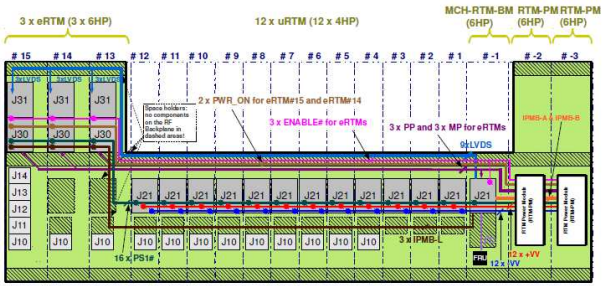
- Vector sum systems require centralized slots with AMC cards that act as concentrators.
  - Modification of the standard PICMG AMC backplane.
  - LLL on ports 8-15 on slot 3,4 to all other slots.
  - Data throughput : 6.25 Gbps by 6 on Point-to-Point.

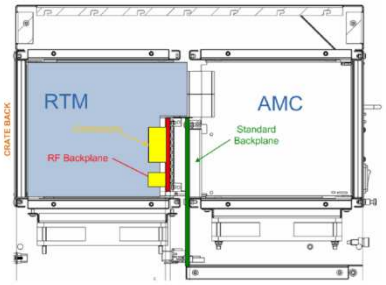
LLRF AMC BKCPL.



- Multichannel systems and limited space require compact signal distribution.
  - uRF Backplane located in the rear side of the standard MTCA.4 crate.
  - For the MCH, the uRF backplane is an extension of the front backplane.



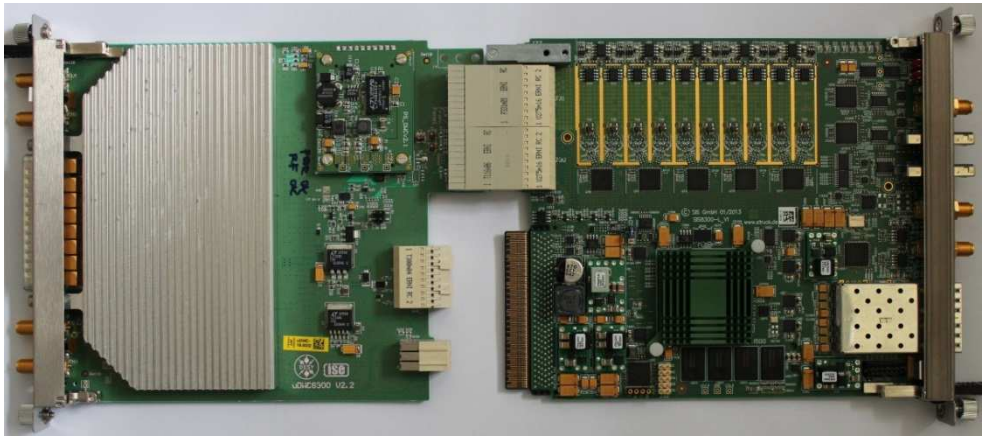




Typical AMC/RTM Pairs.

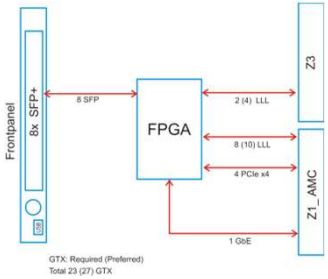
DRTM-DWC10 / SIS8300L

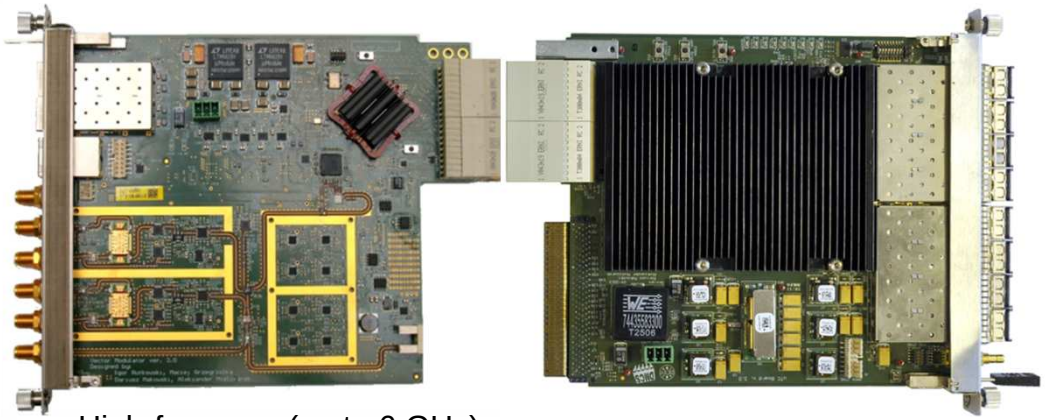
- 10 channel down-converter to IF (<80 MHz).
- RF input 0.7 - 4 GHz
- Variable attenuators
- Low residual phase and amplitude noise.
- 10 channels with 16 bit, 125 MSPS ADCs
- Virtex 6, 4 x 4 Gbit DDR3



DRTM-VM2 / DAMC-TCK7

- 2 I/Q modulators with RF switch driven by interlocks.
- Spartan 6, 16- bit DACs
- On-board CLK generation.
- Data concentrator based on Kintex 7, 23 (27) GTXs.
- LLL up to 12.5 Gbps.
- PCIe Gen. 3 (16Gb/s/4 lanes)





High-freq. ver. (up to 6 GHz)

Low-freq. ver. (0.1 – 1.5 GHz)

General Purpose AMC Boards.

DAMC-FMC25

- A general purpose FMC Carrier
- Two HPC connectors
- Virtex 5 XC5VFX70T-2FF1136, DSP, application specific tasks, etc.
- Spartan 6 XC6SLX45T-2CSG324I for on-board management

DAMC-FMC20

- A general purpose low-cost FMC Carrier
- One HPC connector and one LPC connector
- Spartan 6 XC6SLX45T (for PCIe conn.) and Spartan 6 XC6SLX150 (for appl. and Z3 conn.)

DAMC-DS800

- Fast digitizer with 8 input channels at 0.8 GSPS or 4 at 1.6 GSPS
- 4 x DACs
- On-board fan-out for CLKs
- Virtex 6

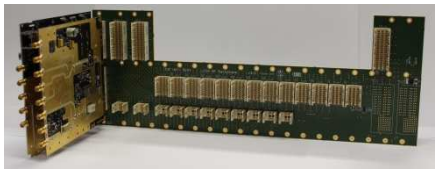
Specific RTM boards.

DRTM-PZT4

- 4 power amplifiers with 0-100V, -100V/+100V
- DAC outputs +/-5V, +/-10V, 0/5V, 0/10V
- Each power amplifier can drive up to 10uF capacitance.
- Remotely variable output analog filter
- Possibility for external power supply

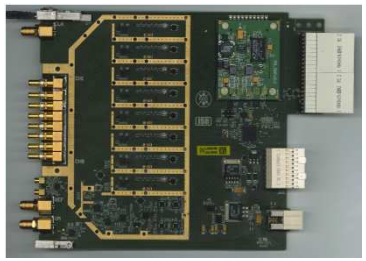
DRTM-LOG1300

- Generation of the LO and CLK signals from single REF input.
- Distribution over uRF backplane.
- Splitting of 3 RF signals to 9 x 3 RF outputs.
- Fan-out of 22 LVPECL CLK signals.
- Each RF and/or CLK channel can be switched off individually
- Temperature control of the circuit via Peltier elements and TECs.



DRTM-DWC8VM1, DRTM-DS8VM1

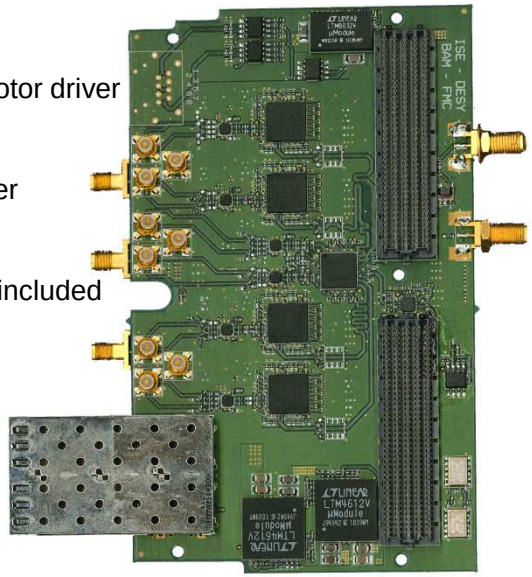
- Field detection and RF drive output on single RTM.
- Low frequency (direct sampling 5 MHz – 450 MHz) and high frequency version (down conversion 0.7 – 6 GHz).
- I/Q modulator with monitoring and RF switch.
- On-board CLK generation via extr. REF or/and on-board VCXO.



More FMC/RTM Cards.

DFMC-MD22

- Dual channel stepper motor driver
- LPC connector
- Includes motion controller
- Monitoring of motor load
- Protection mechanisms included



DFMC-BAM

- Two ch. with interleaved sampling of 2 ADCs.
- On-board CLK distribution and phase shifting

DRTM-AD84

- 8 ADCs 10 MSPS, 4 DACs 1 MSPS
- ADC : DC-95 MHz input BW, switchable ADC input impedance
- DAC : DC-1 MHz output BW, 50 ohm output impedance

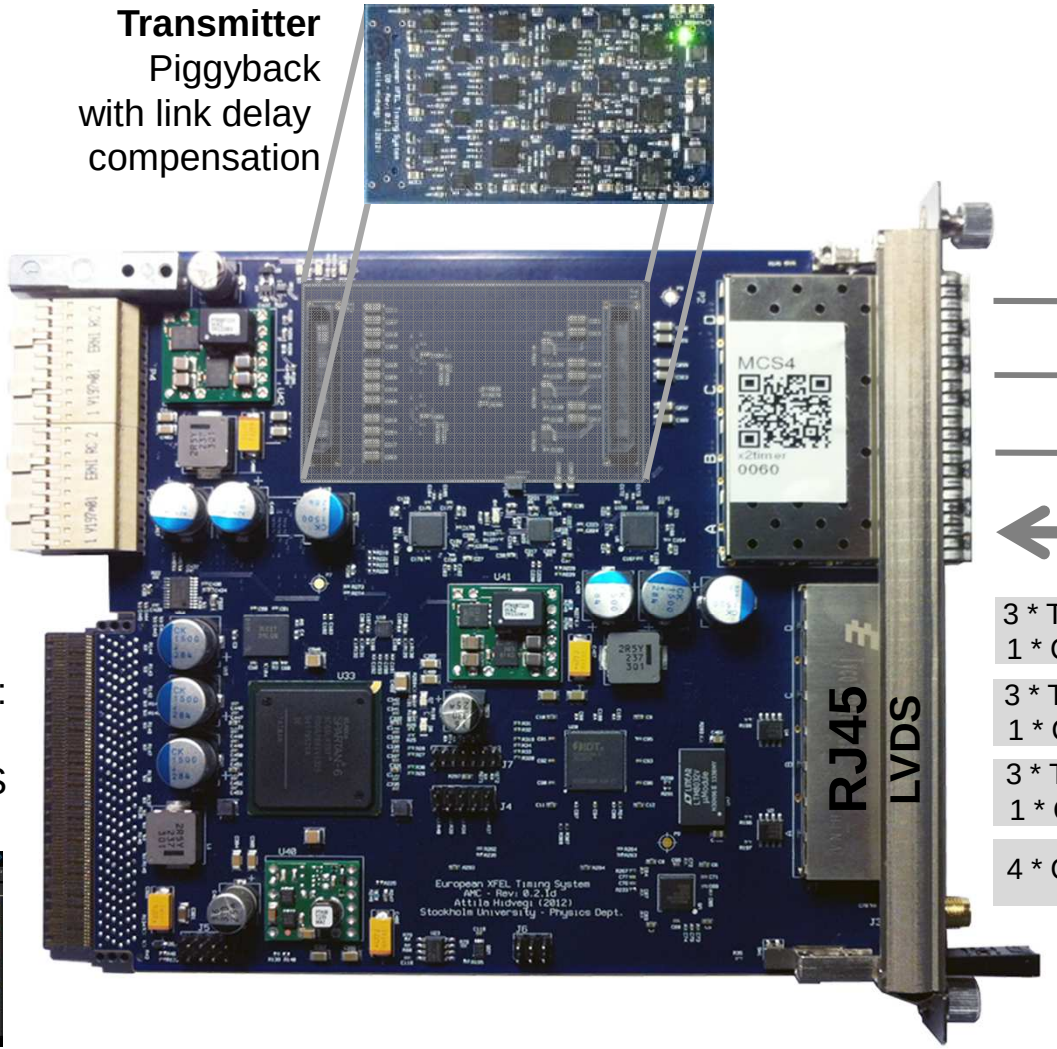
ps Timing System for XFEL and FLASH

Can be used as a timing **receiver** or **transmitter**

Transmitter
Piggyback with link delay compensation

Optional **RTM**:
9 transmitters,
Further triggers or clocks

MicroTCA **backplane**:
TCLKA and TCLKB,
8 * M-LVDS



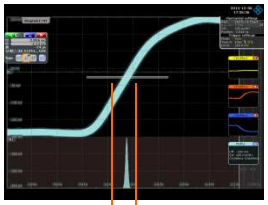
PICMG
MTCA.4

3 * Trigger out
1 * Clock out

3 * Trigger out
1 * Clock out

3 * Trigger out
1 * Clock out

4 * General I/O



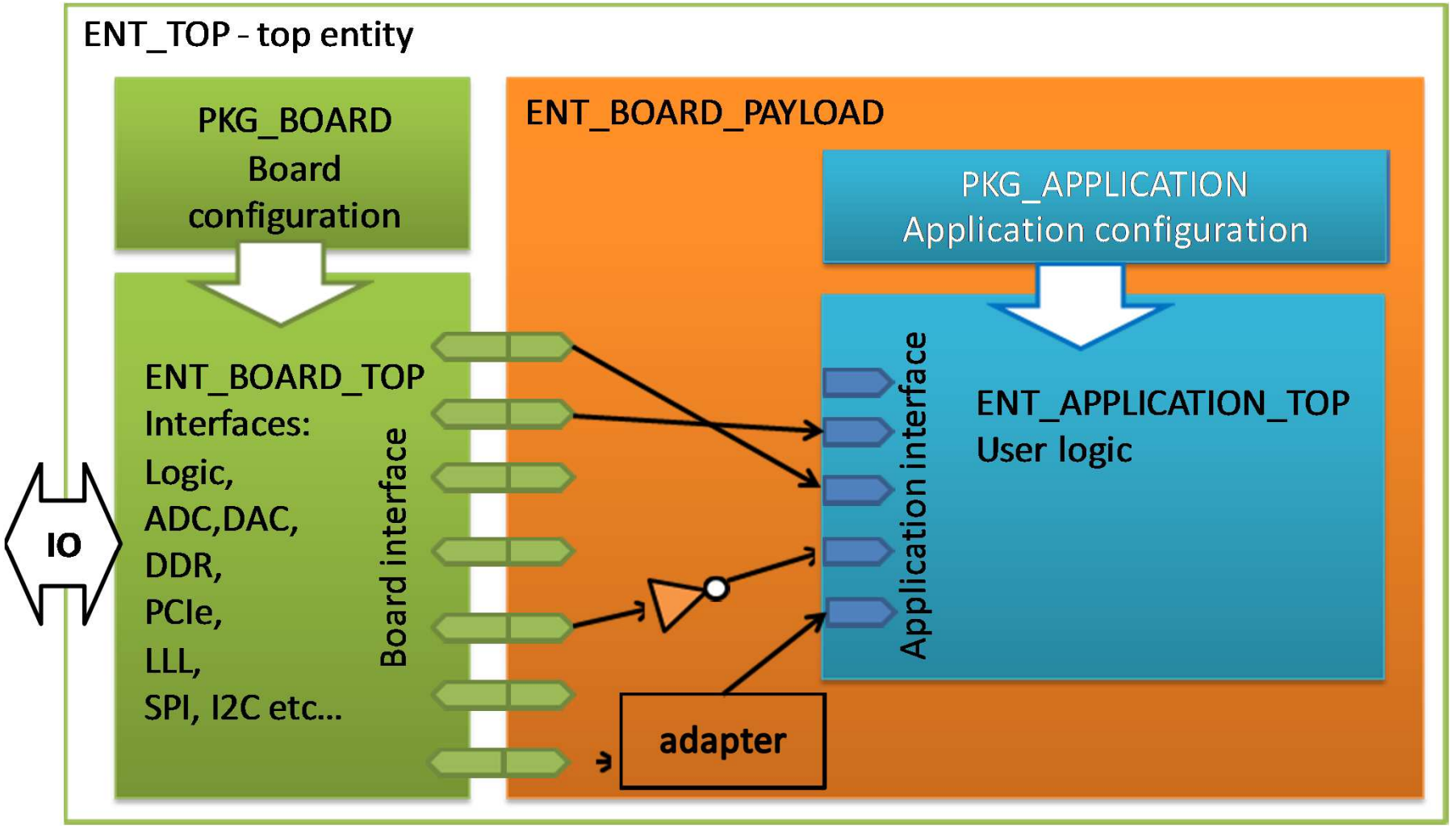
100 ps

With link length compensation active (over 4 km distribution)

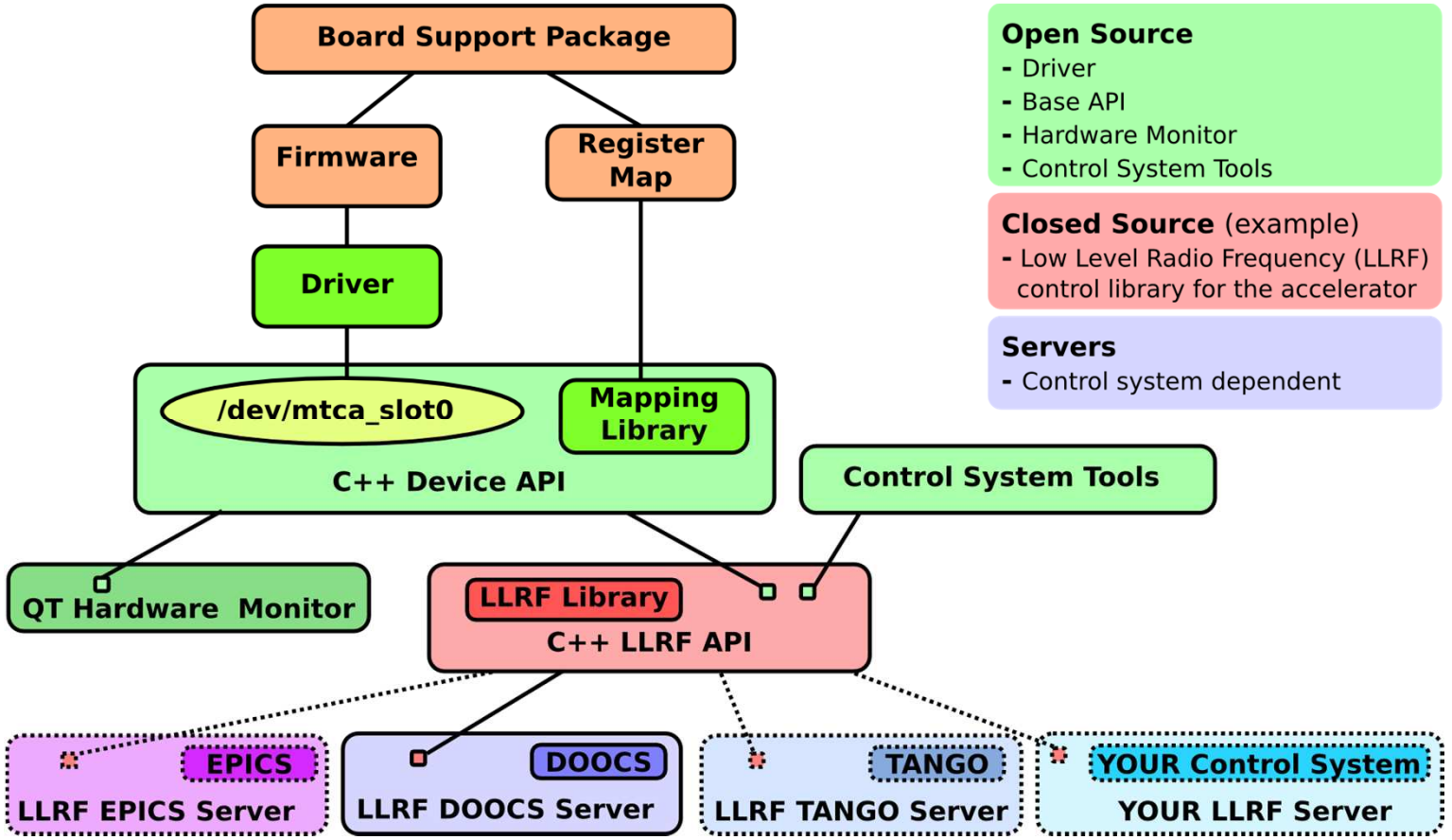
FYSIKUM

DESY

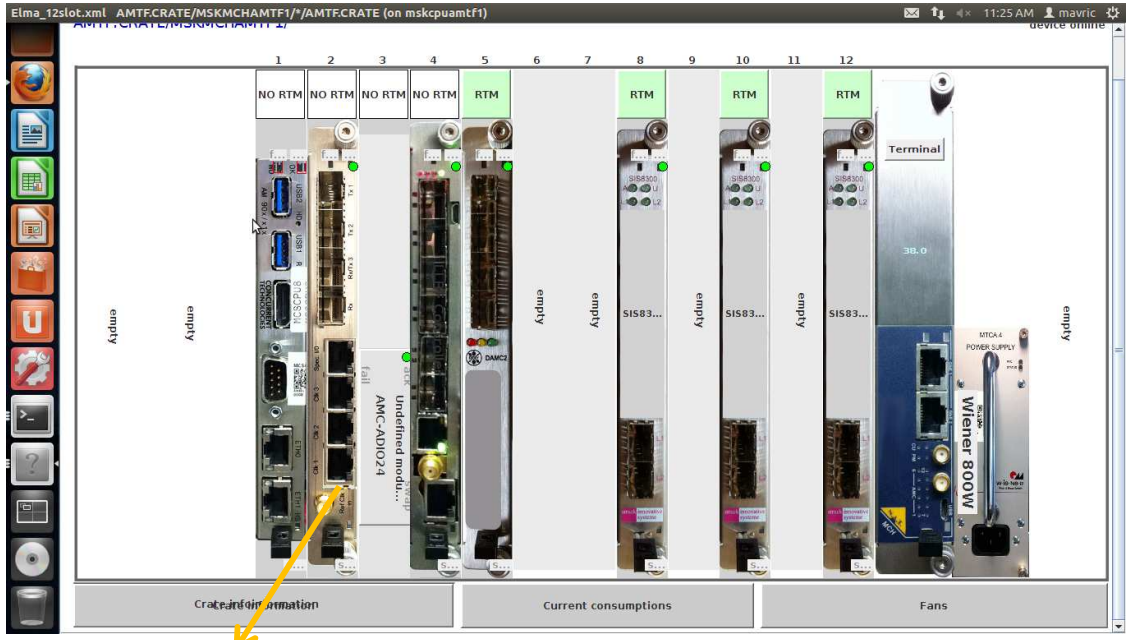
FPGA Structure.

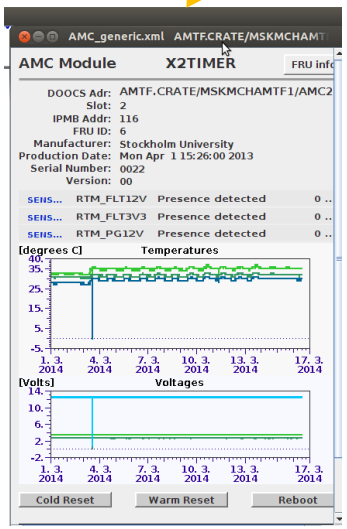


SW and Driver.



Platform Status Monitoring.





- jDDD based graphical interface for remote monitoring the HW status over IPMI (temperatures, voltages, currents, FRU information, HP status etc.)
- Individual board deactivation, remote crate/board restart, etc.

Platform Related Activities.

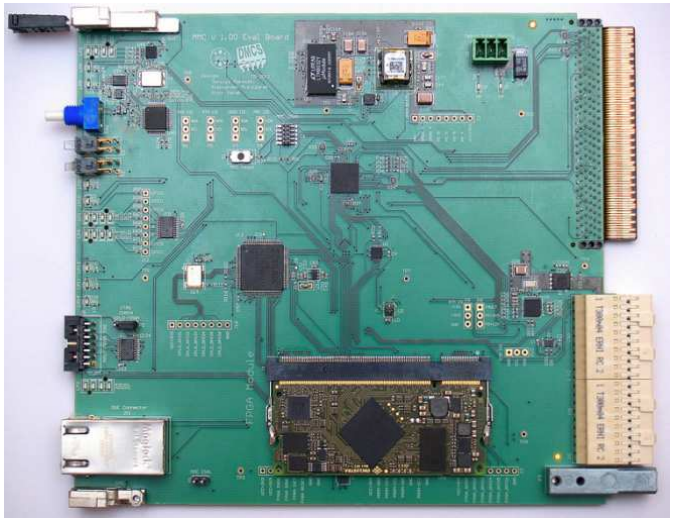
- Platform related issue and Interoperability were a major “showstopper” at the beginning:
  - Platform management related (FW and HW)
  - Debugging in collaboration with industry
  - Long debugging periods
- MTCA interoperability workshop
- 2,5 years of debugging in collaboration with industry
- Tracking of bugs:
  - RT (https://rt-system.desy.de/) - ~80 bugs reported and solved
  - Redmine (https://mskllrfredminesrv/projects/mtca4platform/issues?set_filter=1&tracker_id=1)
  - DESY Log-book (http://ttfinfo.desy.de/uTCAelog/index.jsp) – a list of bugs and procedures
- Regular bi-weekly meetings on Tuesdays (e.g. tomorrow 18.03.2014) starting at 9:15.

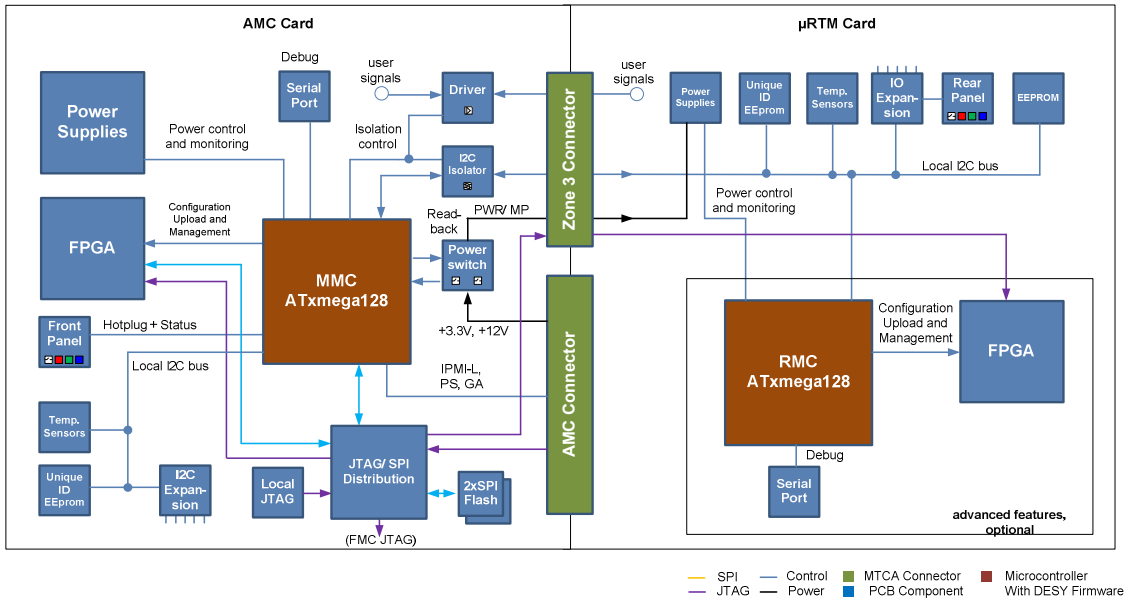
Everyone welcome to join!

Skype : mtca.4_meeting

Emal : uros.mavric@desy.de

MMC1.0.





- MMC1.0 unifies the MMC functionality (HW and FW) on all the presented boards.
- It offers a tested, ready-to-use solution for the AMC and RTM management controllers and tackles demands of various complexities (advanced and basic versions).
- A test/demo board is being tested and will be available (with FW).

Zone 3 Classes Recommendations in MTCA.4.

https://mtca.desy.de/resources/zone_3_recommendation/index_eng.html

- Class A1.x mainly for analog signal transmission over Zone 3
- Class D1.x for digital signal transmission over Zone 3
- Recommendation – no standardization to be open for future signal types

- Requires
  - AMC FPGA module based,
  - 2 ADF 30 pair (Mid-size) connectors
  - Class A1.x and D1.x needs not to be compatible

- Supports
  - LVDS, LVCMOS, OC, CML, analog differential
  - Digital signals (single-, diff.-ended, bi-directional)
  - Analog signals
  - High-speed links
  - non-FPGA low-jitter clock signals
  - non-FPGA signals with fixed direction
  - ps-stable timing signals

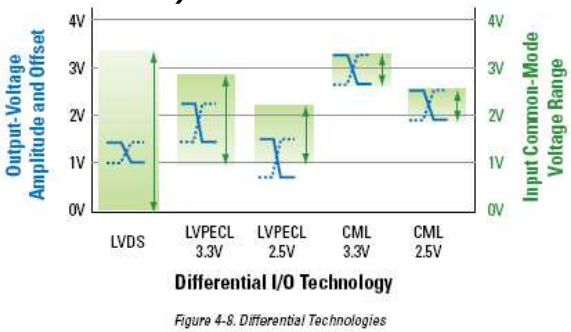
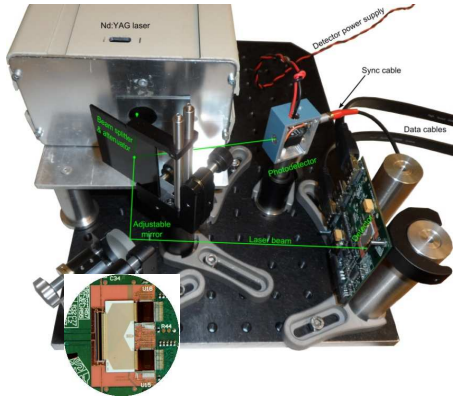


Figure 4-8. Differential Technologies

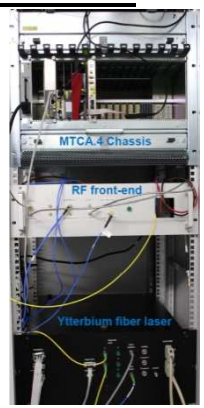
MTCA.4 in Practice at DESY.

- LLRF systems at FLASH, AMTF, CMTB, REGAE,…

Electro-optical detector

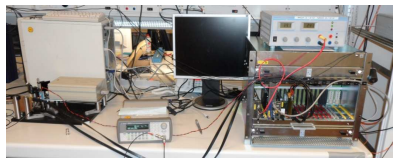


- Special Diagnostics



Laser Synchronization

EBPM




Thank you for your attention!