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AMC FMC carrier for CMS

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with acknowledgements & thanks to: John Jones, Jan Troska
FC7 (FMC Carrier – Xilinx Series 7)

- flexible, uTCA compatible card for generic CMS data acquisition/control uses

- suitable for production systems or prototyping/benchtop use

- collaborative effort between CERN & UK

- evolution of existing board designs (CERN GLIB & Imperial MP7)
overview of requirements/specifications

- uTCA AMC implemented as a generic **dual FMC carrier**
- Xilinx series 7 FPGA to support line rates up to **10Gbps**
- **simple solution**, minimise risk and reduce development time to maturity by basing design on existing hardware
TCDS (trigger, control & timing distribution) upgrade

- the FC7 will satisfy the role of both Local Partition Manager and Partition Interface boards using different FMC mezzanines
- system (70 boards) to be assembled over next 6-12 months

Phase I Pixel FED/FEC prototype

- development to begin in 2014
- could possibly satisfy role as final production board
November 2012
Spec approved

June 2013
First (incomplete) prototype submitted

July 2013
Majority of design validated, no major issues
Begin assembly of test system & firmware

August 2013
Re-spin submitted
First prototypes received (2)

September 2013
Re-spun prototypes received (2)
Design validated, one minor design issue
Serious manufacturing issues uncovered

November 2013
Informal Price Inquiry
Pre-production series submitted with two manufacturers

January 2014
Pre-production batch #1 received (10 pieces)

February 2014
Pre-production batch #2 received (2 pieces)

March 2014
70pcs ordered for TCDS
16 layers
Nelco N4000 13-EPSI
- low loss tangent
- low dielectric constant
- misaligned with PCB weave

good performance at ~10GHz (MP7)
reset switches
/JTAG
config

SRAM
decoupling

Kintex 7
FPGA

debug
header

oscillators/clock
generator-jitter
cleaner

AMC connector

FMC 1

FMC 2
high range Kintex 7 part pin compatible XC7K420T or XC7K480T (difference only in logic)

Kintex 7 FPGA

XC7K420T
35mm x 35mm
416,960 logic cells
30Mb total block RAM
400 IO, 32 GTX MGTs

‘-2’ speed grade – MGTs support 10Gbps (10.3125Gbps max)
I/O operates up to 3.3V signalling
- supports legacy FMCs
supports **LPC mezzanines** with extended functionality - a total of **20 multi-gigabit lines** & **136 user IO** to the front panel

**FMC 1**
- 12 MGT pairs
- 68 user IO (34 differential)

**FMC 2**
- 68 user IO (34 differential)
- 8 MGT pairs

**FC7 is FMC spec compliant but can also accommodate non-standard mezzanines & stacking heights**
FC7: oscillators

125MHz (GbE-system clock)
156.25MHz (SRIO clock)
40.08MHz (LHC clock)
programmable (not mounted)

programmable clock generator & jitter cleaner (required for LHC/TCDS/GBT applications)
Switch to power card from +12V header or via crate.

CPLD JTAG header & switched JTAG header (FPGA/uC/FMC_L12/FMC_L8)

uC, FPGA reload and configurable resets
FC7: bottom view

- Flash power
- CPLD
- USB
- aux power
- uSD
- uC
- FMC 1 power
- SRAM
- FPGA decoupling
- FPGA core power
- SRAM power
- analogue power
- clocking switching logic
- general power
- AMC connector
FC7: DDR3 SRAM

RAM required for buffering short term event information, statuses, low rate event data

4Gb DDR3 RAM (2 ICs of 128M x 16bit)

XC7K420T supports a max DDR3 rate of 1066MT/s per pin (533MHz)

design specified to 480MHz - 30Gbps maximum bandwidth (R+W)
GLIB based flexible clocking tree required to cope with range of FC7 applications and open nature of a multi purpose FMC carrier.

supports virtually any MGT protocol to FMCs
- either natively or via an on-mezzanine source
- fully compatible with GBT link operation (via a dedicated mezzanine)
FC7: backplane links

<table>
<thead>
<tr>
<th>Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 0</td>
<td>GbE</td>
</tr>
<tr>
<td>Port 1</td>
<td>GbE or AMC13-DAQ*</td>
</tr>
<tr>
<td>Port 2</td>
<td>SATA/SAS</td>
</tr>
<tr>
<td>Port 3</td>
<td>SATA/SAS or AMC13-TTC/S (LVDS)</td>
</tr>
<tr>
<td>Ports 4-7</td>
<td>PCIe/SRIO*</td>
</tr>
<tr>
<td>Ports 8-11</td>
<td>Ext Fat-Pipe (SRIO/10GbE XAUI)*</td>
</tr>
<tr>
<td>Ports 12-15</td>
<td>LVDS I/O</td>
</tr>
<tr>
<td>Ports 17-20</td>
<td>unused</td>
</tr>
<tr>
<td>FCLKA</td>
<td>AMC13-TTC or PCIe clocks</td>
</tr>
<tr>
<td>TCLKA/TCLKC</td>
<td>telecoms clock inputs</td>
</tr>
<tr>
<td>TCLKB/TCLKD</td>
<td>telecoms clock outputs</td>
</tr>
</tbody>
</table>

Designed to be compatible with both uTCA for CMS and AMC.[1,4] standards

Supports range of MGT protocols to backplane
FC7: board services

- **flash**
- **CPLD**
- **USB**
- **aux power**
- **uSD**
- **uC**

**FPGA, peripherals & power configuration and management based on MP7**

- Serial line to microcontroller for uC bootloading or user data transfer
- MicroSD card for storage of multiple firmware images, calibration constants, persistent data
- AMC power (MMC) management, peripherals communication, FPGA configuration/firmware loading
FMC and backplane connectivity

- tests on all **general IO** lines to/from FPGA (single ended)

- loopback FMCs (AF-101) & loopback AMC test board (SMA Ultra-9000)

- marching ‘1’s test at 40MHz demonstrate **full connectivity**
FMC and backplane connectivity

- tests on all high speed differential lines to/from FPGA

- IBERT bit test firmware to test serial (GTX) transceivers to backplane (5Gbps) and FMCs (10Gbps) in loopback
FMC and backplane connectivity

- tests on all high speed differential lines to/from FPGA

- IBERT bit test firmware to test serial (GTX) transceivers to backplane (5Gbps) and FMCs (10Gbps) in loopback

full connectivity demonstrated

all transceivers working at specified line rates

0 bit errors in >10^{15} transmitted bits (BER<10^{-14}) using a PRBS-31 data pattern
other connectivity

**DDR3 RAM** -> early testing indicates good operation (no R/W errors) at 480MHz using a pre-built Xilinx traffic generator

**clocking logic** -> no issues detected with clocking scheme, oscillators or programmable clock generator so far, difficult to cover full phase space!

-> more tests needed

**crate operation** -> MMC functionality (board power management, IMPI communication) verified, communication over GbE on Port 0 (IPBus) works

-> sensor data reporting functionality to be added
FMC SERDES

electrical transmission at 10Gbps on FMC MGTs using XM104 (access to two channels)

electrical eyes are wide open for both FMC slots

jitter measured to be ~20ps

channel to channel jitter spread ~1.7ps

easily meets SFF-8431 specifications for SFP+ modules at 10Gb/s of 27.2ps
FMC SERDES

optical transmission at 10Gbps on FMC MGTs using Faster Technology FM-S18 and SFP+ in loopback with variable attenuator

running IBERT test in loopback

initial testing (850nm MM) indicates that the carrier does not degrade performance of optical transceiver (<-11.1dBm)

need more work to define a systematic test stand (well characterised reference FMCs, SFP+s and carriers)
backplane SERDES

electrical transmission at 5Gbps on AMC MGTs using SMA Ultra-9000 and in the crate with the AMC13XG

excellent eyes at 5Gbps (~46ps jitter)

test of Port 1 (CMS DAQ link) between FC7 and AMC13XG using IBERT bit tests using PRBS-31 – no errors in >10^{13} bits

RX bathtub curves on both AMC13 and FC7 on Port 1 0.45UI open
mature version of f/w for basic board control available

- very similar in structure & content to GLIB f/w

- separate user (custom) and system (IPbus & register space, clock & peripherals control) spaces

- available on SVN, much more to come (DDR3, clock control, firmware loading...)

software for basic board control available

https://svnweb.cern.ch/cern/wsvn/ph-ese/be/fc7

ph-ese - Rev 1564
(root)/be/fc7/trunk/fc7_r0/src/sys/

Last modification - Compare with Previous - View Log - Download - RSS
Local Partition Manager (LPM)

- 2x 10Gb/s <-> DAQ
- 8x TTC/TTS <-> TCDS fanout (PI)
- Backplane <-> AMC13

Partition Interface (PI)

- 2x TTC/TTS <-> LPM
- 10x TTC/TTS <-> FEDs
- RJ45 TTS <-> Legacy systems
CMS (CERN/IC) board, merge between MP7 & GLIB

Dual LPC FMC carrier
- w/ additional SERDES as in HPC

Successful preproduction

Mature FPGA firmware

First application (TCDS) already launched production

More to come!