xTCA Interest Group meeting,
CERN, 17.03.14

FC7
AMC FMC carrier for CMS

Mark Pesaresi (Imperial College), Paschalis Vichoudis (CERN)

Magnus Hansen, Francois Vasey (CERN)
Greg Iles, Sarah Greenwood, Andrew Rose, Geoff Hall (Imperial College)

with acknowledgements & thanks to: John Jones, Jan Troska

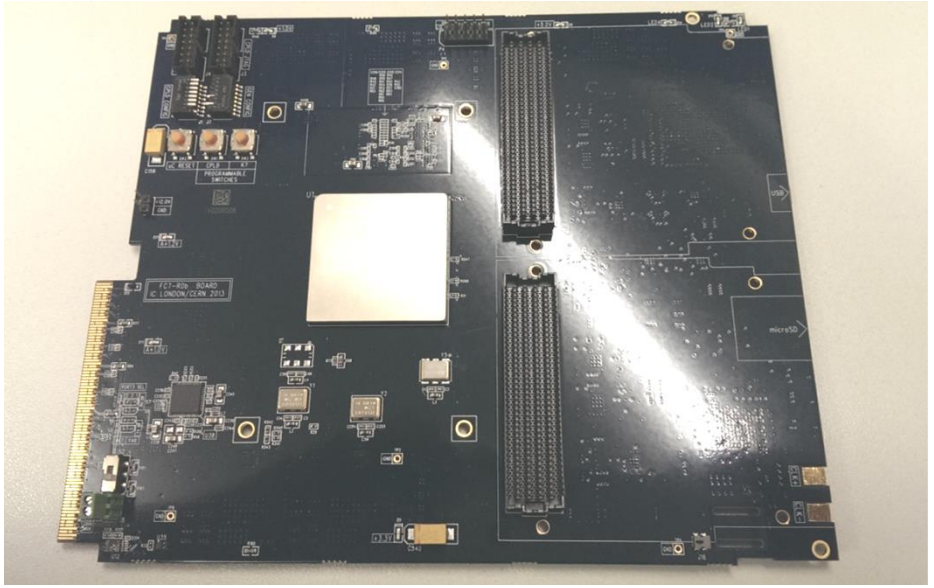
FC7 (**F**MC **C**arrier – Xilinx Series **7**)

- flexible, uTCA compatible card for generic CMS data acquisition/control uses

- suitable for production systems or prototyping/benchtop use

- collaborative effort between CERN & UK

- evolution of existing board designs (CERN GLIB & Imperial MP7)



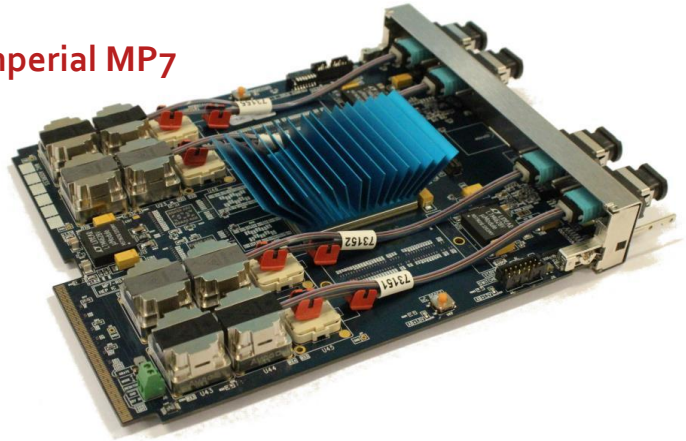
overview of requirements/specifications

- uTCA AMC implemented as a generic **dual FMC carrier**

- Xilinx series 7 FPGA to support line rates up to **10Gbps**

- **simple solution**, minimise risk and reduce development time to maturity by basing design on existing hardware

Imperial MP7



CERN GLIB

MP7 experience with 10Gbps & advanced services

merge

GLIB FMC layout/schematic expertise

TCDS (trigger, control & timing distribution) upgrade

- the FC7 will satisfy the role of both Local Partition Manager and Partition Interface boards using different FMC mezzanines
- system (70 boards) to be assembled over next 6-12 months

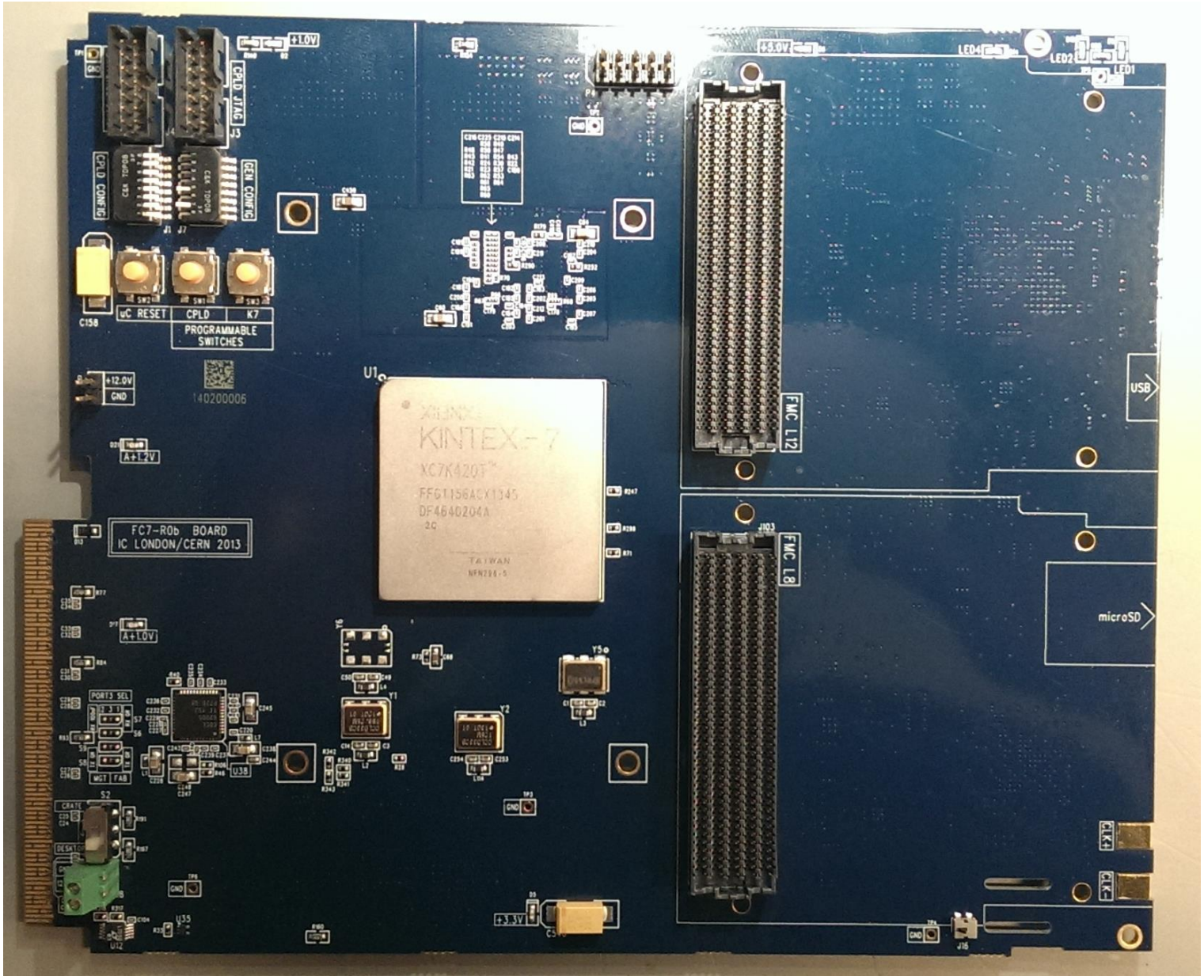
Phase I Pixel FED/FEC prototype

- development to begin in 2014
- could possibly satisfy role as final production board

development history

March 2014	70pcs ordered for TCDS
February 2014	Pre-production batch #2 received (2 pieces)
January 2014	Pre-production batch #1 received (10 pieces)
November 2013	Informal Price Inquiry Pre-production series submitted with two manufacturers
September 2013	Re-spun prototypes received (2) Design validated, one minor design issue Serious manufacturing issues uncovered
August 2013	Re-spin submitted
July 2013	First prototypes received (2) Majority of design validated, no major issues Begin assembly of test system & firmware
June 2013	First (incomplete) prototype submitted
November 2012	Spec approved

FC7: top view

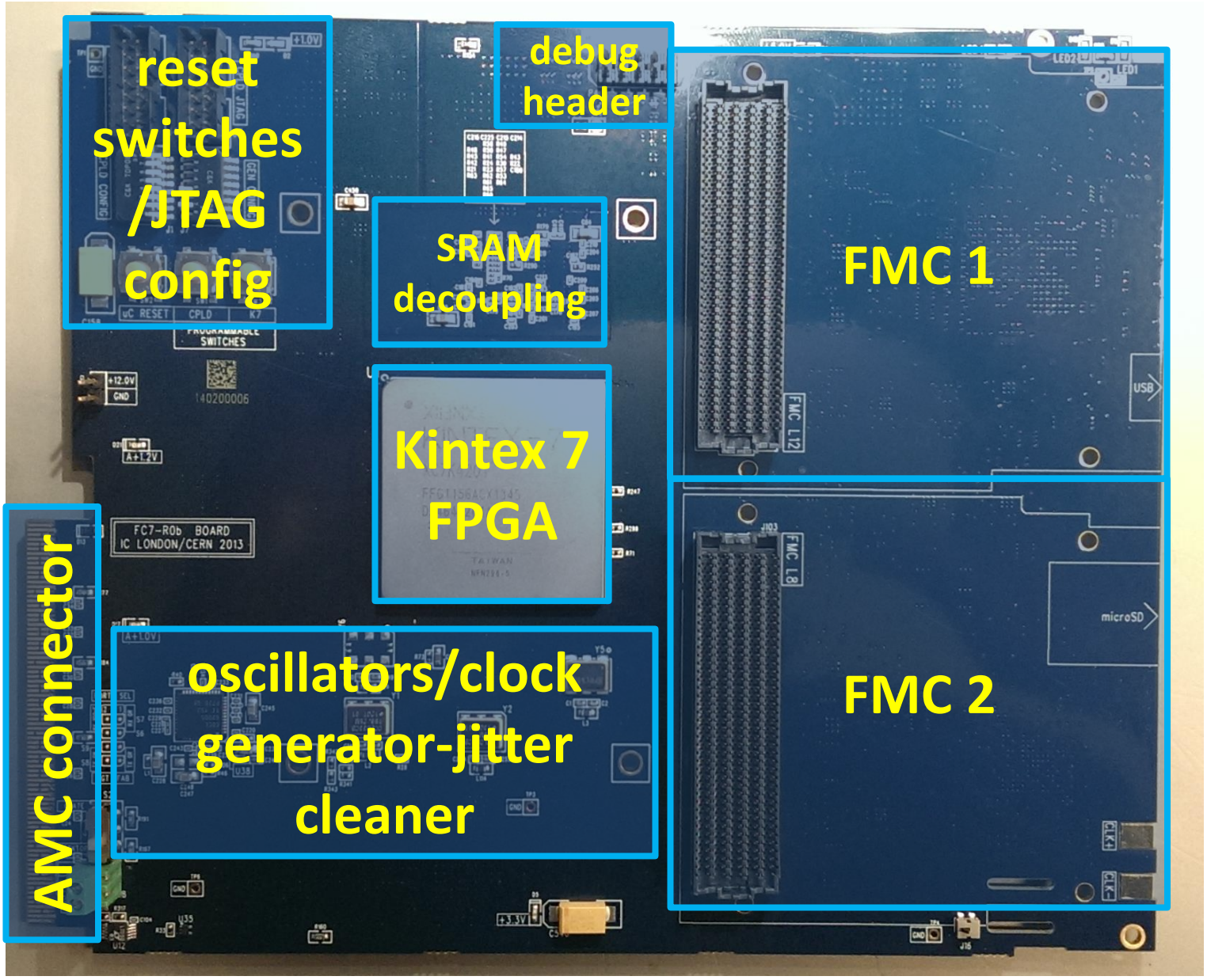


16 layers
Nelco N4000 13-EPSI

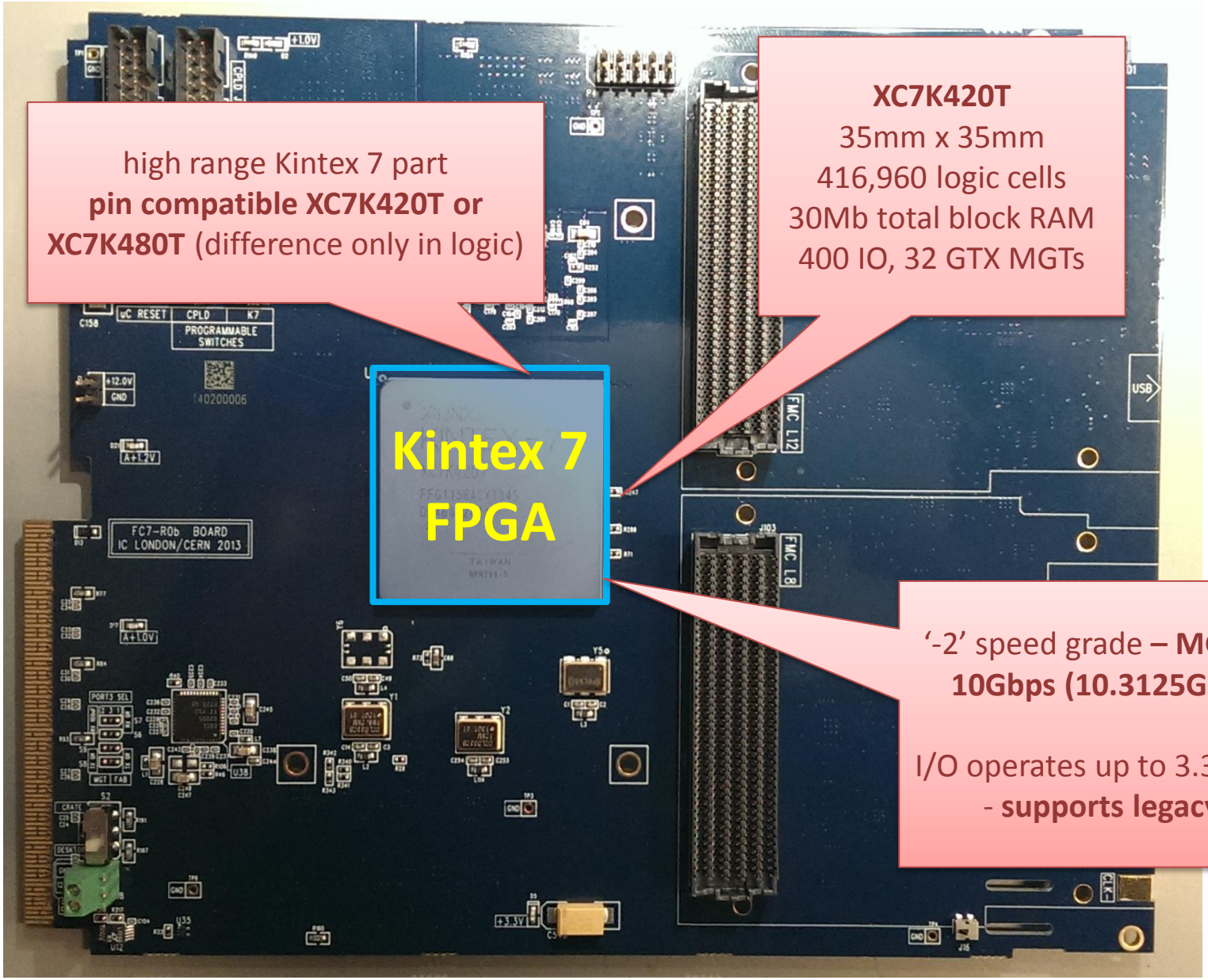
- low loss tangent
- low dielectric constant
- misaligned with PCB weave

good performance at ~10GHz (MP7)

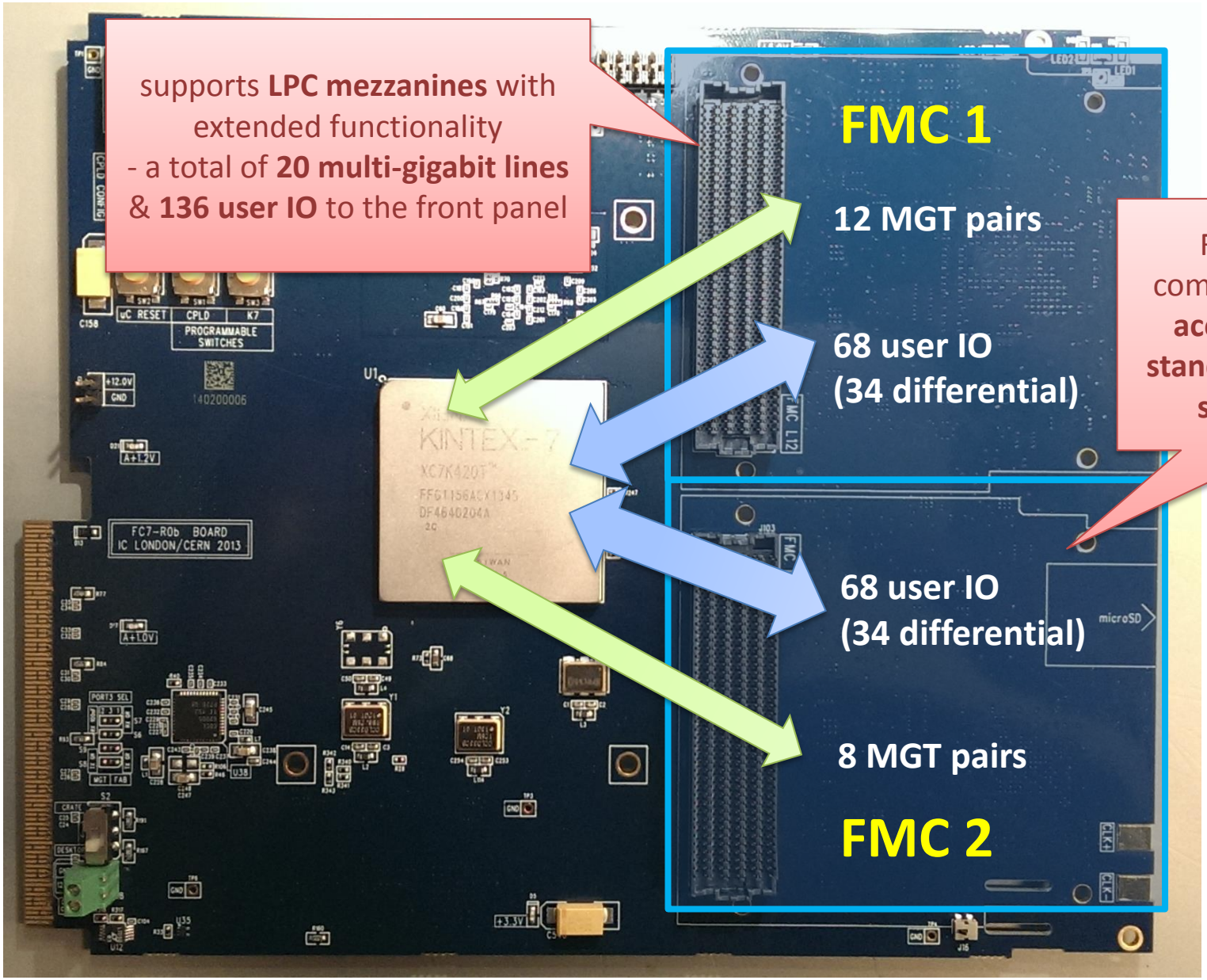
FC7: top view


reset switches /JTAG config
debug header
SRAM decoupling
FMC 1
Kintex 7 FPGA
AMC connector
oscillators/clock generator-jitter cleaner
FMC 2
FC7-R0b BOARD
IC LONDON/CERN 2013
FMC L12
FMC L8
USB
microSD

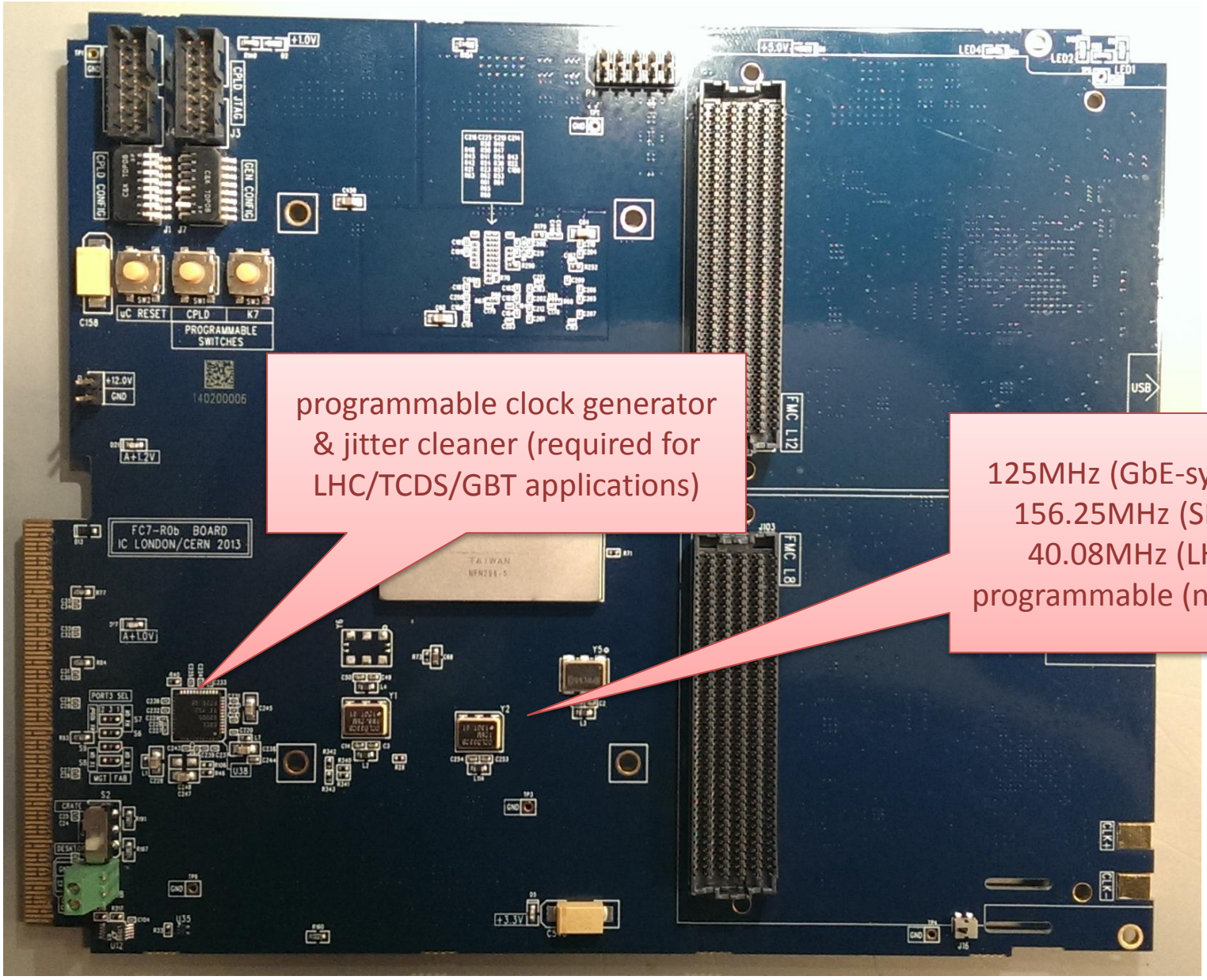
FC7: FPGA


high range Kintex 7 part
pin compatible XC7K420T or XC7K480T (difference only in logic)
XC7K420T
35mm x 35mm
416,960 logic cells
30Mb total block RAM
400 IO, 32 GTX MGTs
Kintex 7 FPGA
'-2' speed grade – **MGTs support 10Gbps (10.3125Gbps max)**
I/O operates up to 3.3V signalling - **supports legacy FMCs**
FC7-R0b BOARD
IC LONDON/CERN 2013
FMC L12
FMC L8
USB

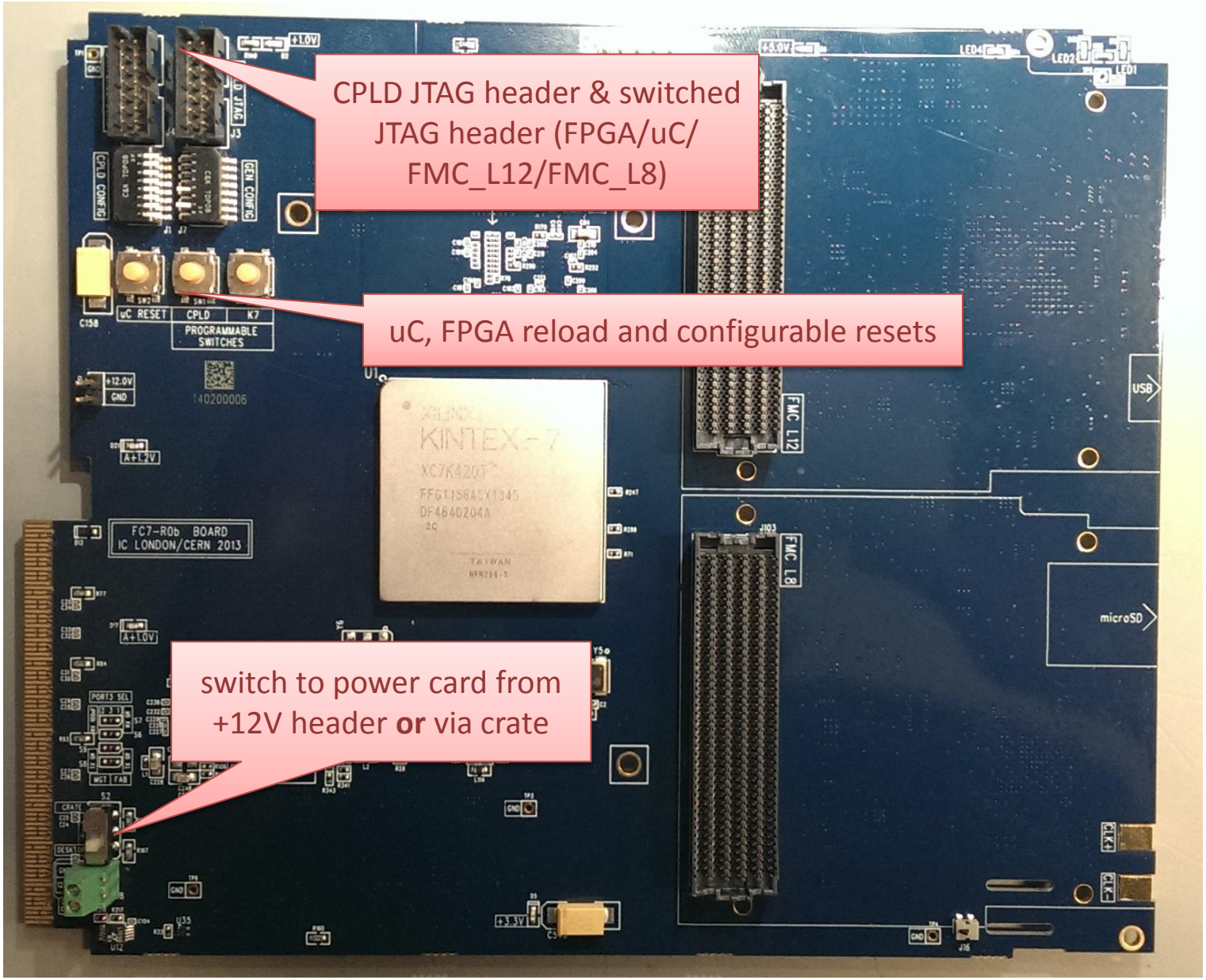
FC7: FMCs


supports **LPC mezzanines** with extended functionality
- a total of **20 multi-gigabit lines** & **136 user IO** to the front panel
FMC 1
12 MGT pairs
68 user IO (34 differential)
68 user IO (34 differential)
8 MGT pairs
FMC 2
FC7 is FMC spec compliant but **can also accommodate non-standard mezzanines & stacking heights**
FC7-R0b BOARD
IC LONDON/CERN 2013
KINTEX-7
microSD

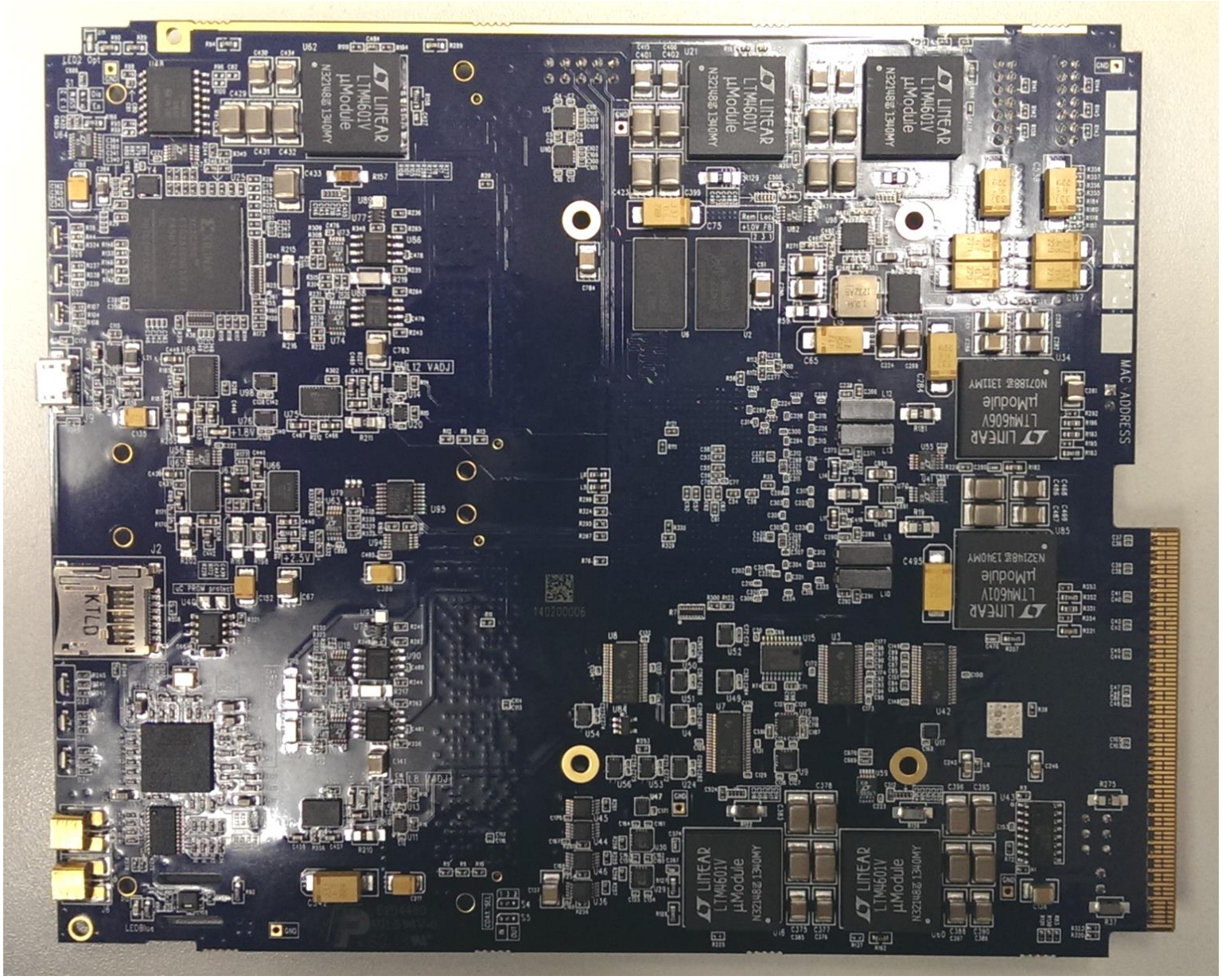
FC7: oscillators



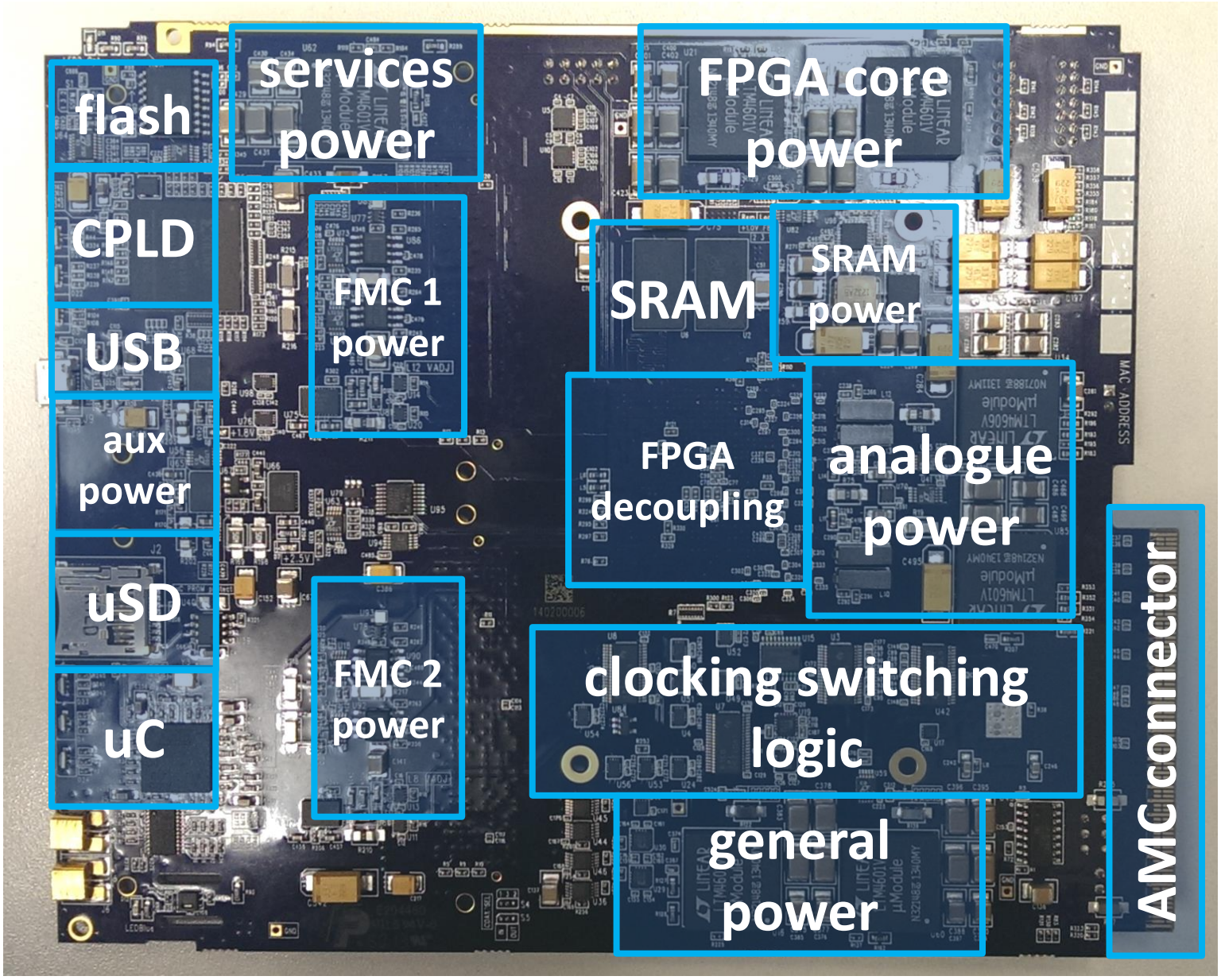
FC7: configuration



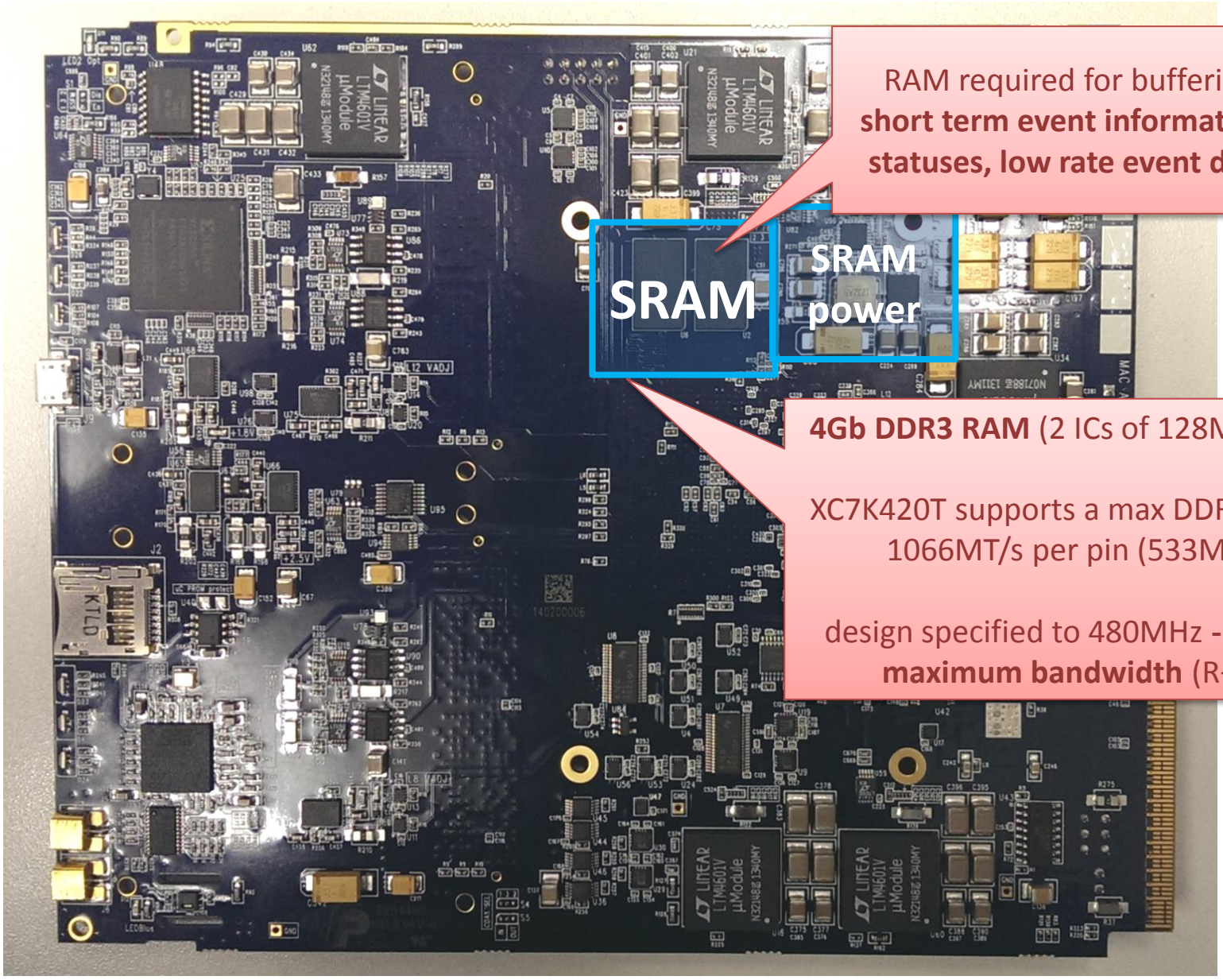
FC7: bottom view



FC7: bottom view



FC7: DDR3 SRAM



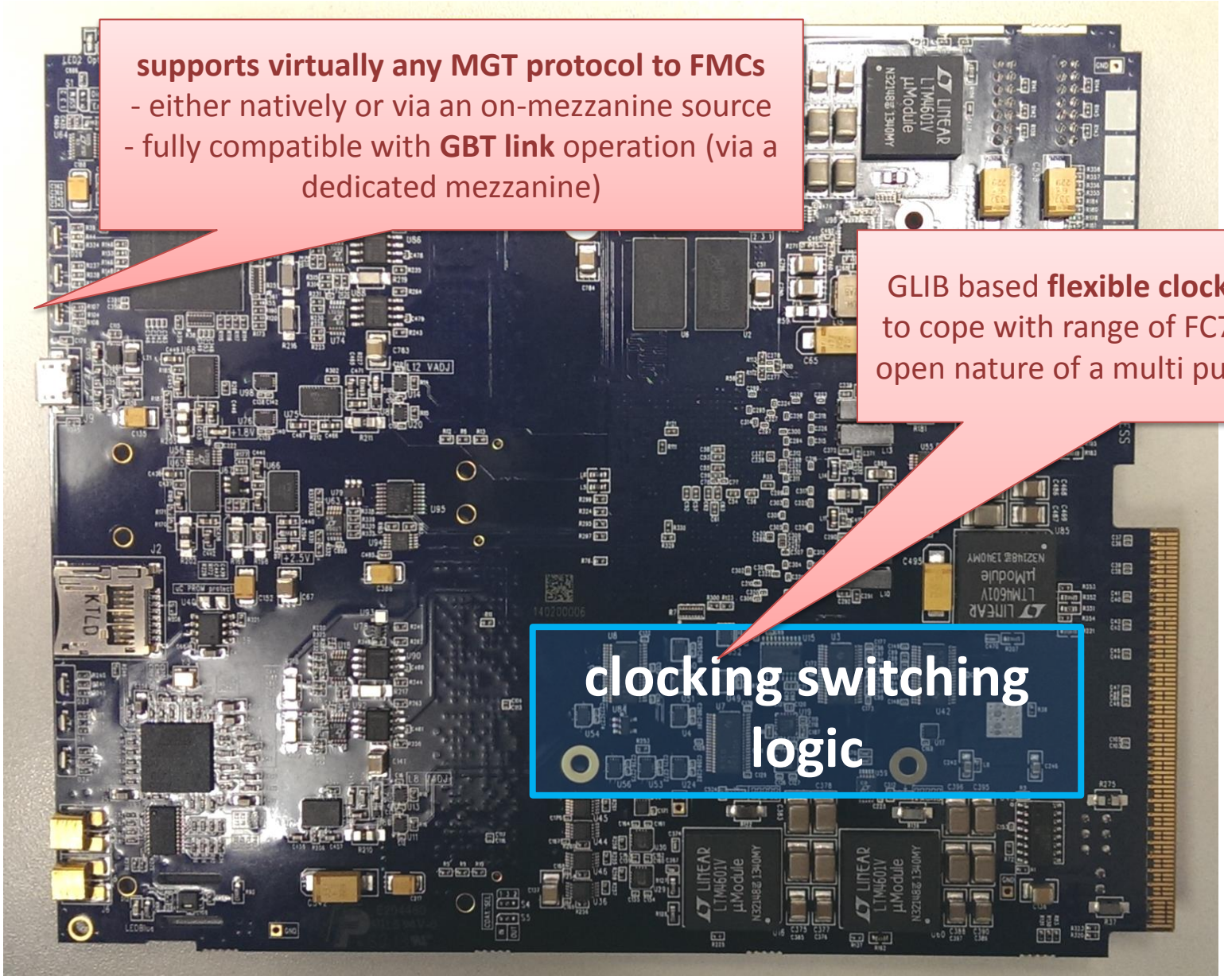
RAM required for buffering **short term event information, statuses, low rate event data**

4Gb DDR3 RAM (2 ICs of 128M x 16bit)

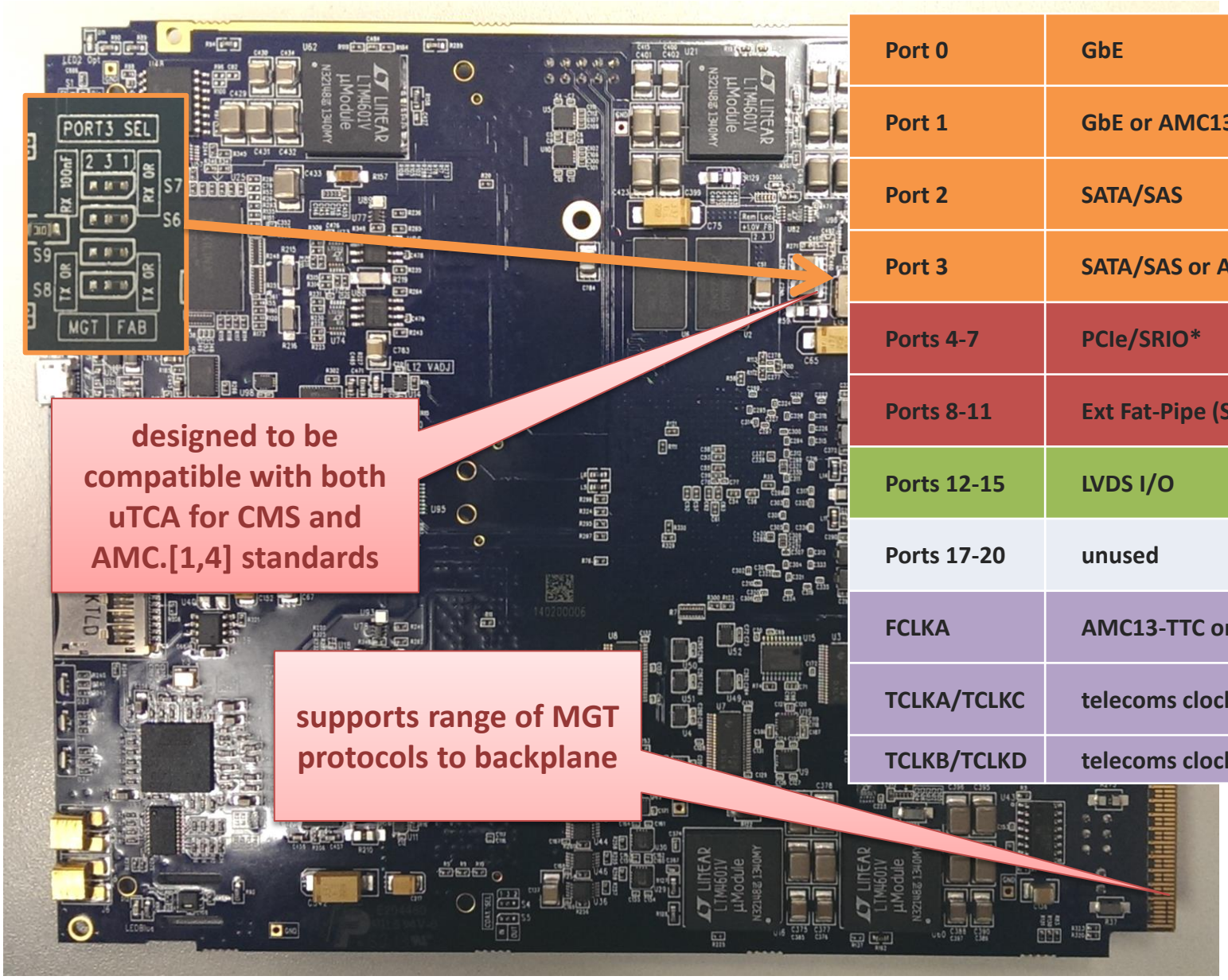
XC7K420T supports a max DDR3 rate of 1066MT/s per pin (533MHz)

design specified to 480MHz **- 30Gbps maximum bandwidth** (R+W)

FC7: clocking tree

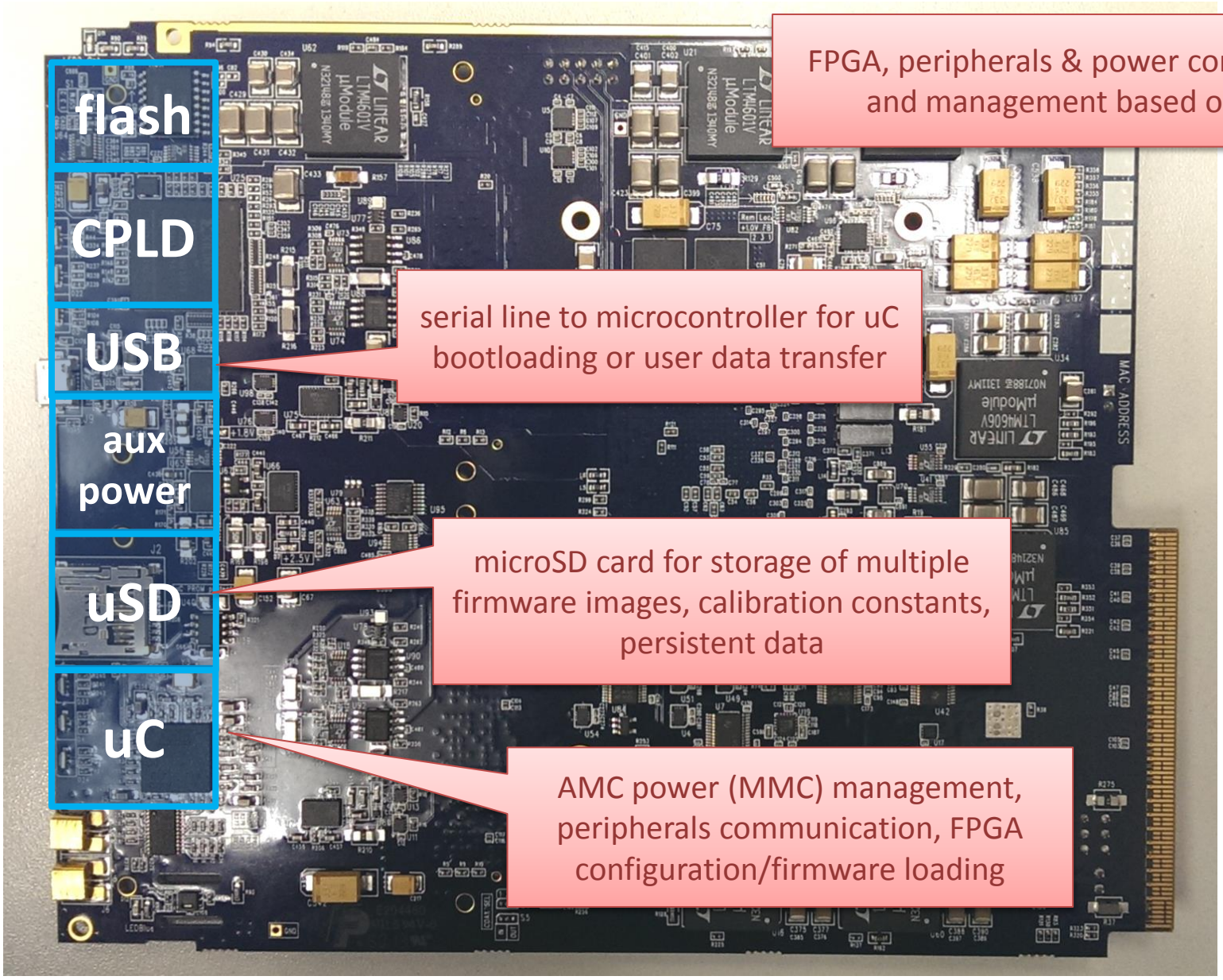


FC7: backplane links



Port 0	GbE
Port 1	GbE or AMC13-DAQ*
Port 2	SATA/SAS
Port 3	SATA/SAS or AMC13-TTC/S (LVDS)
Ports 4-7	PCIe/SRIO*
Ports 8-11	Ext Fat-Pipe (SRIO/10GbE XAUI)*
Ports 12-15	LVDS I/O
Ports 17-20	unused
FCLKA	AMC13-TTC or PCIe clocks
TCLKA/TCLKC	telecoms clock inputs
TCLKB/TCLKD	telecoms clock outputs

FC7: board services

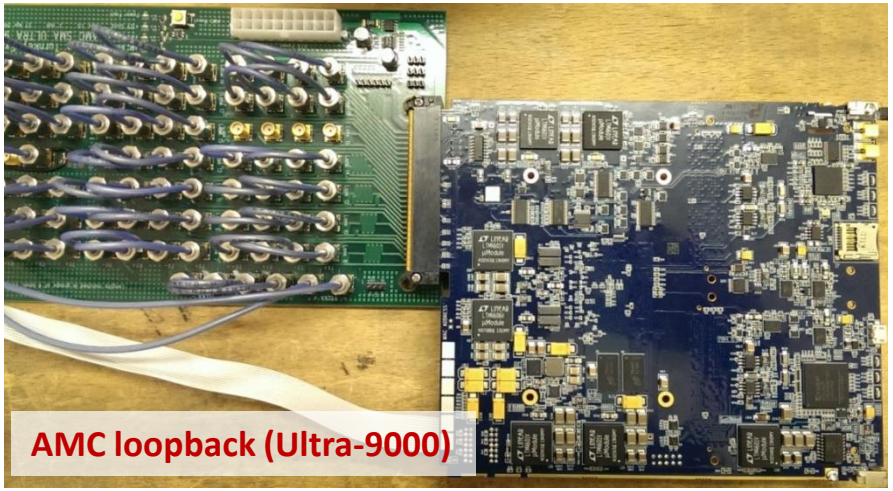


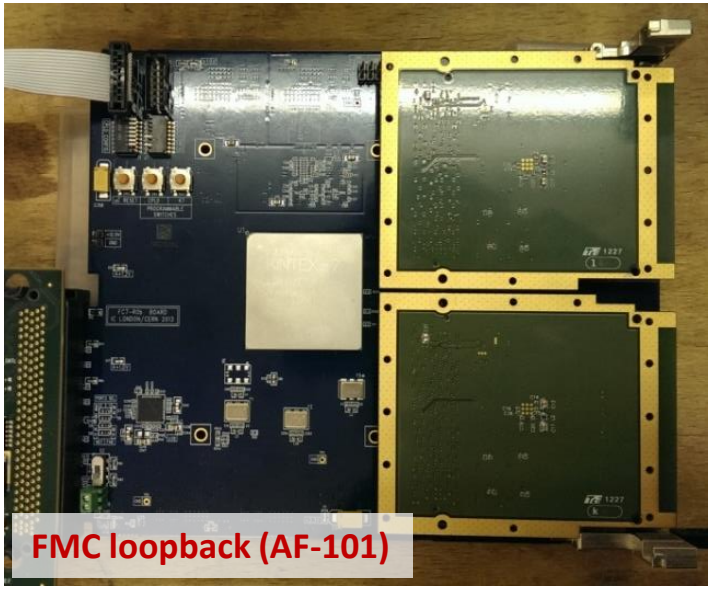
FMC and backplane connectivity

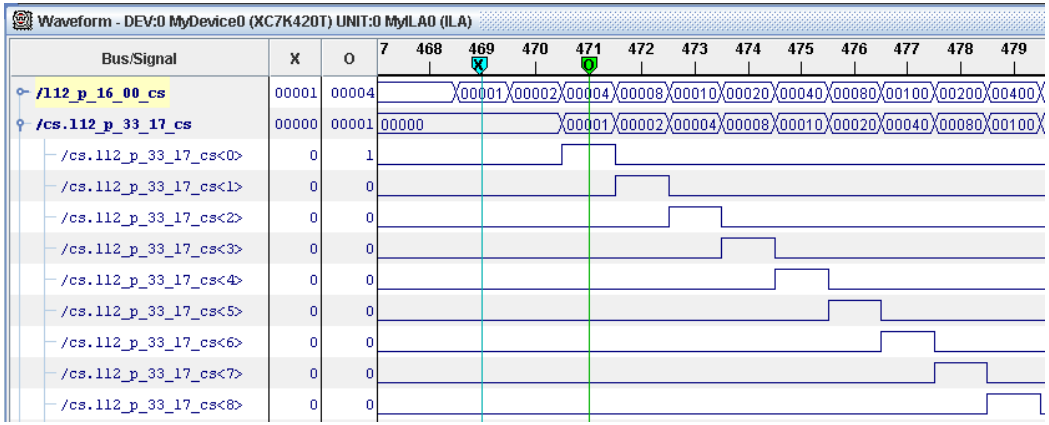
- tests on all **general IO** lines to/from FPGA (single ended)

- loopback FMCs (AF-101) & loopback AMC test board (SMA Ultra-9000)

- marching ‘1’s test at 40MHz demonstrate **full connectivity**



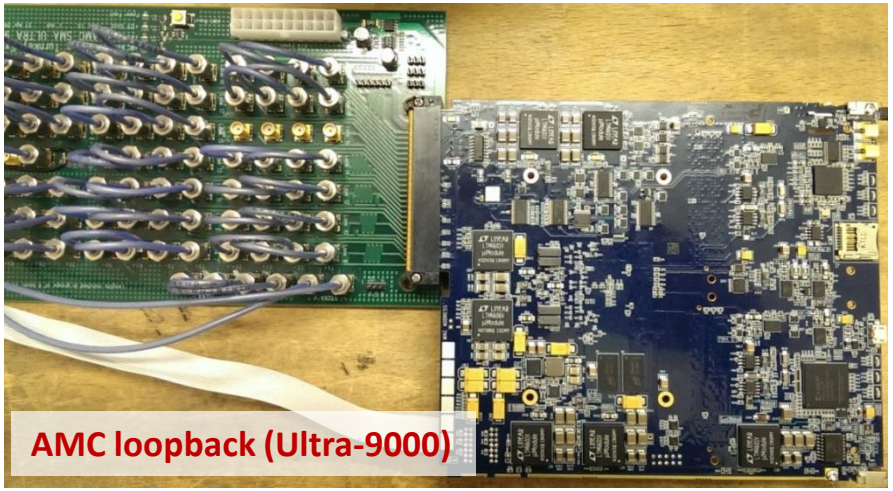




FMC and backplane connectivity

- tests on **all high speed** differential lines to/from FPGA

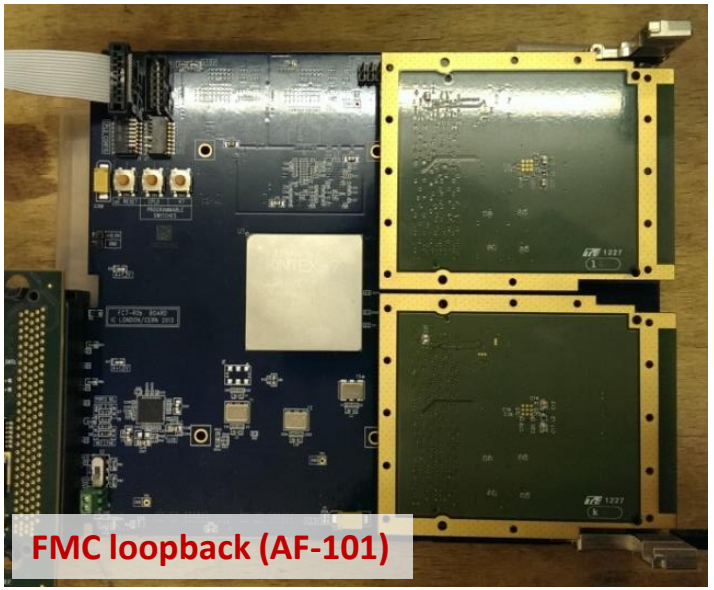
- IBERT bit test firmware to test serial (GTX) transceivers to backplane (5Gbps) and FMCs (10Gbps) in loopback



IBERT Console - DEV:0 MyDevice0 (XC7K420T) UNIT:1_0 MyIBERT K7 GTX1_0 (IBERT K7 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | RX Margin Analysis

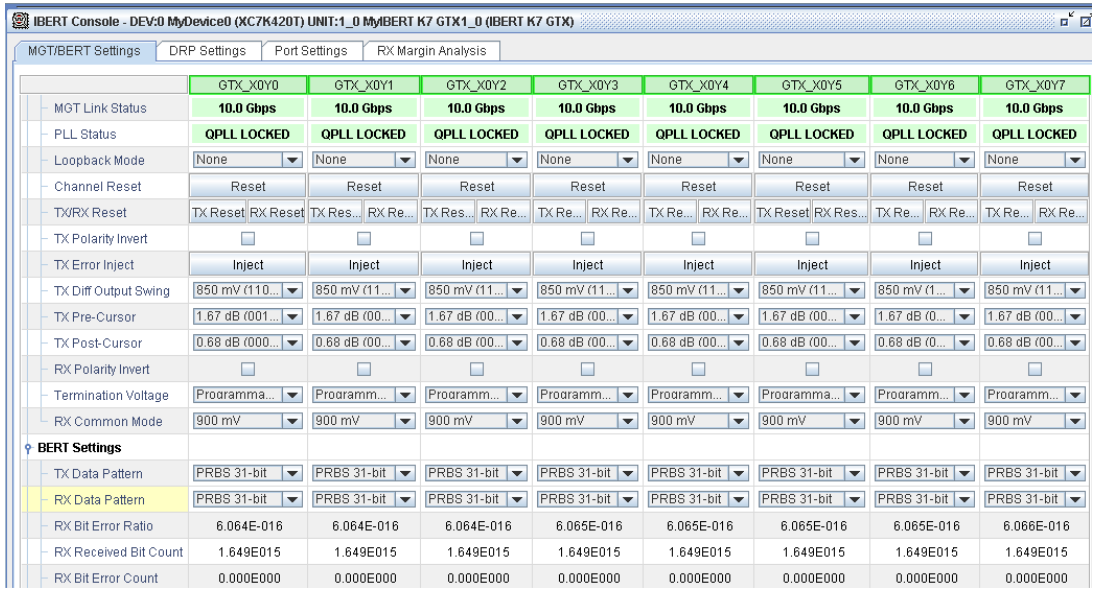
	GTX_X0Y0	GTX_X0Y1	GTX_X0Y2	GTX_X0Y3	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Link Status	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps	10.0 Gbps
PLL Status	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED	QPLL LOCKED
Loopback Mode	None	None	None	None	None	None	None	None
Channel Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
TX/RX Reset	TX Reset / RX Reset	TX Res... / RX Re...	TX Res... / RX Re...	TX Re... / RX Re...	TX Re... / RX Re...	TX Reset / RX Res...	TX Re... / RX Re...	TX Re... / RX Re...
TX Polarity Invert	☐	☐	☐	☐	☐	☐	☐	☐
TX Error Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	850 mV (110...	850 mV (11...	850 mV (11...	850 mV (11...	850 mV (11...	850 mV (11...	850 mV (1...	850 mV (11...
TX Pre-Cursor	1.67 dB (001...	1.67 dB (00...	1.67 dB (00...	1.67 dB (00...	1.67 dB (00...	1.67 dB (00...	1.67 dB (0...	1.67 dB (00...
TX Post-Cursor	0.68 dB (000...	0.68 dB (00...	0.68 dB (00...	0.68 dB (00...	0.68 dB (00...	0.68 dB (00...	0.68 dB (0...	0.68 dB (00...
RX Polarity Invert	☐	☐	☐	☐	☐	☐	☐	☐
Termination Voltage	Programma...	Programm...	Programm...	Programm...	Programm...	Programma...	Programm...	Programm...
RX Common Mode	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV	900 mV
BERT Settings								
TX Data Pattern	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit
RX Data Pattern	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit	PRBS 31-bit
RX Bit Error Ratio	6.064E-016	6.064E-016	6.064E-016	6.065E-016	6.065E-016	6.065E-016	6.065E-016	6.066E-016
RX Received Bit Count	1.649E015	1.649E015	1.649E015	1.649E015	1.649E015	1.649E015	1.649E015	1.649E015
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000	0.000E000



FMC and backplane connectivity

- tests on **all high speed** differential lines to/from FPGA

- IBERT bit test firmware to test serial (GTX) transceivers to backplane (5Gbps) and FMCs (10Gbps) in loopback



full connectivity demonstrated

all transceivers working at specified line rates

0 bit errors in >10^{15} transmitted bits (BER<10^{-14}) using a PRBS-31 data pattern

batch #1: reception testing

other connectivity

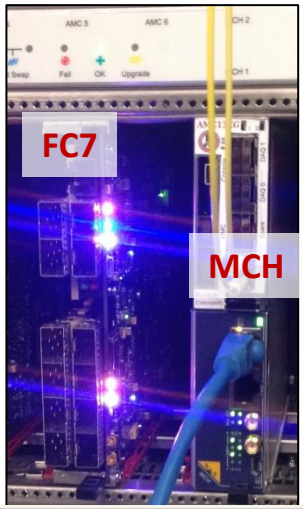
DDR3 RAM -> early testing indicates good operation (no R/W errors) at 480MHz using a pre-built Xilinx traffic generator

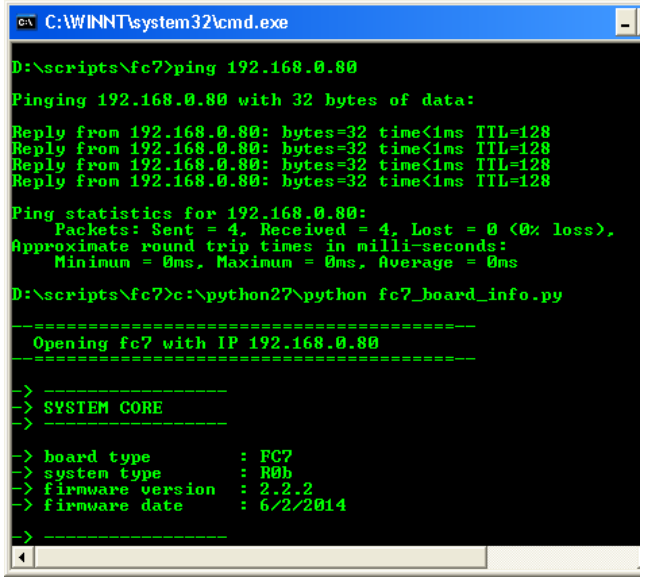
clocking logic -> no issues detected with clocking scheme, oscillators or programmable clock generator so far, difficult to cover full phase space!

-> more tests needed

crate operation -> MMC functionality (board power management, IMPI communication) verified, communication over GbE on Port 0 (IPBus) works

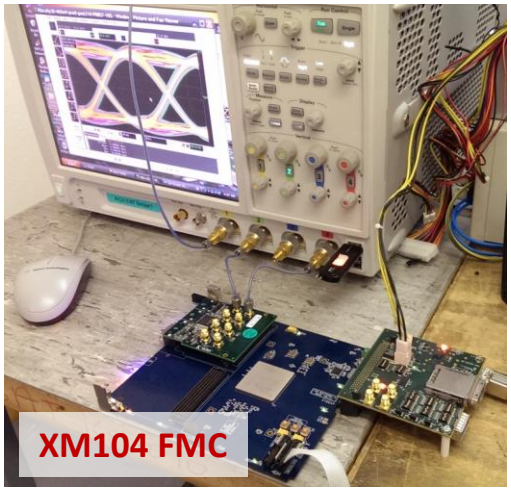
-> sensor data reporting functionality to be added





FMC SERDES

electrical transmission at 10Gbps on FMC MGTs using XM104 (access to two channels)

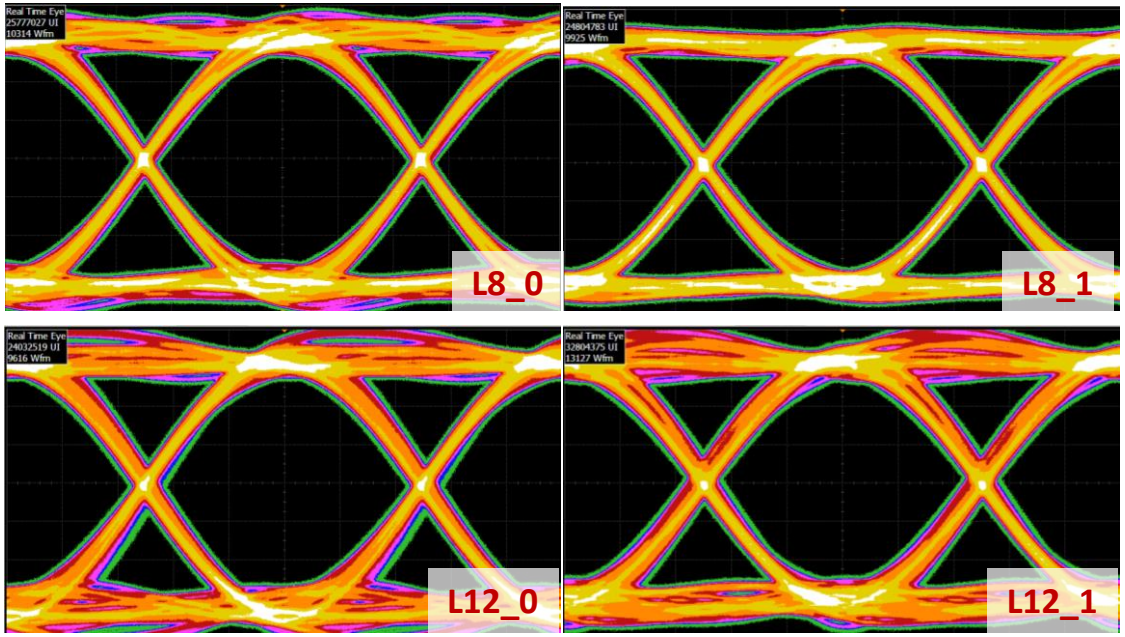


electrical eyes **are wide open** for both FMC slots

jitter measured to be ~**20ps**

channel to channel jitter spread ~**1.7ps**

easily **meets SFF-8431 specifications** for SFP+ modules at 10Gb/s of 27.2ps



batch #1: performance testing

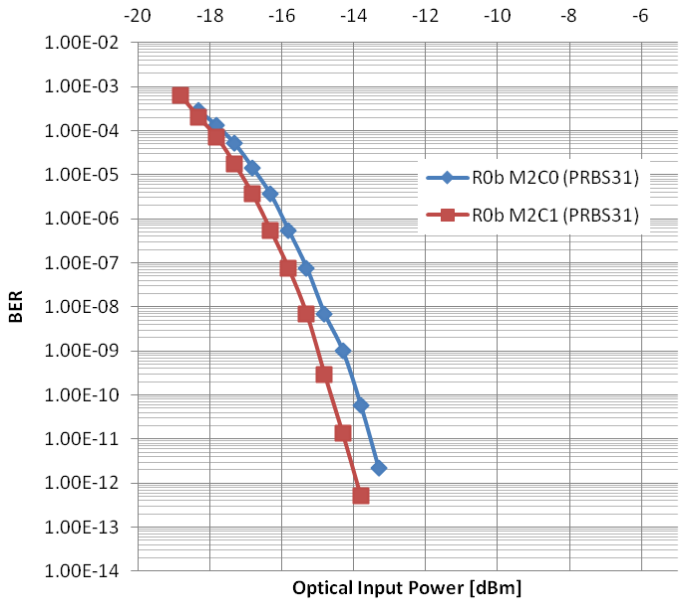
FMC SERDES

optical transmission at 10Gbps on FMC MGTs using Faster Technology FM-S18 and SFP+ in loopback with variable attenuator

running IBERT test in loopback

initial testing (850nm MM) indicates that the carrier does not degrade performance of optical transceiver (<-11.1dBm)

need more work to define a systematic test stand (well characterised reference FMCs, SFP+s and carriers)



batch #1: performance testing

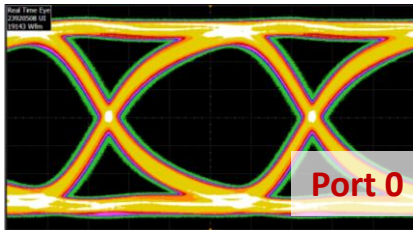
backplane SERDES

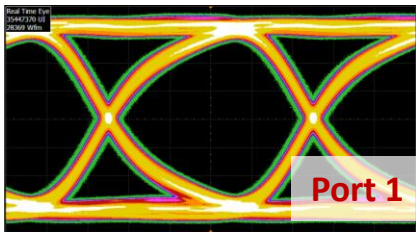
electrical transmission at 5Gbps on AMC MGTs using SMA Ultra-9000 and in the crate with the AMC13XG

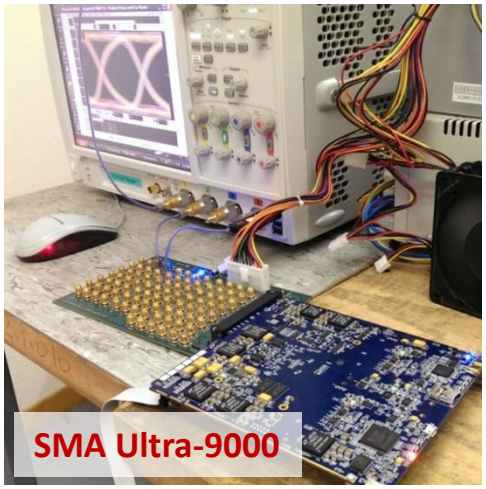
excellent eyes at 5Gbps (~**46ps jitter**)

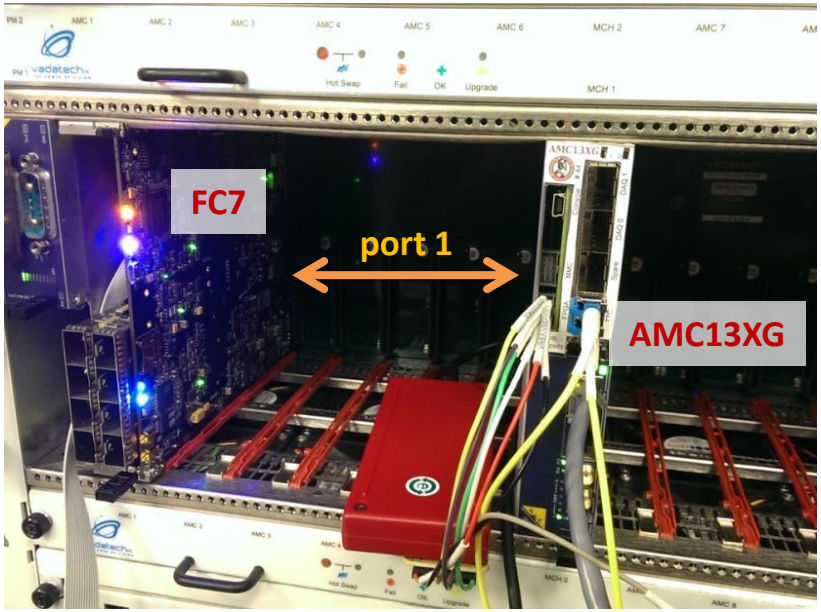
test of Port 1 (CMS DAQ link) between **FC7 and AMC13XG** using IBERT bit tests using PRBS-31 – **no errors in >10^{13} bits**

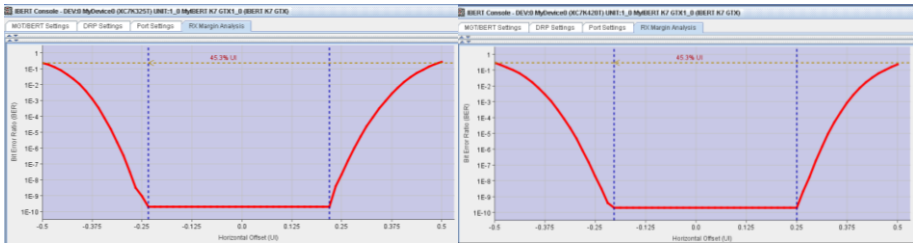
RX bathtub curves on both AMC13 and FC7 on Port 1 **0.45UI open**











mature version of f/w for basic board control available

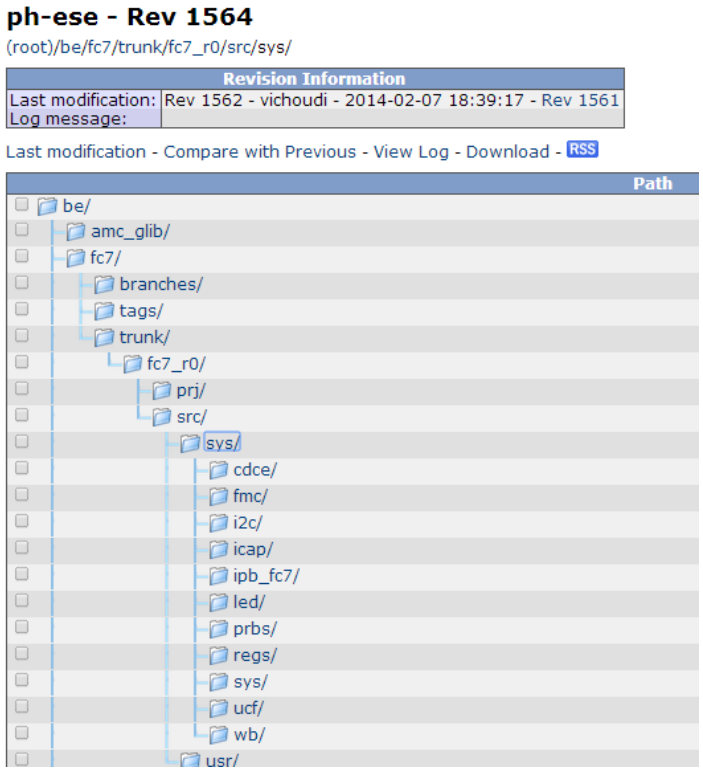
- very similar in structure & content to GLIB f/w

-separate user (custom) and system (IPbus & register space, clock & peripherals control) spaces

- available on SVN, much more to come (DDR3, clock control, firmware loading…)

software for basic board control available

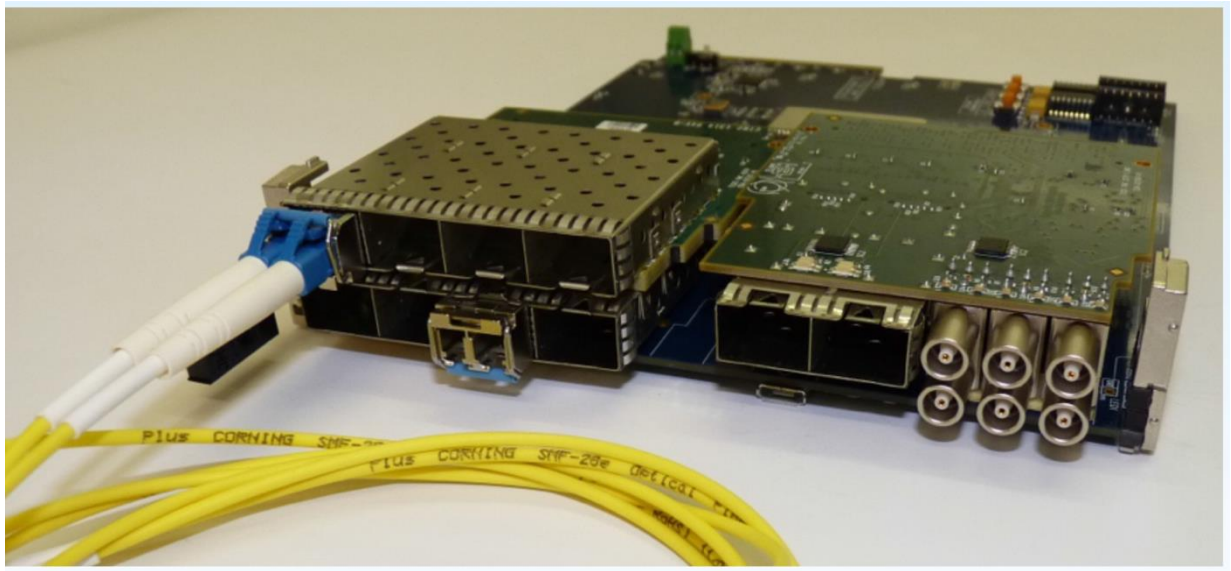
https://svnweb.cern.ch/cern/wsvn/ph-ese/be/fc7



First FC7 application: TCDS

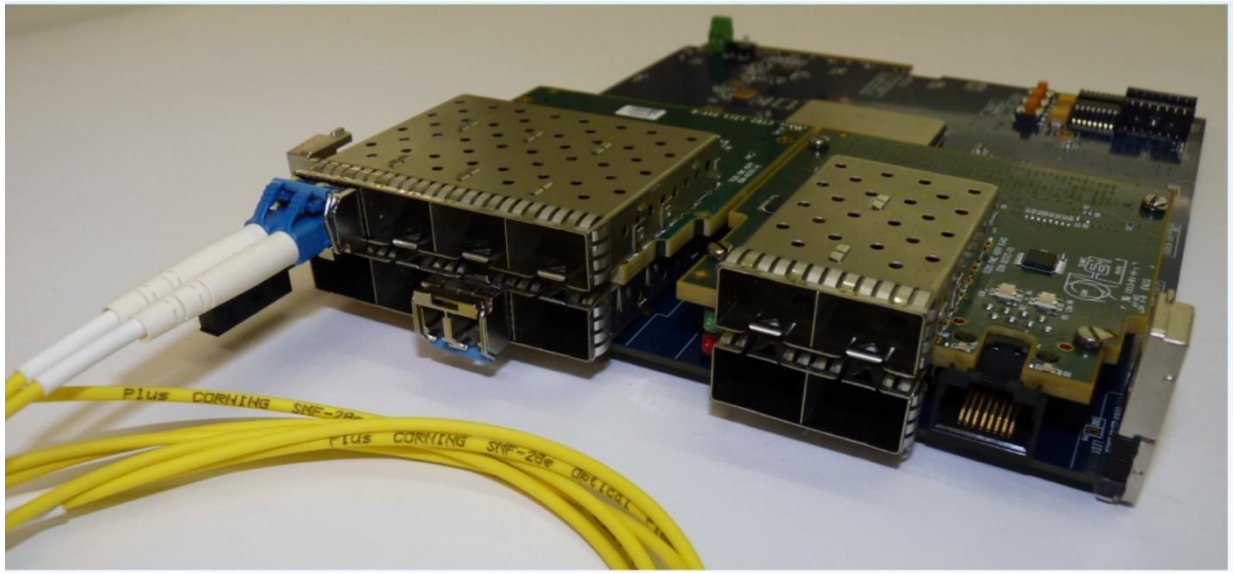
Local Partition Manager (LPM)

- 2x 10Gb/s <-> DAQ
- 8x TTC/TTS <-> TCDS fanout (PI)
- Backplane <-> AMC13



Partition Interface (PI)

- 2x TTC/TTS <-> LPM
- 10x TTC/TTS <-> FEDs
- RJ45 TTS <-> Legacy systems



summary

CMS (CERN/IC) board, merge between MP7 & GLIB

Dual LPC FMC carrier

- w/ additional SERDES as in HPC

Successful preproduction

Mature FPGA firmware

First application (TCDS) already launched production

More to come!