

Pixel 2014 - Niagara Falls, Canada

Pixel detector (sensors) for the CMS phase-II upgrade

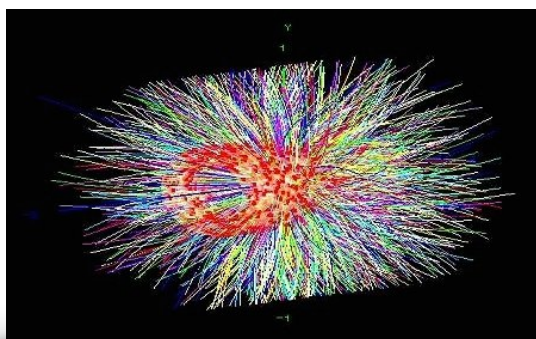
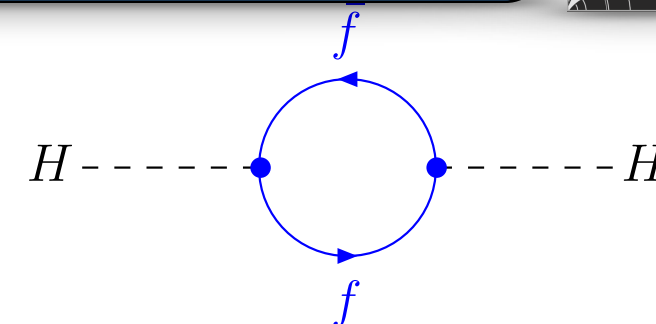


Mauro Dinardo

Università degli Studi di Milano Bicocca and INFN, Italy

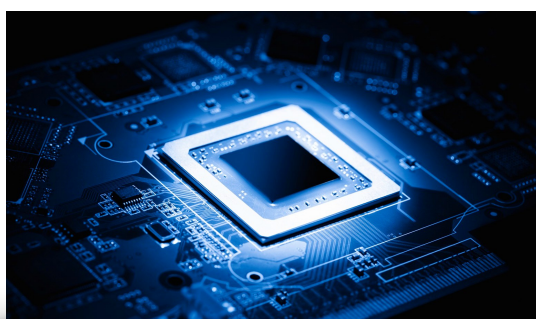
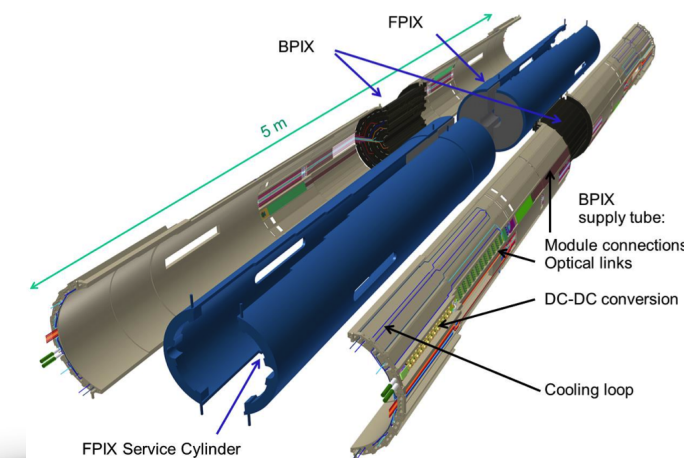
On behalf of the CMS collaboration

- CMS pixel phase-II upgrade motivations



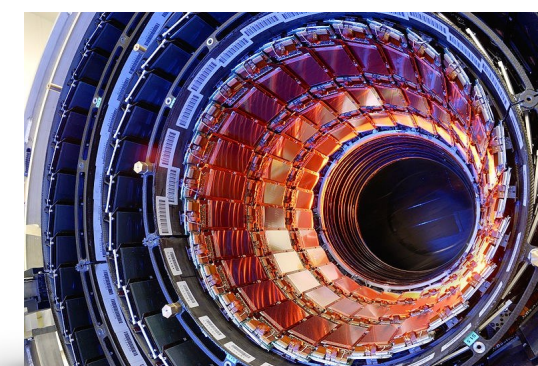
- Detector operating conditions

- Detector layout choices



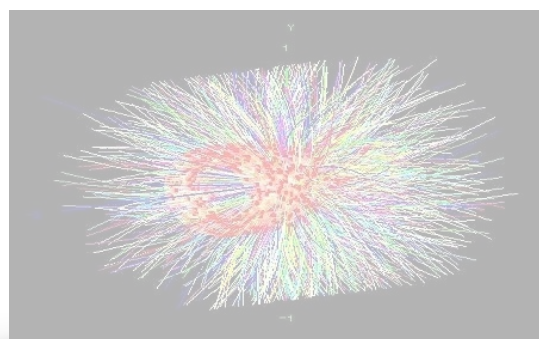
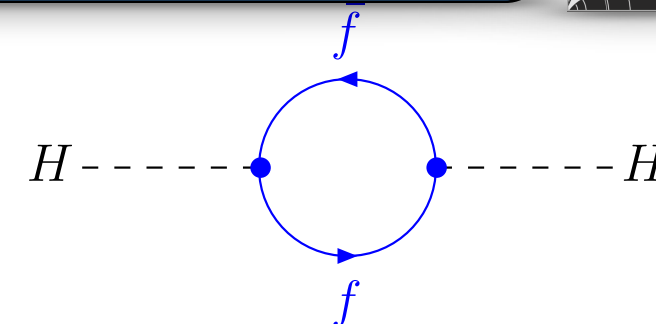
- Readout chip specifications

- Possible sensor choices

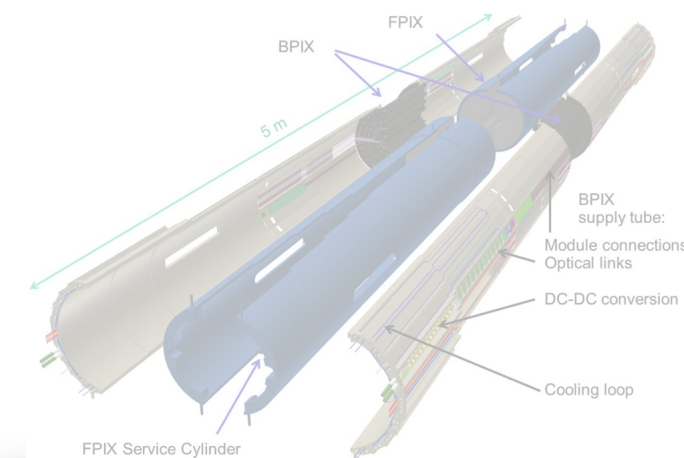


- Conclusions

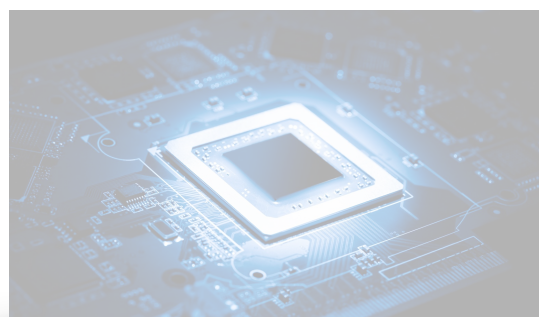
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- Detector operating conditions

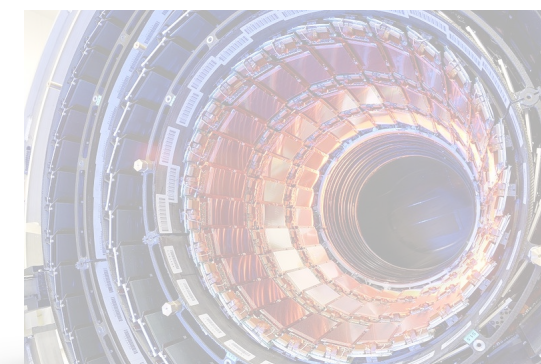


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Major achievement of LHC: Higgs discovery in 2012 !

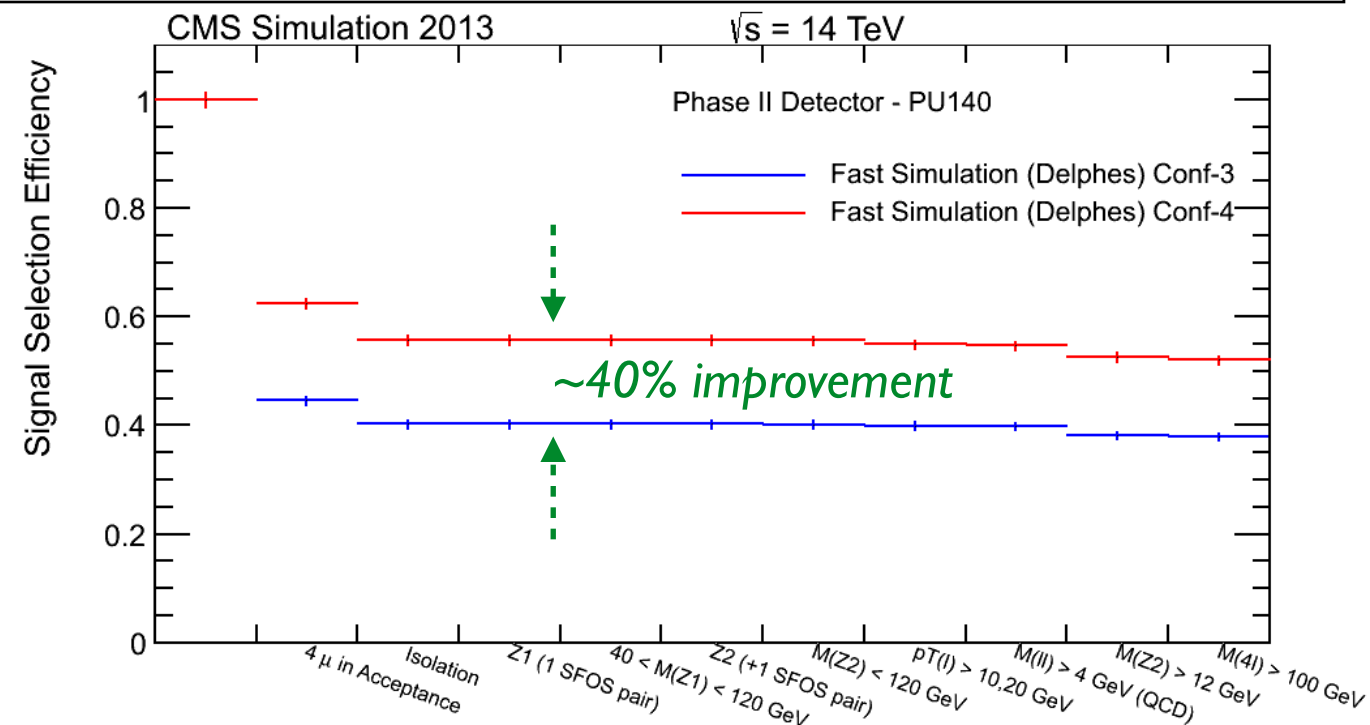
That's not the whole story, there are other questions that need to be answered

- Need to investigate the entire Higgs sector
 - Higgs coupling and property measurements
 - Di-Higgs searches with the aim of Higgs self coupling measurement
 - Vector Boson Scattering (VBS) measurements (*crucial forward tagging jets*)
- Standard Model (SM) measurements
 - Precision measurements (*e.g. m_W , $\sin\theta_W$, α_s*)
 - Search for rare SM processes, enhanced by BSM (*e.g. $B_{s,d} \rightarrow \mu\mu$*)
 - Differential measurements of W, Z, di-boson, Top

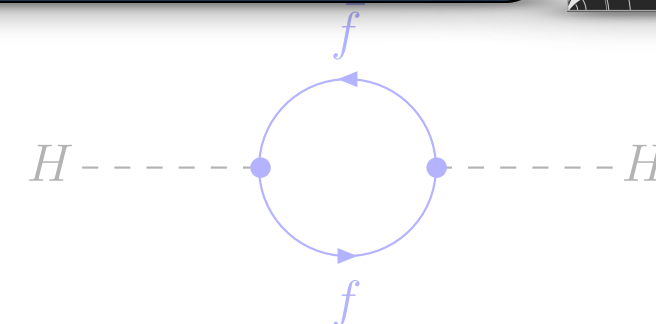
All these measurements require a lot of data

Efficiency cut flow for $H \rightarrow ZZ \rightarrow \mu\mu\mu\mu$

- **Conf-3:** sub-detectors have same **angular acceptance** as **current version**, but central tracking detector and the forward electromagnetic calorimeters are replaced and improved
- **Conf-4:** tracking, electromagnetic and hadronic calorimetry, and muon detector, are **increased in acceptance up to $\eta \approx 4$**

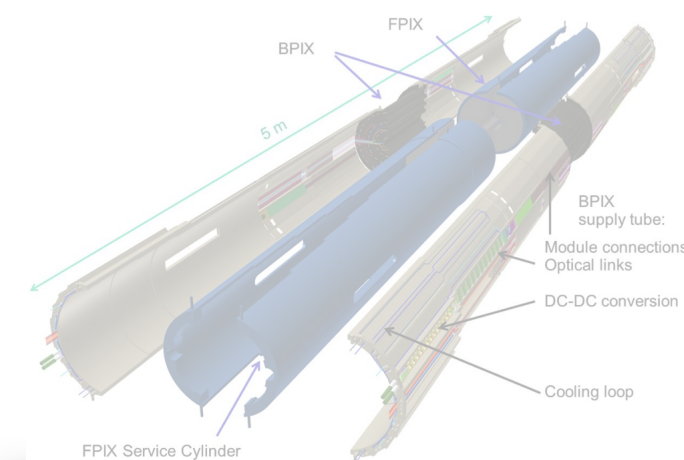


- CMS pixel phase-II upgrade motivations



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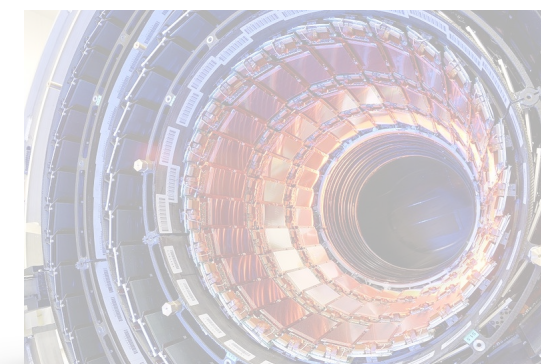
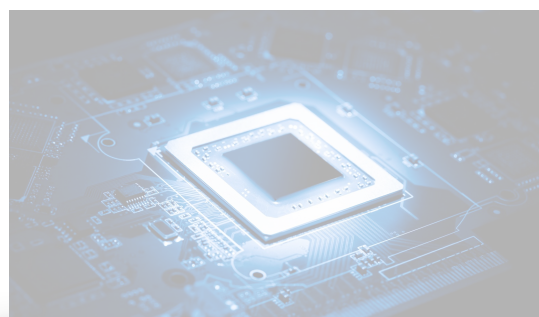
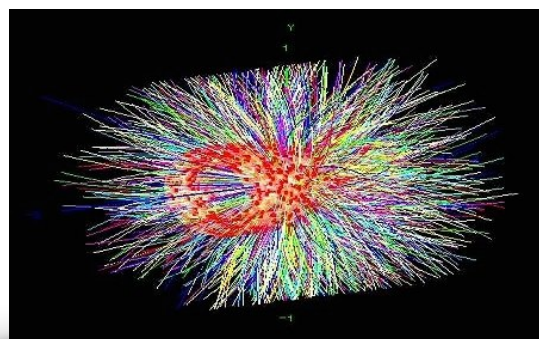
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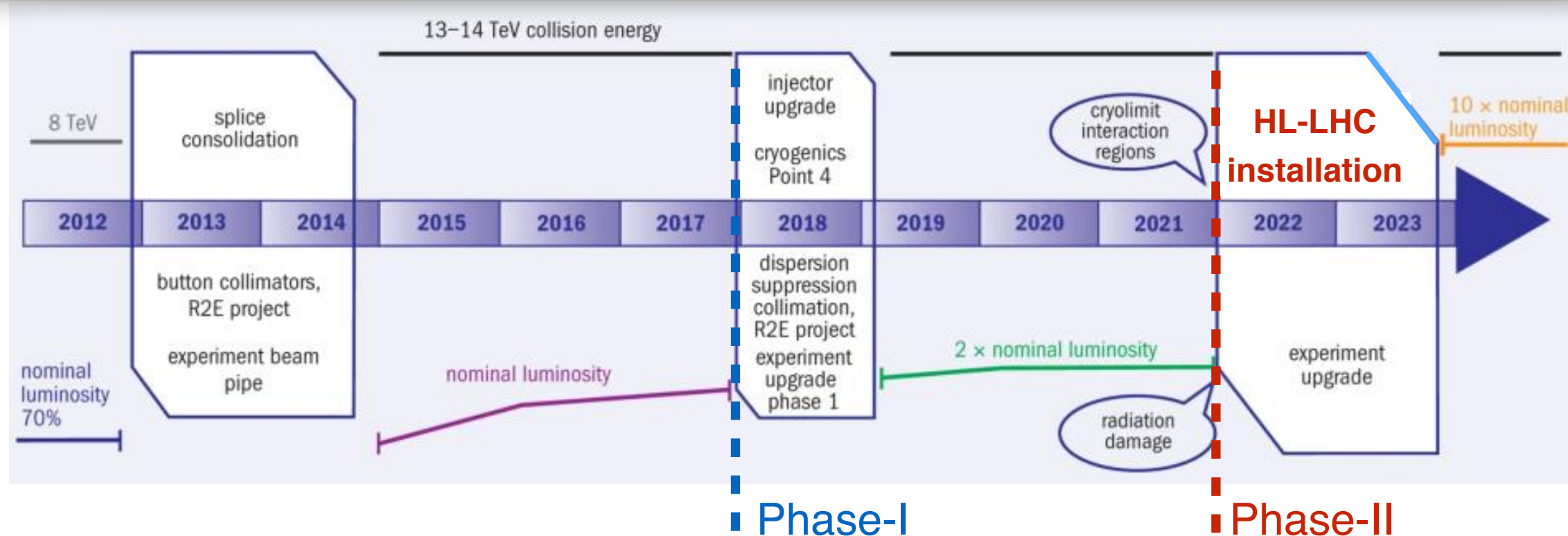
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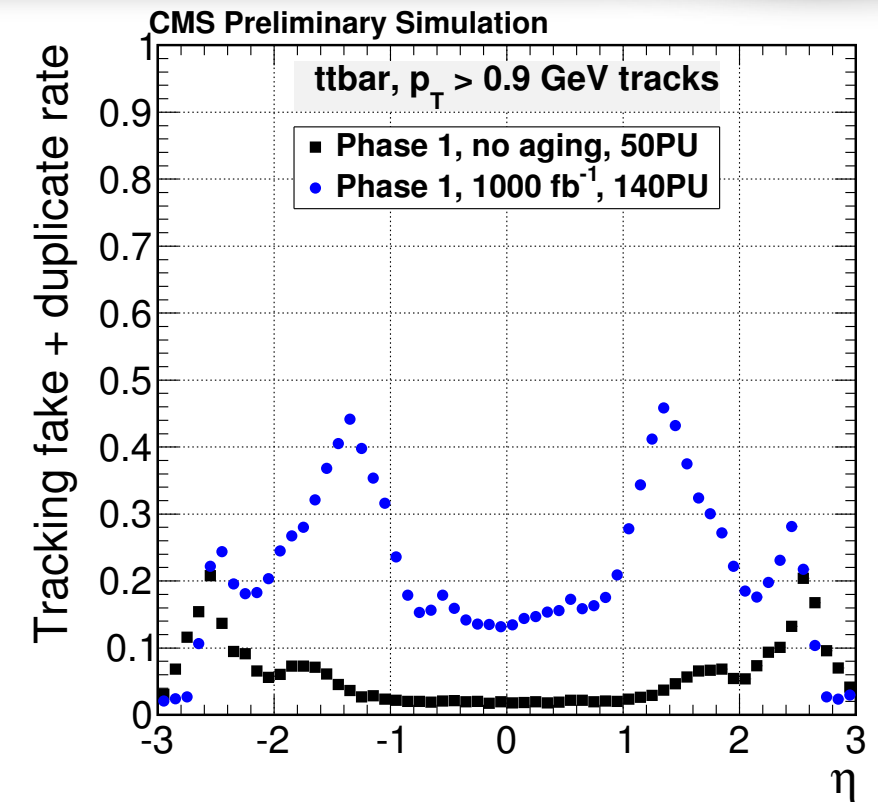
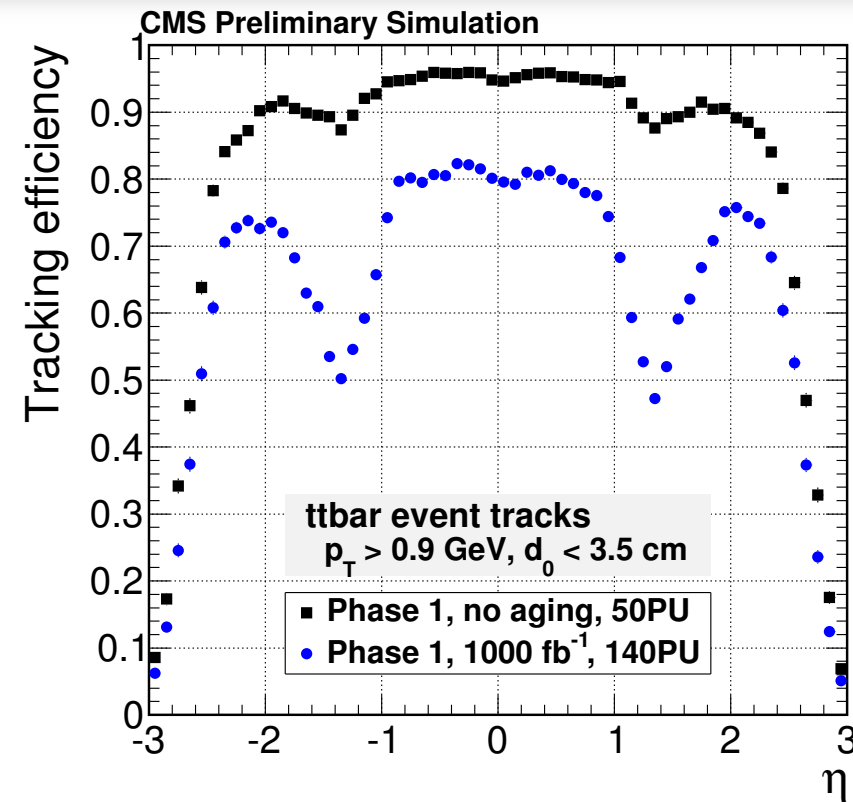
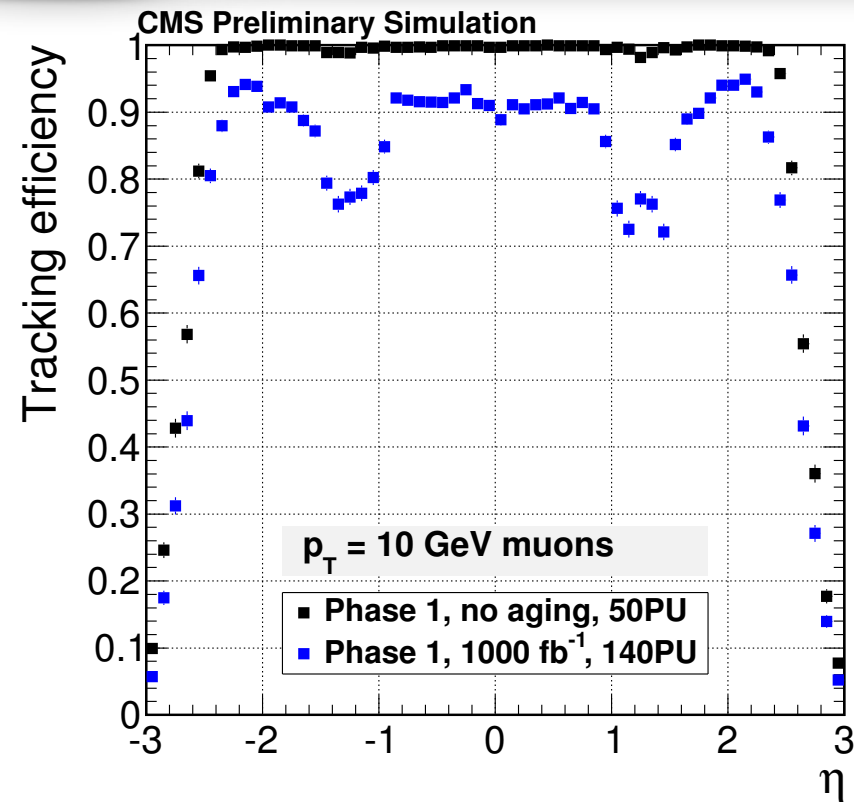
Pixel detector operating conditions



High Luminosity (HL) - LHC: upgrade damaged low- β triplets and install crab-cavities to optimise bunch overlap

- Energy = 14 TeV
- $L_{\text{inst}} = 5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ ($\rightarrow \sim 10$ times now)
- $L_y = \sim 300 \text{ fb}^{-1} / \text{year}$ ($L_{\text{total}} \sim \mathbf{3000 \text{ fb}^{-1}}$ in 10 years)
- 25 ns bunch spacing
- $\langle \text{PileUp} \rangle = \mathbf{140}$ (\rightarrow now 25)
- Radiation @30 mm from IP: $\mathbf{2 \times 10^{16} \text{ n}_{\text{eq}} / \text{cm}^2}$ ($\rightarrow \sim 10$ times phase-I)
- Dose @30 mm from IP: $\mathbf{10 \text{ MGy}}$ (1 Grad)
- Hit rate: $\sim \mathbf{2 \text{ GHz}} / \text{cm}^2$ ($\rightarrow \sim 10\text{-}20$ times now)

Huge R&D is required to cope with harsh environment



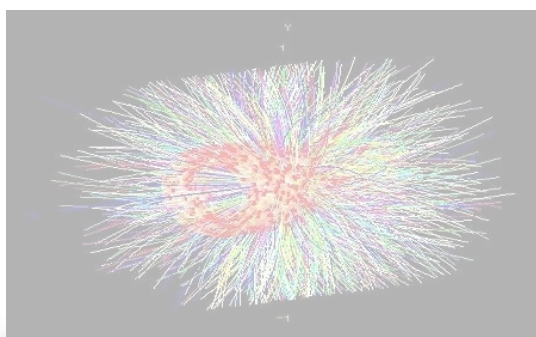
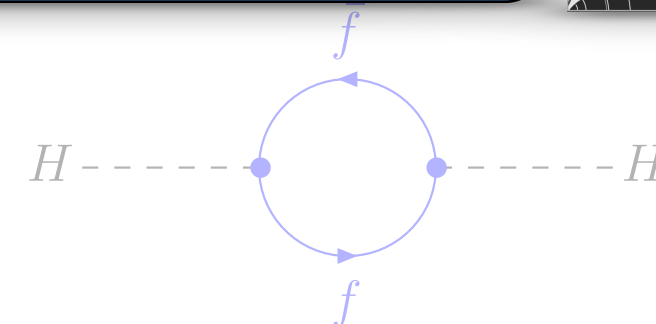
Overall tracking performance degradation with ageing

- After 500 fb^{-1} **impact parameter** degradation of more than **50%**
- $\langle \text{PU} \rangle = 140$ imply an irreducible **data loss** of $\sim 7\%$

Effects on the physics program

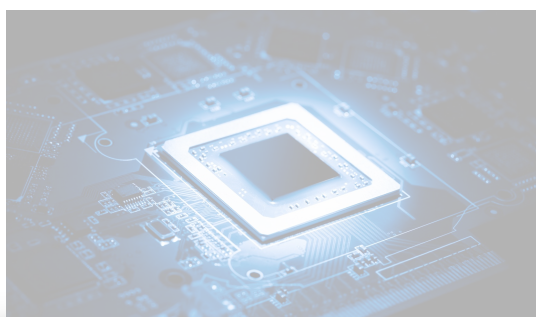
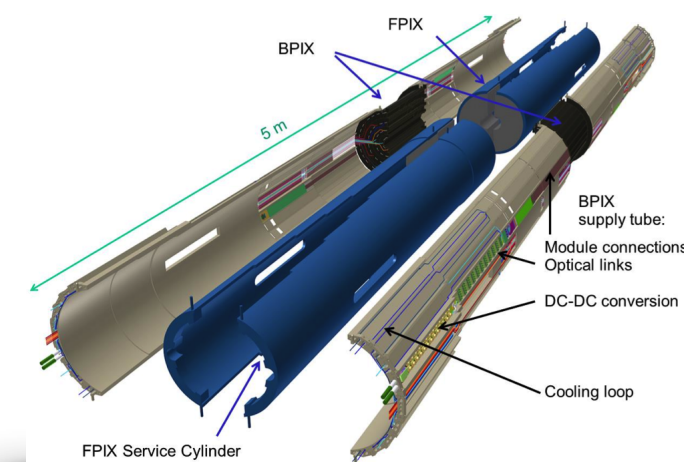
- Efficiency loss diminishes effectiveness of high- p_T lepton isolation, and degrades jet energy and missing transverse energy resolutions
- Fake tracks causes biases and resolution degradation in jet energy measurements, increases background levels, and adversely affects high- p_T lepton isolation criteria

- CMS pixel phase-II upgrade motivations



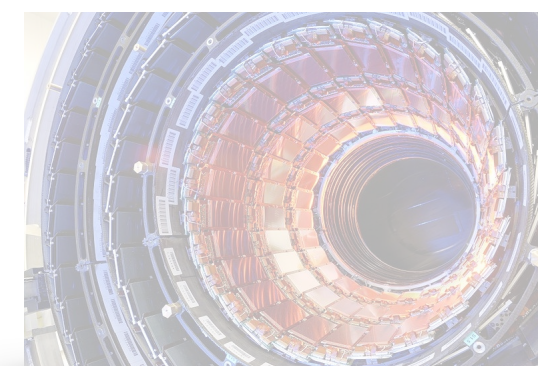
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- Readout chip specifications

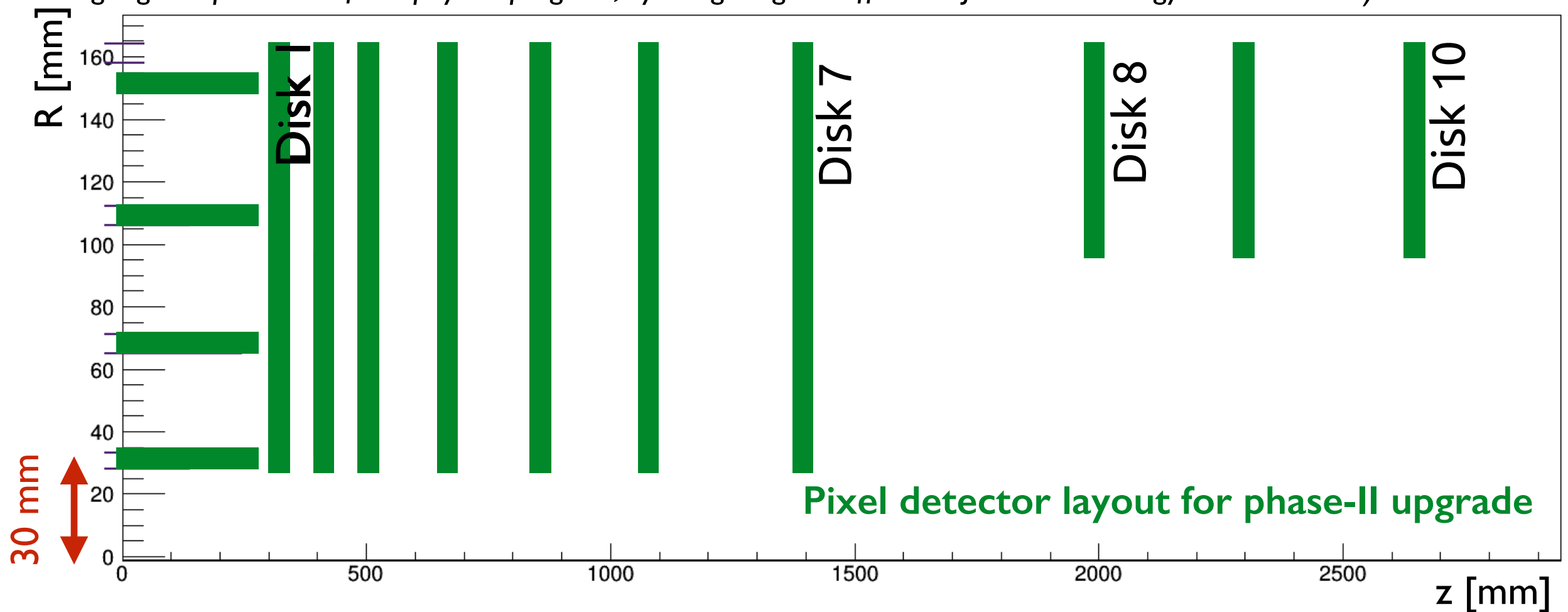
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Pixel detector layout for phase-II upgrade

- Improve resolution at high- p_T and improve two-track separation → increase granularity (*present tracker has degraded track finding performance in high-energy jets due to hit merging in the pixel detector*)
- Improve resolution at low- p_T and reduce secondary interactions → reduce material
- Increase forward acceptance (*to cover peak production region of jets from Vector Boson Fusion and VBS, among highest priorities of the physics program, by mitigating PU effects in jet-ID and energy measurement*)



4 barrel layers (→ 3 layers now)

10+10 forward disks, coverage up to $\eta \approx 4$ (→ 2+2 disks now, up to $\eta \approx 2.4$)

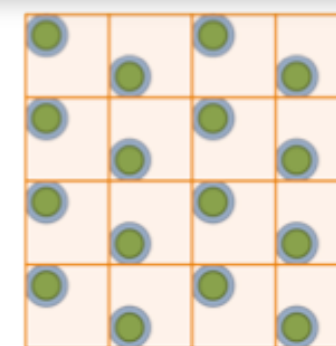
Preserve the ease-of-access of current detector (*possibility to replace degraded parts over technical stops*)

Readout chip

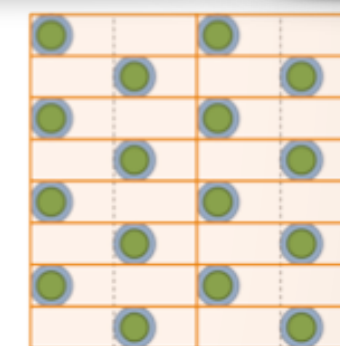
- Candidate technology: **65 nm CMOS** (*RD-53 cross collaboration Atlas-CMS for development*)
- Cell size: **50x50 μm^2** or **25x100 μm^2** (*aim large chip $\sim 20 \times 20 \text{ mm}^2$*)
- Staggered bumps:
 - possibility to switch off 1/2 or 3/4 pixels (*e.g. outer regions with pixels of 100x100 μm^2 or 50x200 μm^2*)

Sensors

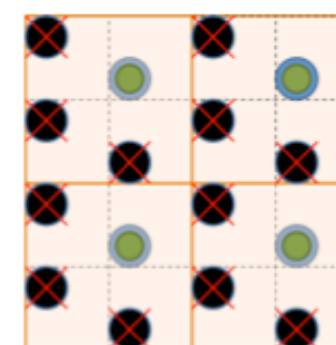
- Favoured technology: **planar Silicon**
 - Define suitable n-in-p process and design (*more cost effective than present n-in-n because single sided process*)
 - Thin thickness
 - Requires robust spark rejection material
- Alternative/complementary for innermost layer: **3D Silicon**
 - Define suitable number of electrode columns
 - Define suitable electrode geometry and sensor thickness
 - Address production issues (*e.g. yield and cost*)



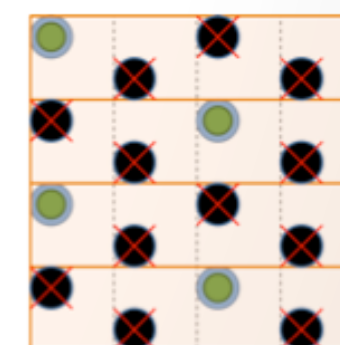
50x50 μm^2



25x100 μm^2



100x100 μm^2



50x200 μm^2



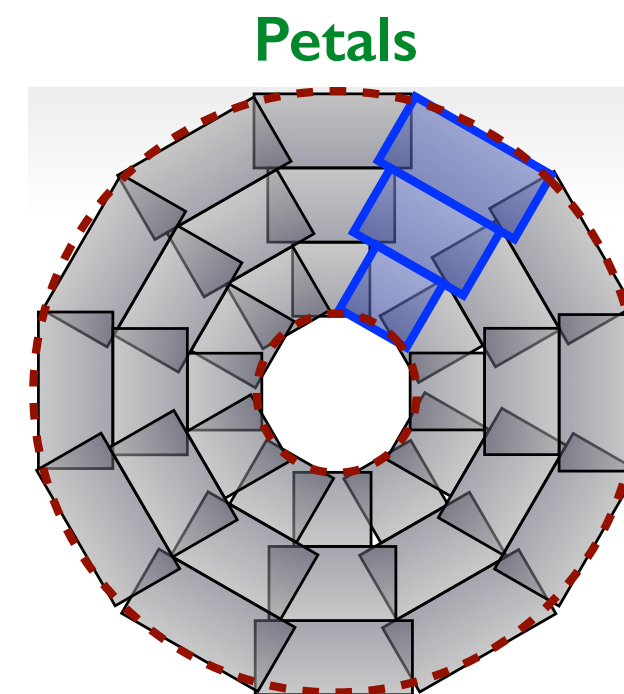
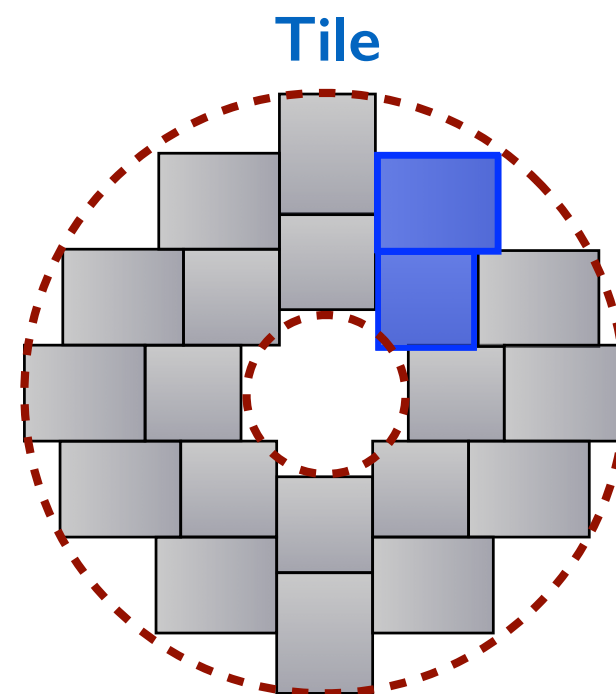
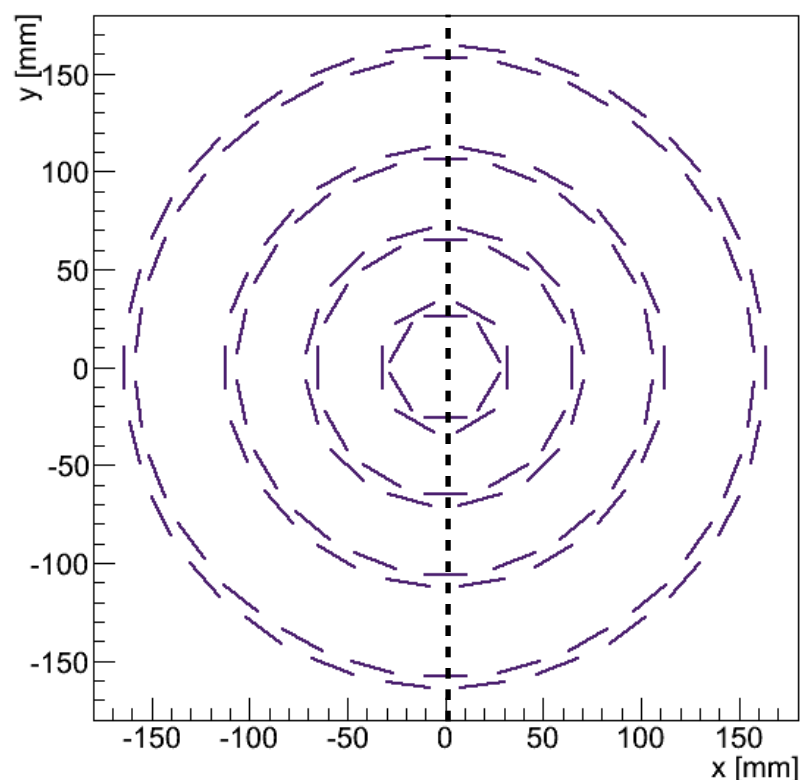
disabled pixel

Total active area: $\sim 4 \text{ m}^2$

($\rightarrow \sim 1.5$ times phase-I)

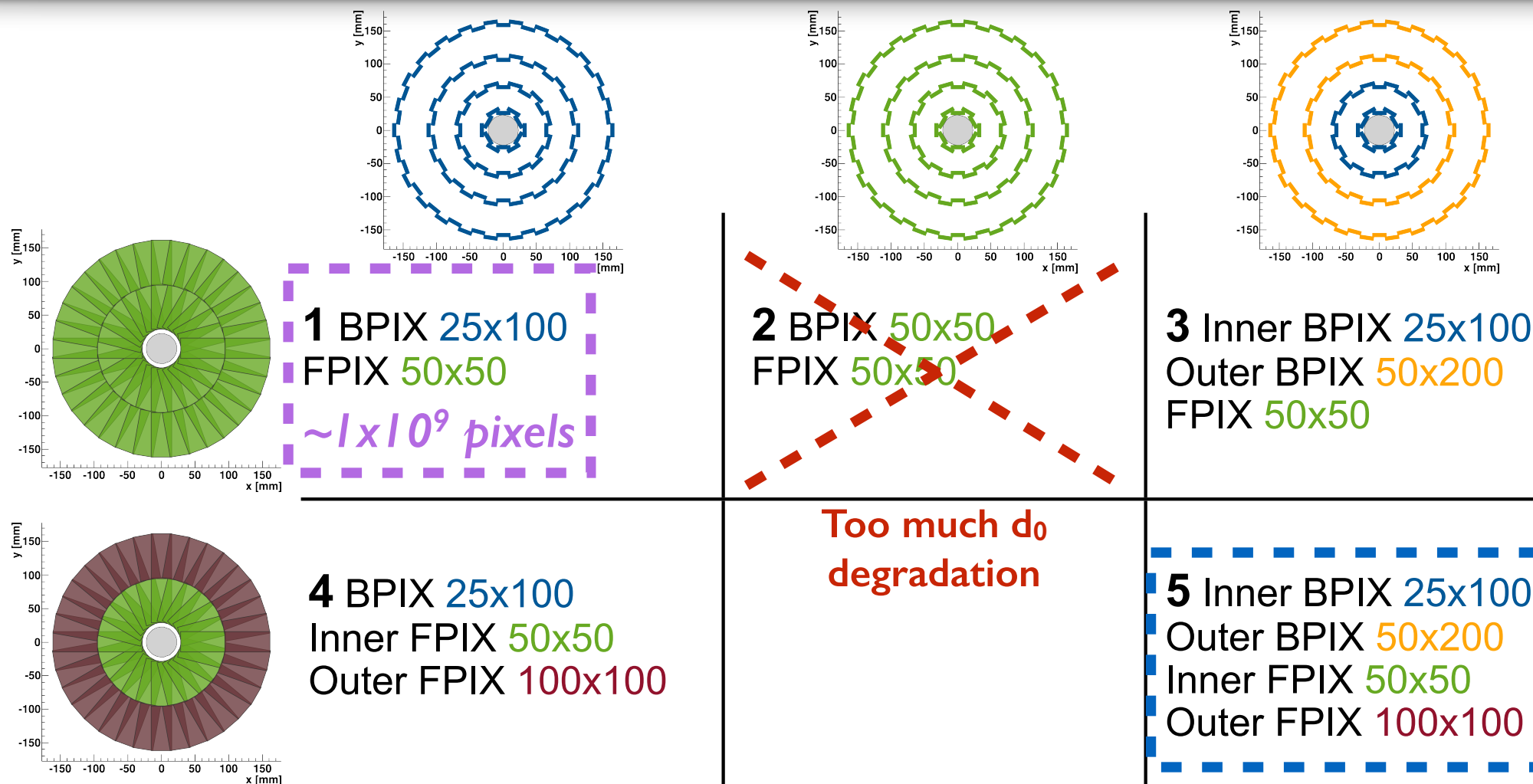
Barrel geometry: two module types with 4x2 or 4x1 chips and no projective hole at $z = 0$

Forward geometry: two possible coverage schemes are being considered



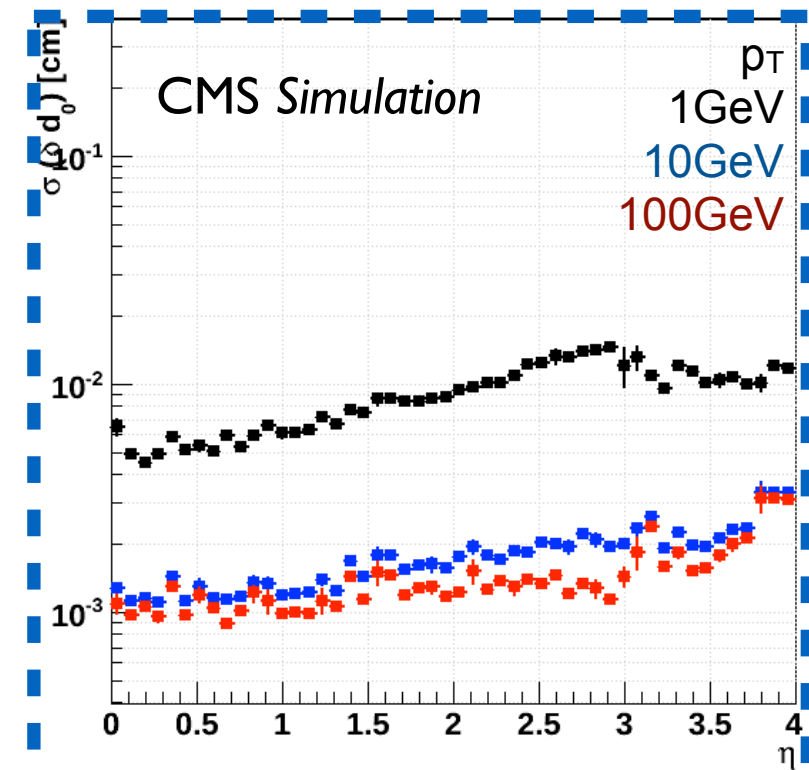
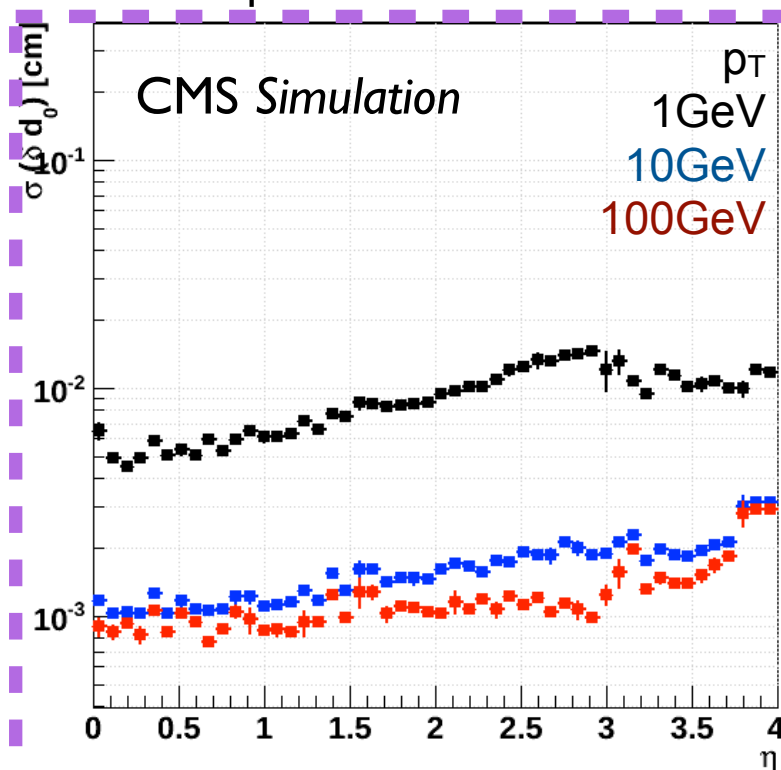
Geometry	Coverage	Overlap	#modules	#chips
Tile	89%	12%	26	160
Petals	98%	45%	44	232

- Numbers are per disk
- Tile modules 4x2, 4x1, 2x2
- Petals modules 4x2, 2x1
- Chip size 21x23 mm² active area

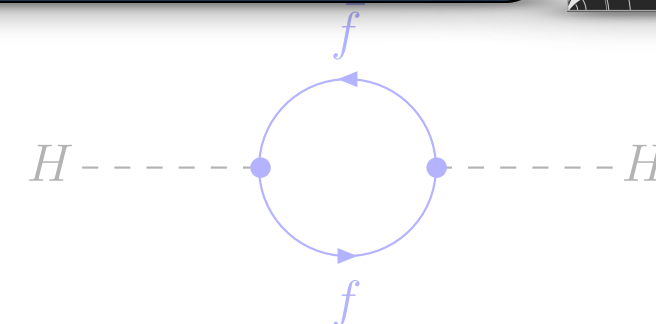


Pixel cell size studies

- Too much d_0 degradation with pure squared pixels in BPIX
- Two extreme configurations, **#1** and **#5**, have comparable tracking performance
- Configuration **#5** has $\sim 1/2$ channels of **#1**

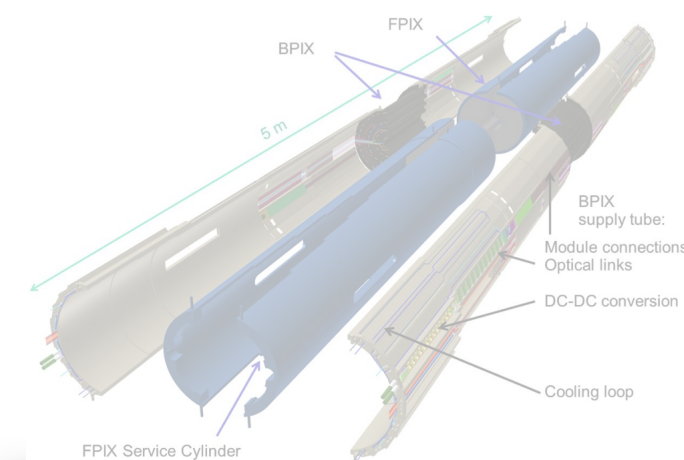


- CMS pixel phase-II upgrade motivations



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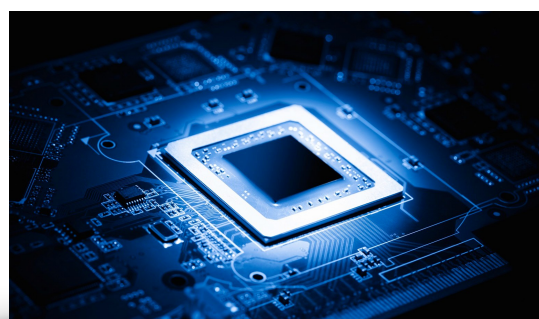
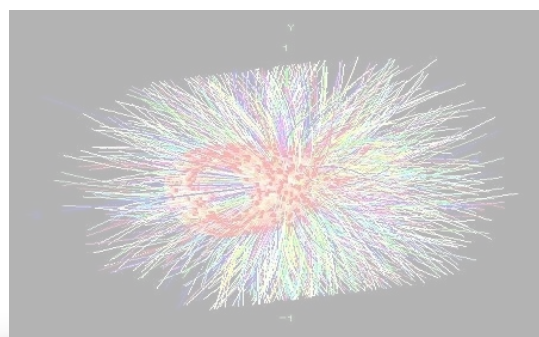
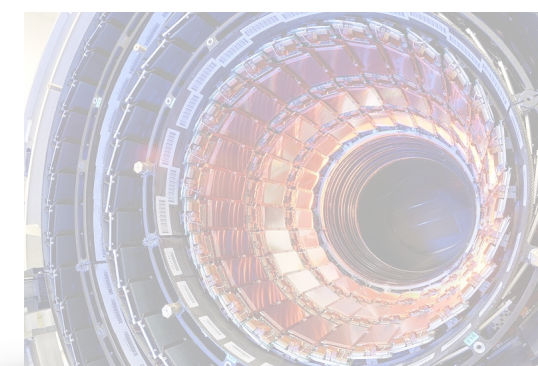
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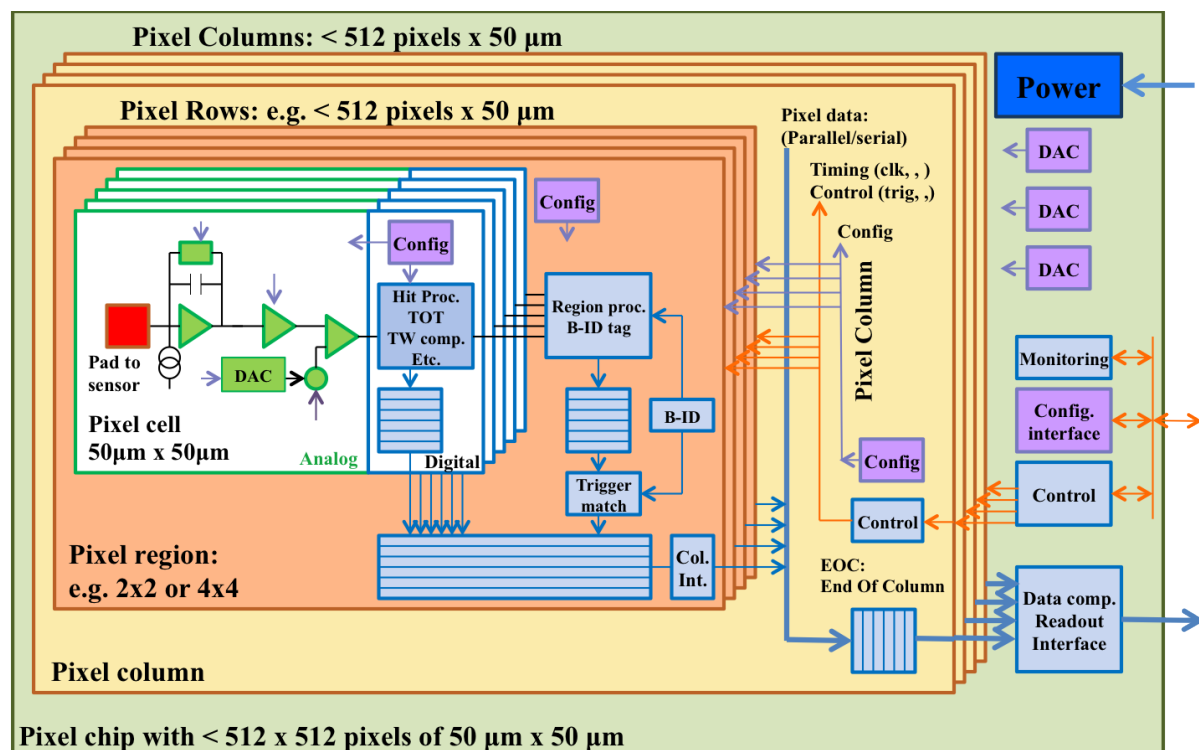
Extremely challenging requirements

Generation	Present	Phase-I	Phase-II
Pixel size	100x150 μm^2	100x150 μm^2	50x50 (25x100) μm^2
Sensor	2D, 300 μm	2D, 300 μm	thin 2D, 3D
Chip size	8x10 mm^2	8x10 mm^2	> 20x20 mm^2
Transistors	1.3x10 ⁶	?	~10⁹
Hit rate	100 MHz / cm^2	400 MHz / cm^2	~2 GHz / cm^2
Hit memory per chip	0.1 Mb	1 Mb	~16 Mb
Trigger rate	100 kHz	100 kHz	~1-2 MHz
Trigger latency	3.2 μs	3.2 μs	~12 μs
Readout rate	40 Mb/s	400 Mb/s	~2 Gb/s
Radiation	15 Mrad, $r = 42 \text{ mm}$, $L = 150 \text{ fb}^{-1}$	120 Mrad, $r = 29 \text{ mm}$, $L = 500 \text{ fb}^{-1}$	1 Grad, $r = 30 \text{ mm}$, $L = 3000 \text{ fb}^{-1}$
Technology	250 nm	250 nm	65 nm
Architecture	Analog	Digital	Digital
Buffer location	End Of Column	End Of Column	Pixel
Power	~0.15 W / cm^2	~0.15 W / cm^2	~0.3 - 0.5 W / cm^2

See talk from Maurice GARCIA-SCIVERES: "RD-53 Progress on High Rate Pixel Readout chip"

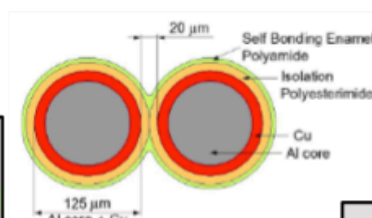
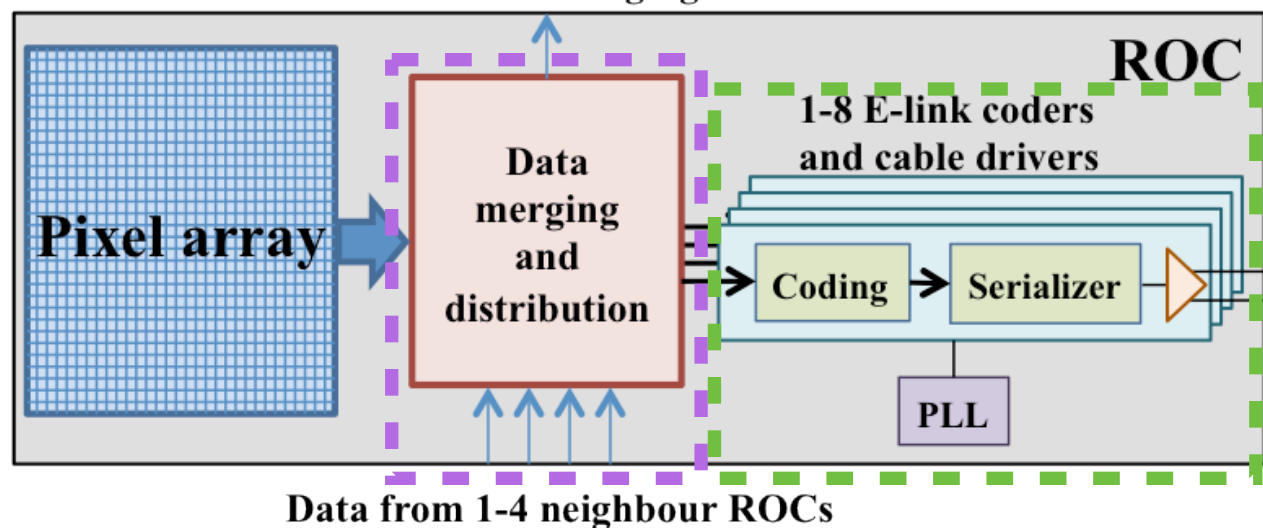
Pixel readout chip and data link specifications

Readout chip architecture



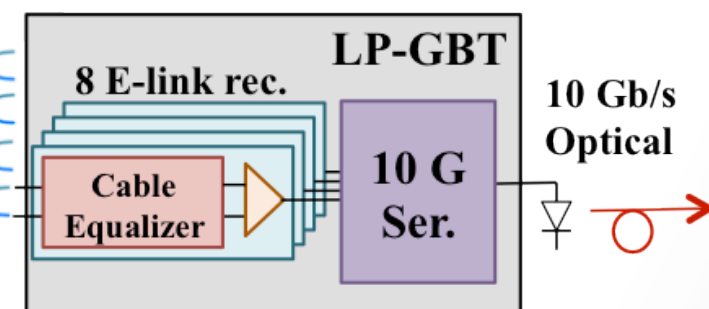
- Possibility to tune bias currents of analogue front-end to account for different sensor choices
- Digital hit processing, including trigger latency buffer, implemented in *pixel regions* (e.g. 2x2 or 4x4 pixels) followed by data merging, formatting and readout after the first level trigger accept (*the price of local digital processing is that digital noise injection into the front end must be controlled, and clocks and trigger signals must be distributed throughout the pixel matrix*)

Data to data merging ROC



1.2 Gb/s
Twisted pair
cables ≤ 2 m

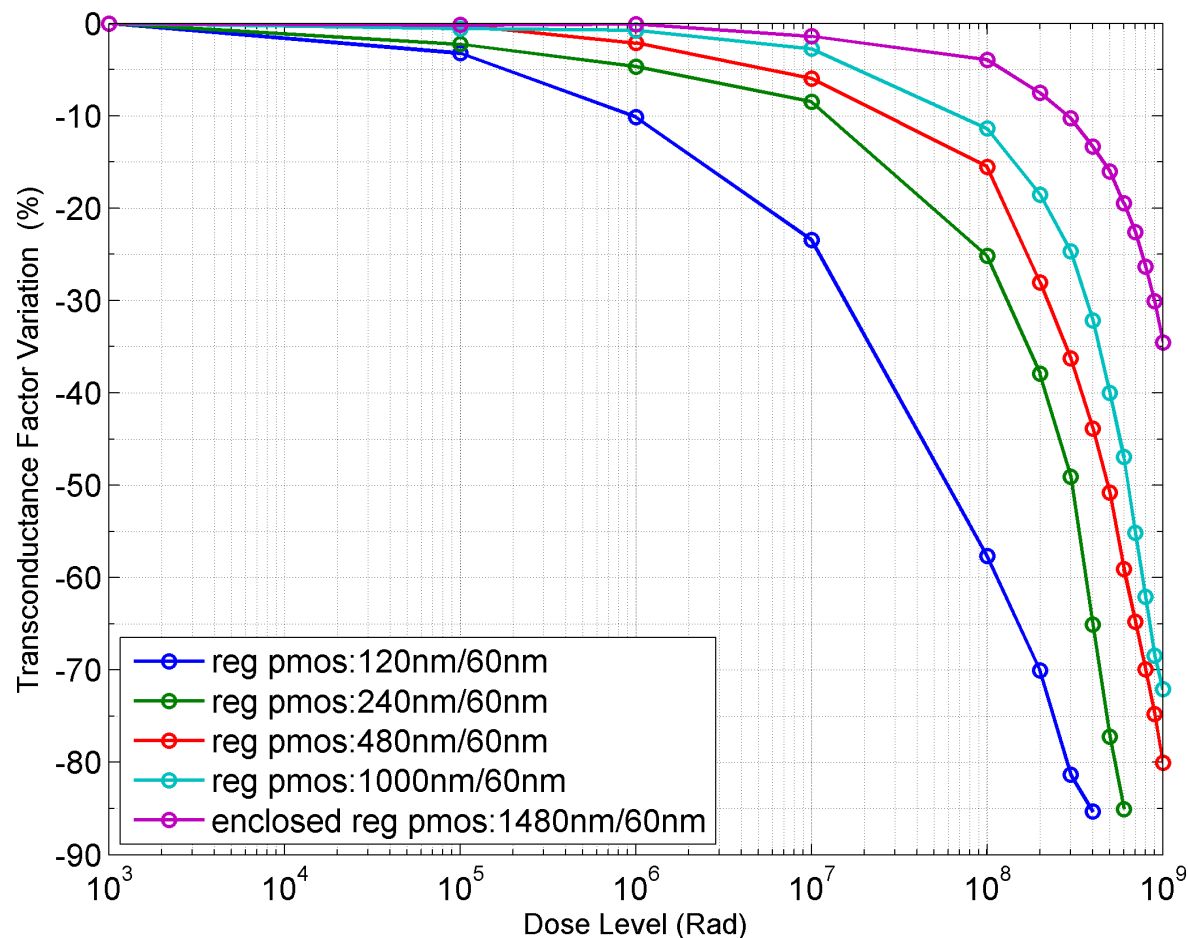
Low Power-GigaBit Transceiver



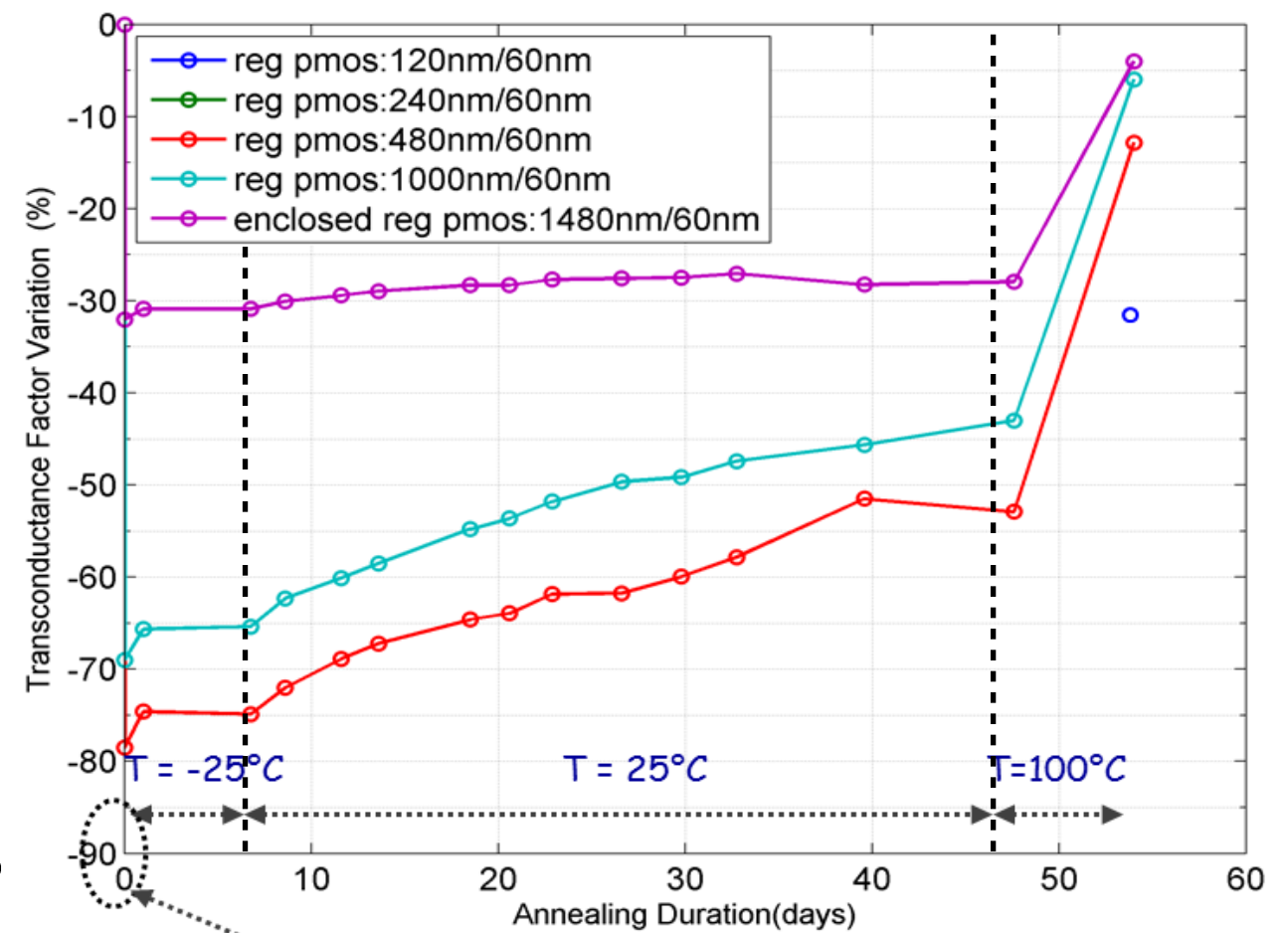
The chip will also implement data merging functionality (from 2 or even 4 chips in the innermost region)

The chip should provide up to 8 data output e-links of 1.3 Gb/s

Transconductance factor variation vs. dose



Transconductance factor variation vs. annealing time

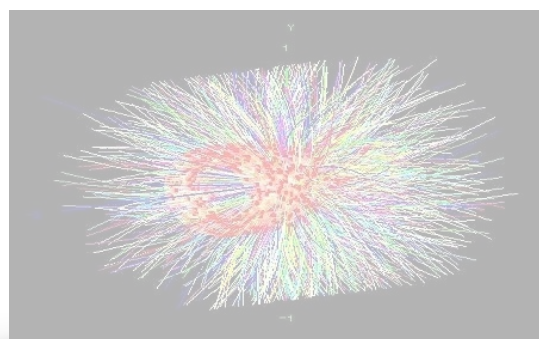
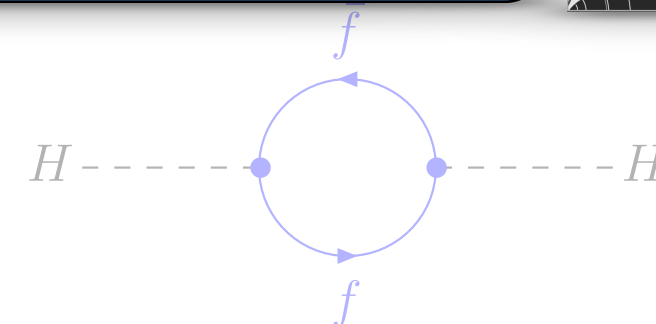


RD-53 collaboration

See talk from Mohsine MENOUNI: "RD53 investigation of CMOS radiation hardness up to 1 Grad"

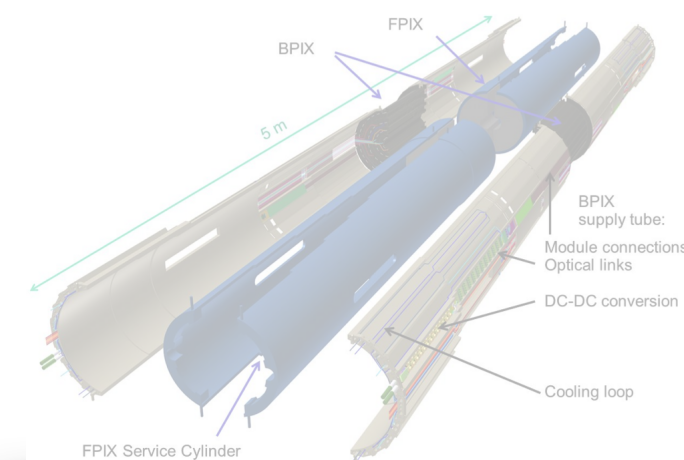
- Among other effects, PMOS-FETs (especially minimum size ones) show **large transconductance degradation vs. dose** (becomes very steep at dose > 100 Mrad)
- Damage mechanisms have yet to be fully understood
- It appears that some of the radiation damage in the chip could be **annealed with high temperatures** → possibly define plausible annealing scenarios during detector maintenance to optimise longevity of sensors and electronics (detailed evaluation of annealing effects on sensor performance)

- CMS pixel phase-II upgrade motivations

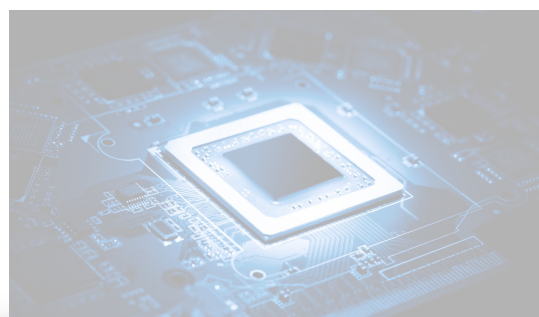


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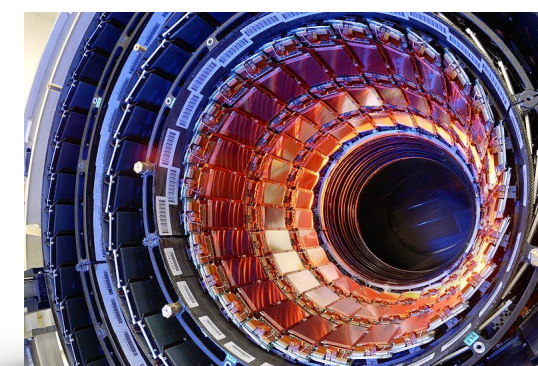
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Planar Silicon n-in-p we need to define

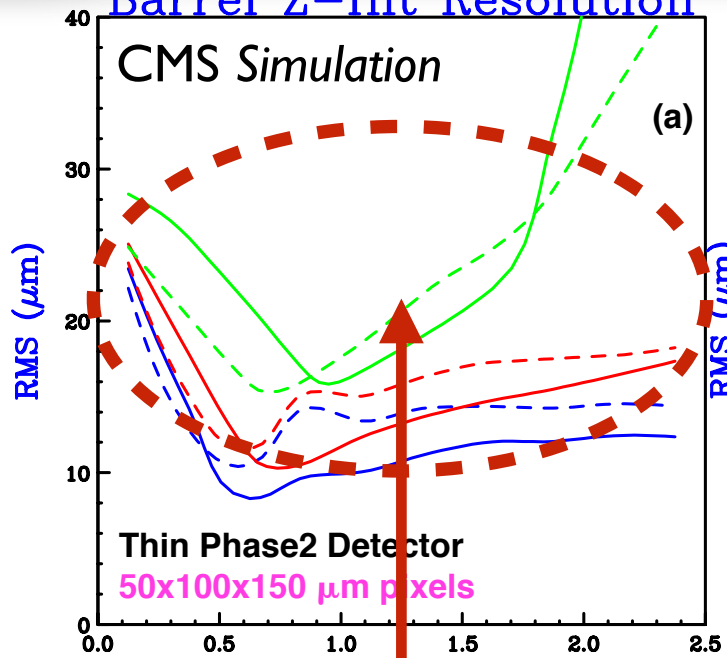
- Sensor thickness
- Sensor process (*FZ, MCz, EPI*)
- Spark rejection material
- Pixel isolation and bias scheme

3D Silicon we need to define

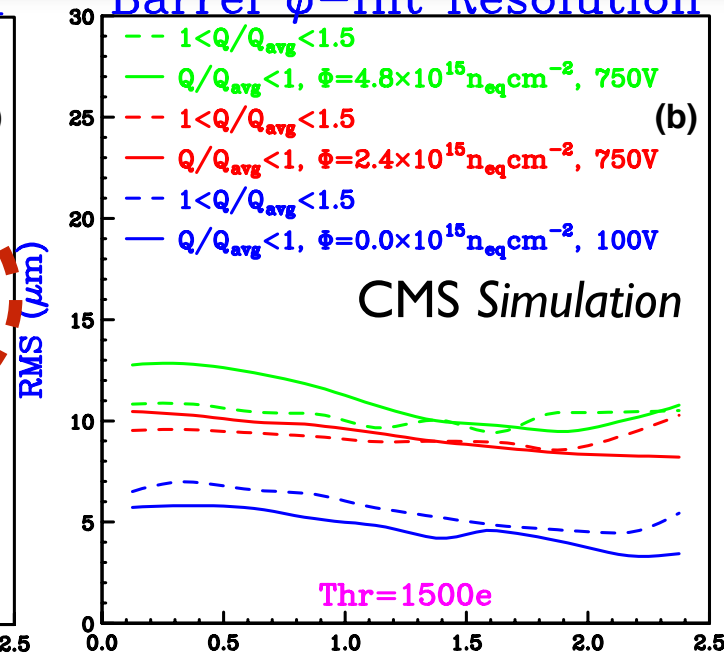
- Number of columns per cell
- Column size → sensor thickness
- Pad position
- Production process: single/double sided

Thin planar Silicon sensors: thin thickness

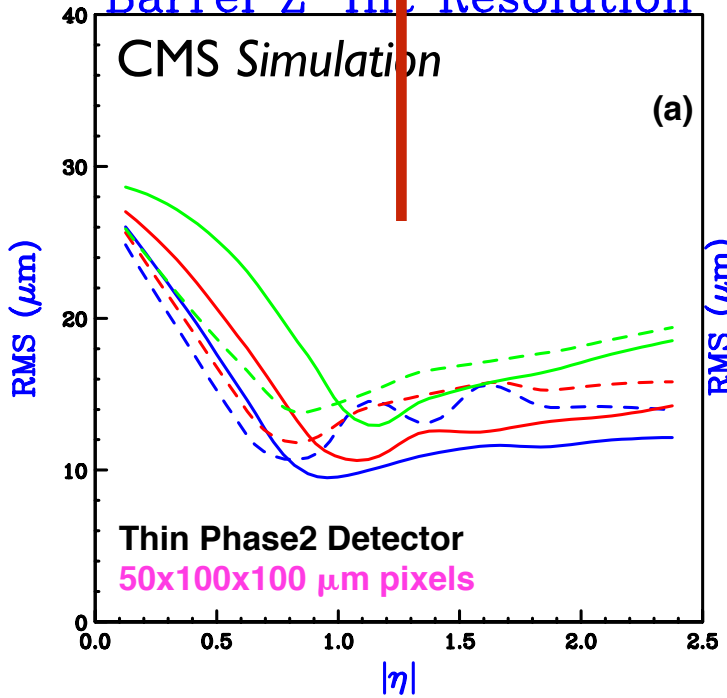
Barrel Z-Hit Resolution



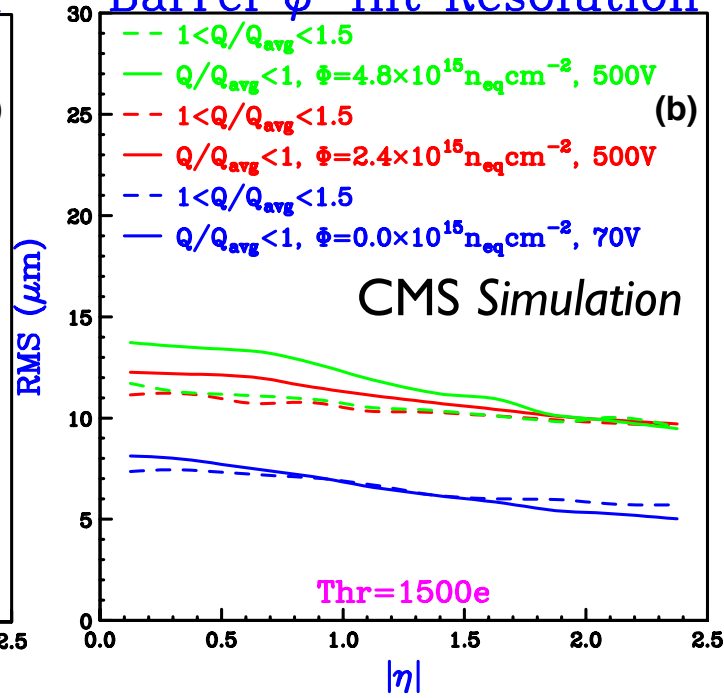
Barrel ϕ -Hit Resolution



Barrel Z-Hit Resolution



Barrel ϕ -Hit Resolution



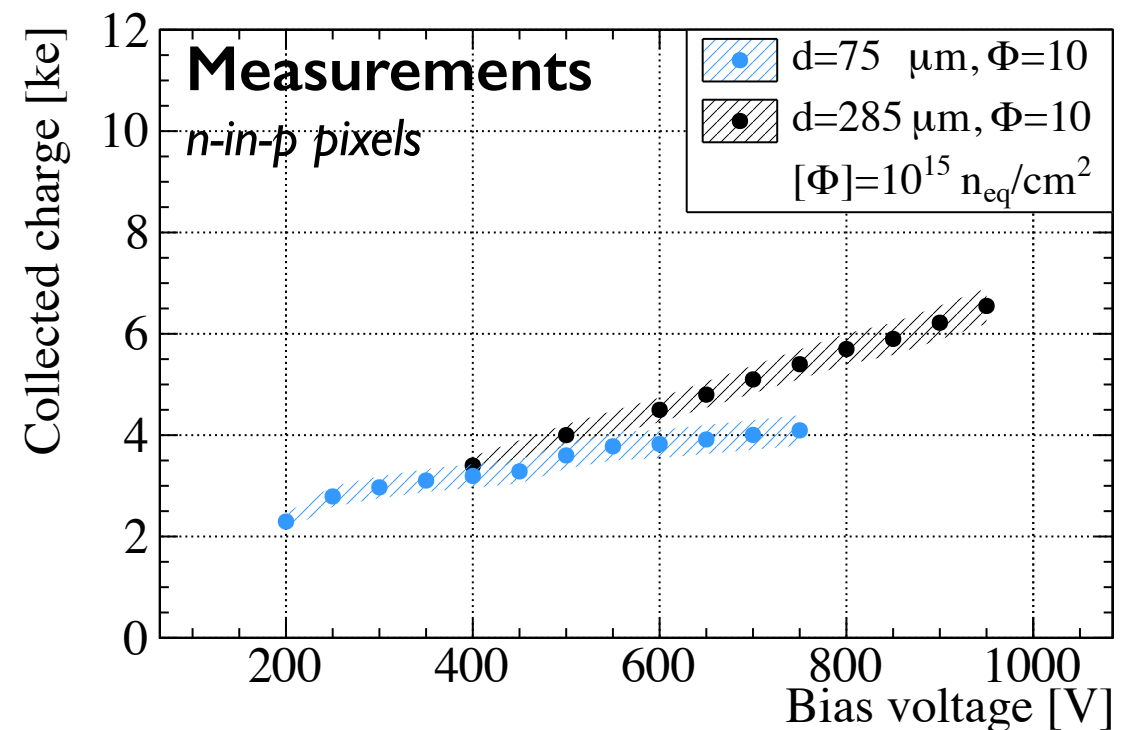
Assumptions

- Noise 150 e^- and other readout and calibration effects are small
- Extrapolate DOFZ irradiated Silicon model, tuned on data up to $1.2 \times 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2$, to larger fluence, $4.8 \times 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2$
- Average E-fields of 50 kV / cm can be achieved

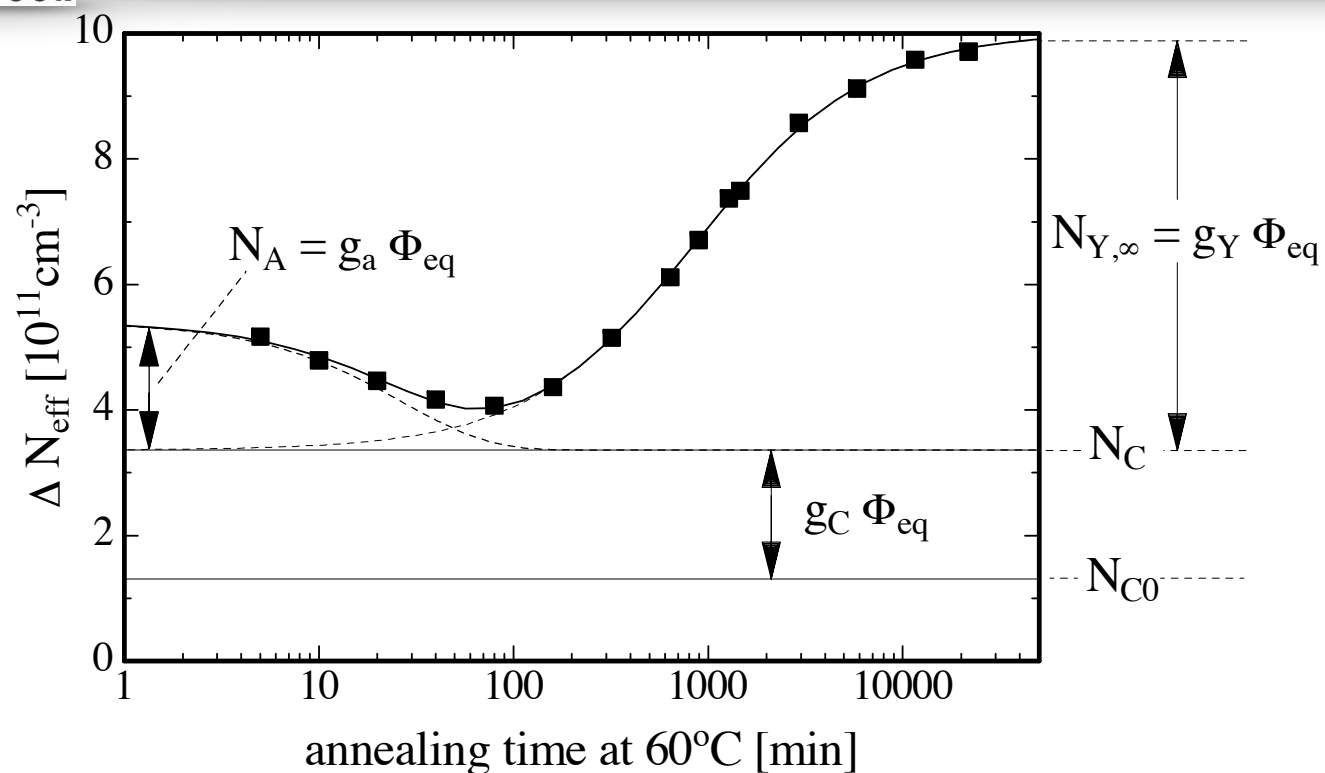
Thin planar sensors advantages

- Higher fields with same bias \rightarrow shorter drift time \rightarrow less trapping \rightarrow ultimately, better radiation hardness
- Reduced full-depletion voltage
- Smaller clusters \rightarrow reduction of merged clusters in dense jets

At very **high fluences** thick and thin planar sensors give similar charge

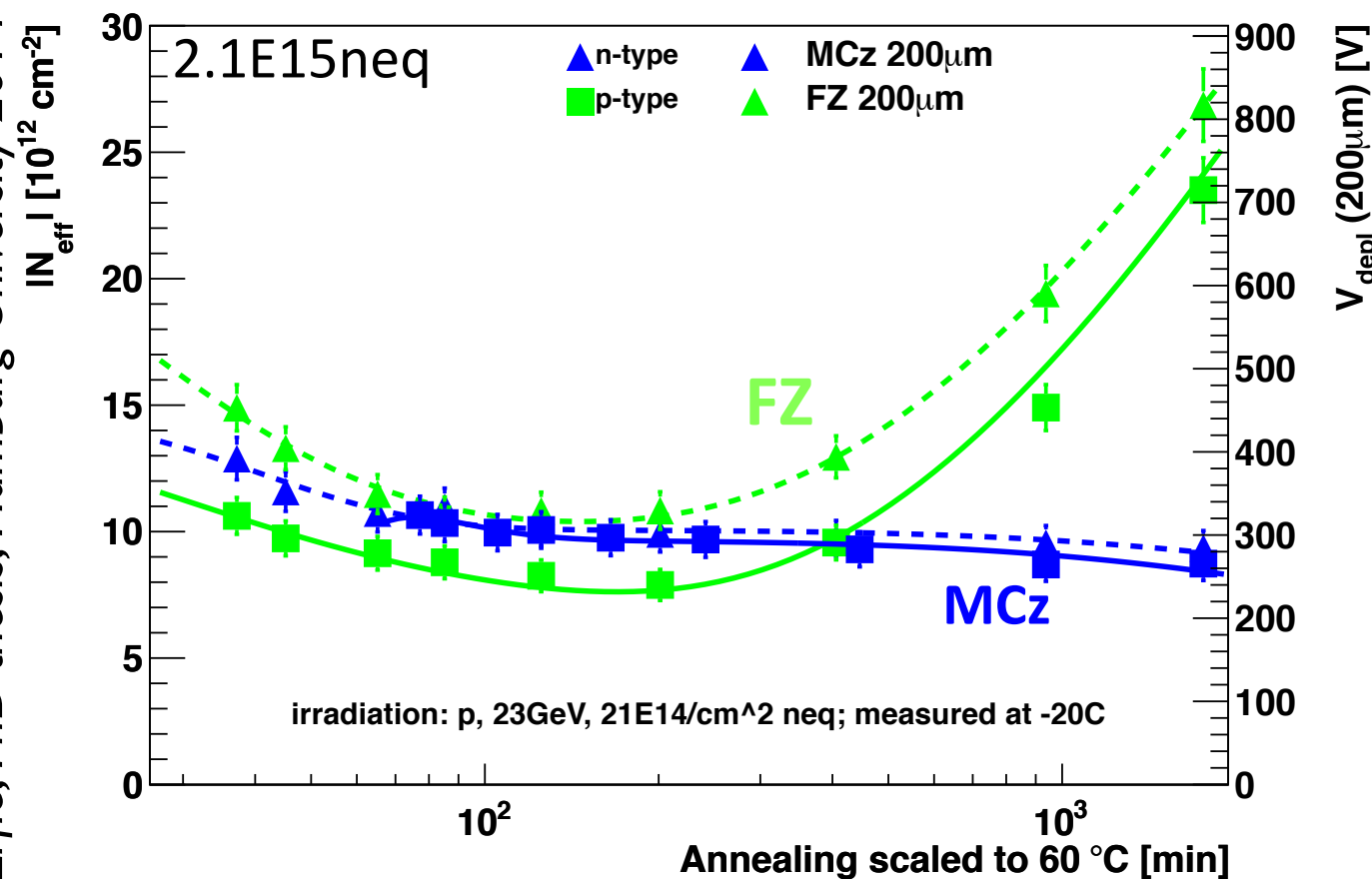


Thin planar Silicon sensors: different processes



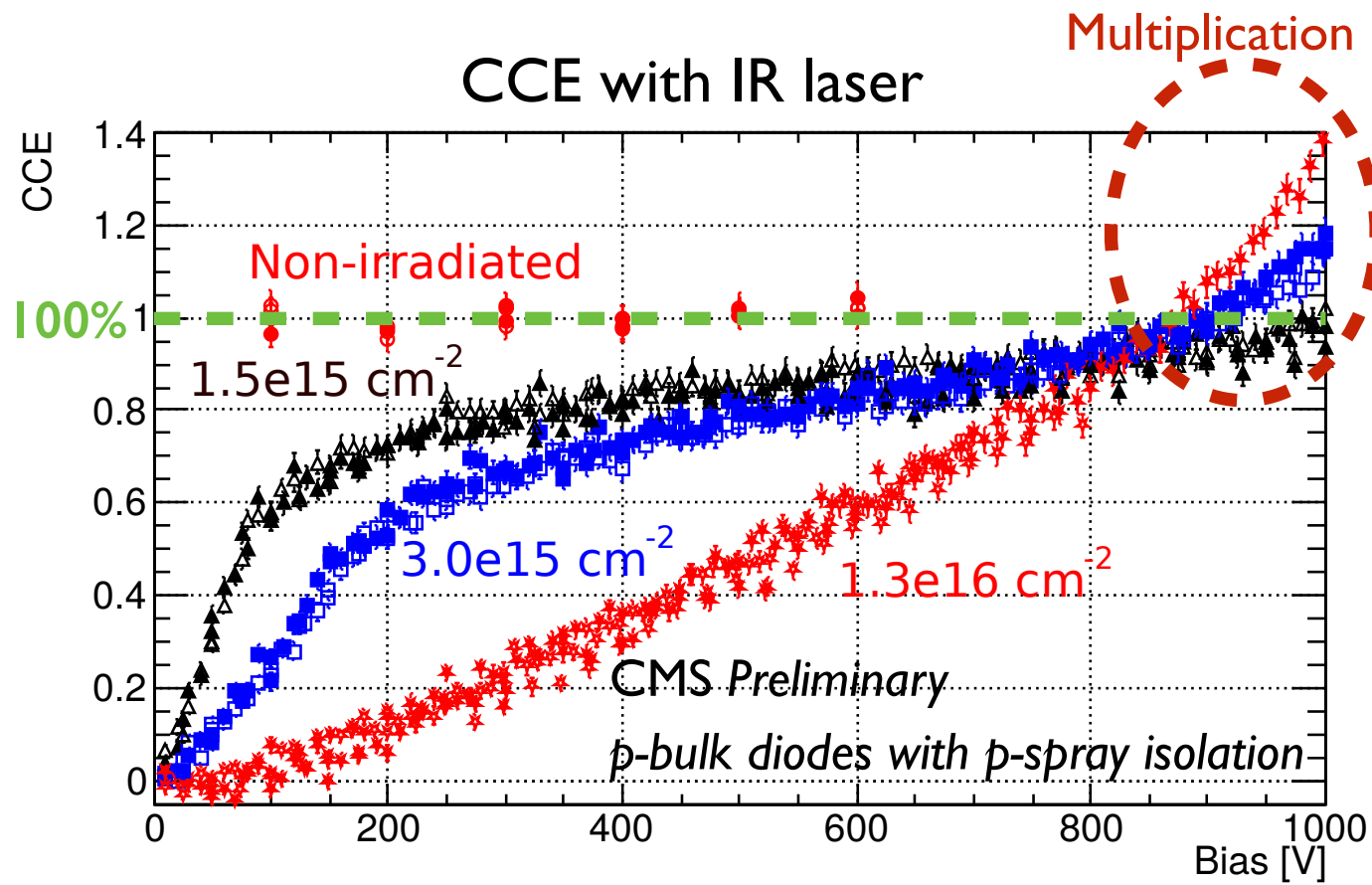
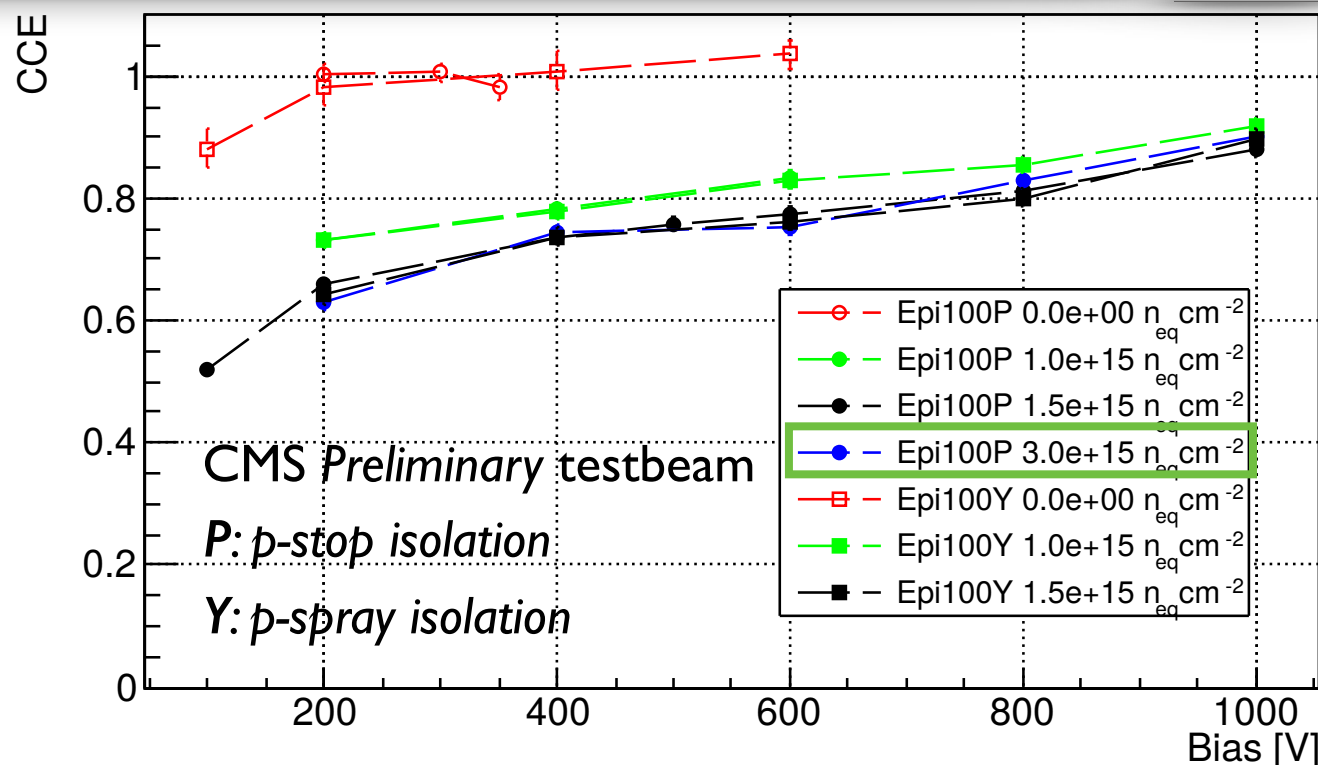
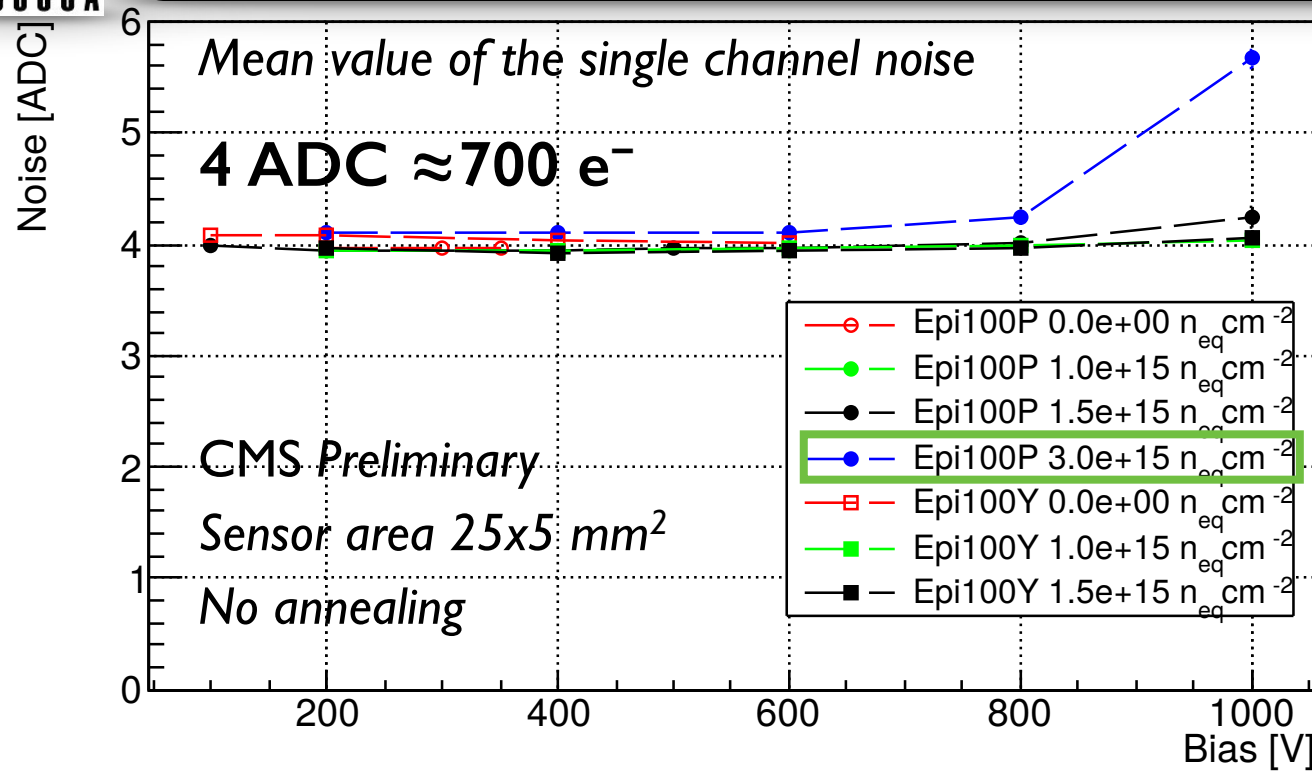
Usual annealing behaviour of Silicon after irradiation: beneficial annealing and reverse annealing

$$V_{\text{depl}} \approx q_0 / (2\epsilon_0\epsilon_r) |N_{\text{eff}}| d^2$$



- MCz is much more stable in time than FZ
- With MCz longer warm periods are possible → might impact readout chip operations / annealing
- But price for MCz is expected to be higher than FZ

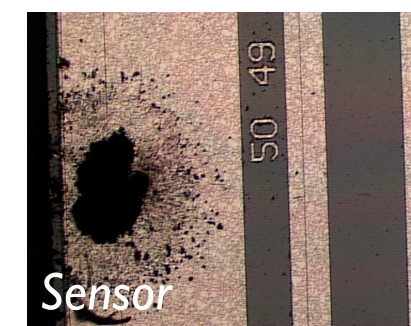
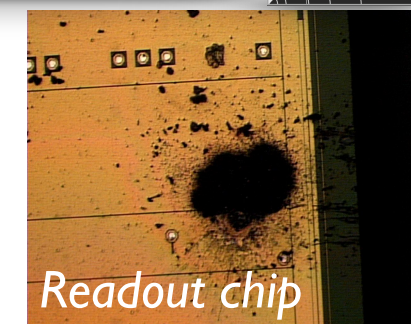
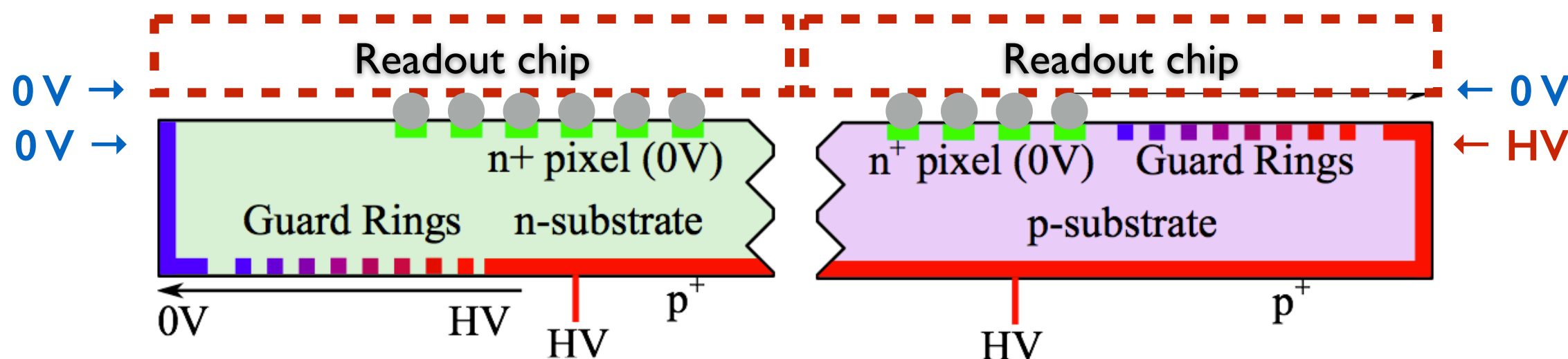
Thin planar Silicon sensors: EPI Silicon performances



n-in-p EPI strip sensors (100 μ m thick, 80 μ m pitch)

- Irradiated: -20°C (chip at $\sim +9^\circ\text{C}$)
- Non-irradiated: $+20^\circ\text{C}$ (chip at $\sim +24^\circ\text{C}$)
- Testbeam data are in agreement with measurements on diodes
- High-bias / low-temperature are needed

See poster from Matteo CENTIS VIGNALI: "Characterisation of thin irradiated epitaxial silicon sensors for the CMS phase II pixel upgrade"



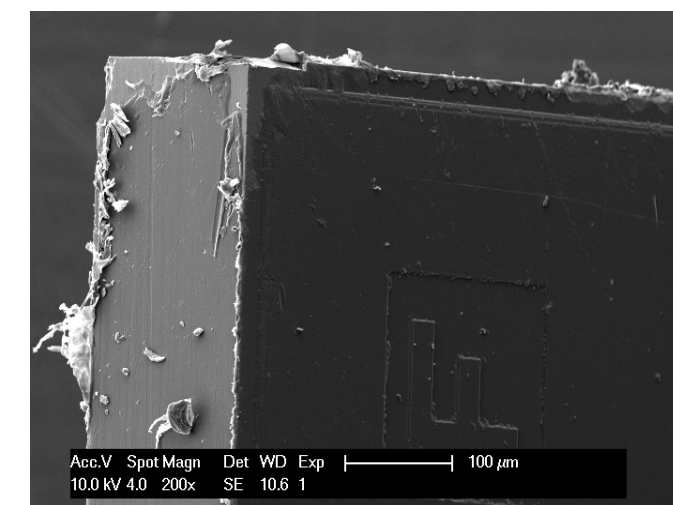
Possible solutions

● Parylene-N (5-10 μm , deposited all over the module)

- no sparking up to 1000 V
- no effect of irradiation ($1 \times 10^{16} \text{ neq} / \text{cm}^2$)
- good passivation
- concerns about protection of bond pads during module manufacturing

● BenzoCycloButene (3 μm , lithography needed)

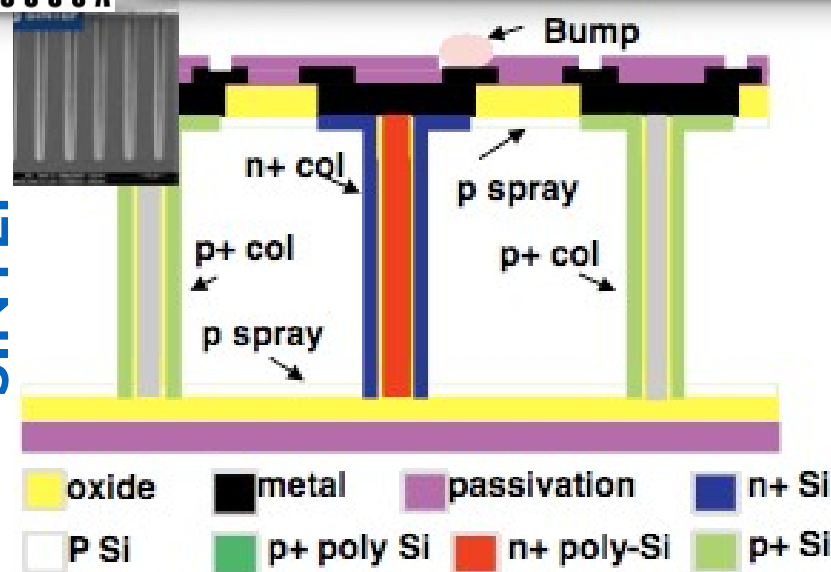
- no sparking up to 1000 V
- can be deposited before bump bonding at IZM
- need to prove radiation resistance



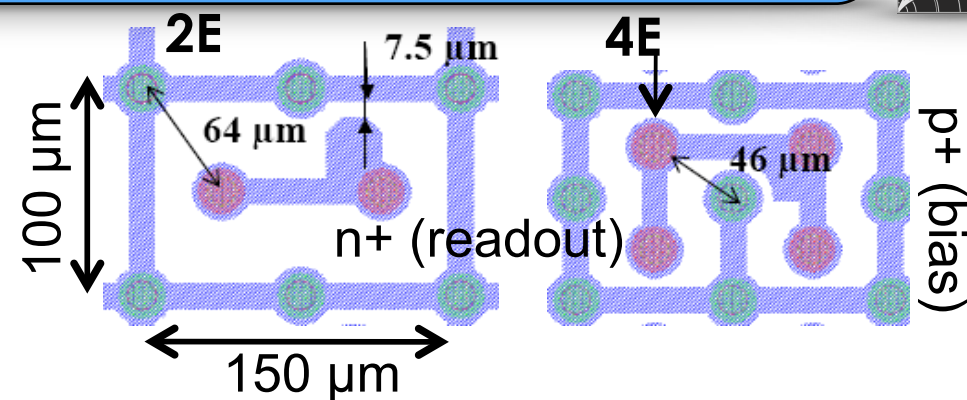
Uniform 2 μm Parylene coating
Scanning Electron Microscope image

Silicon 3D sensors: different processes

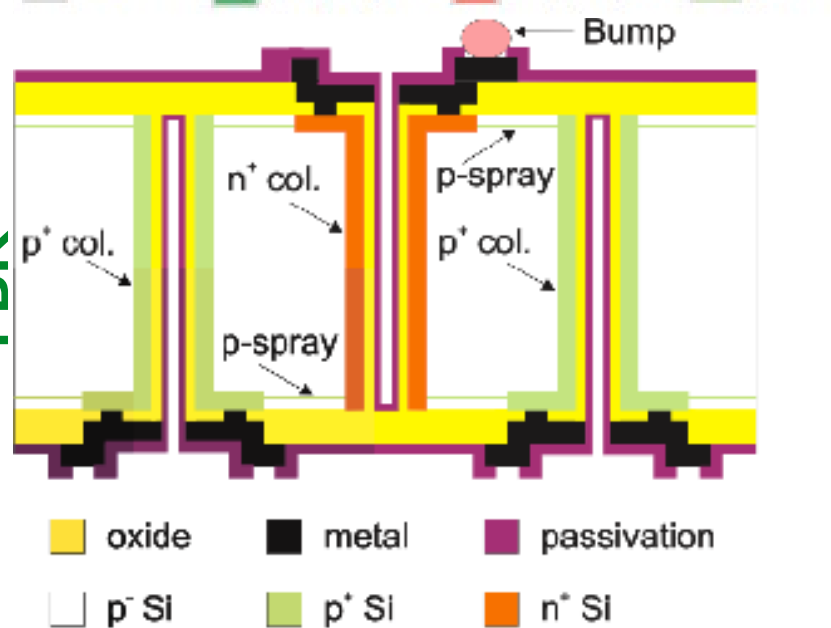
SINTEF



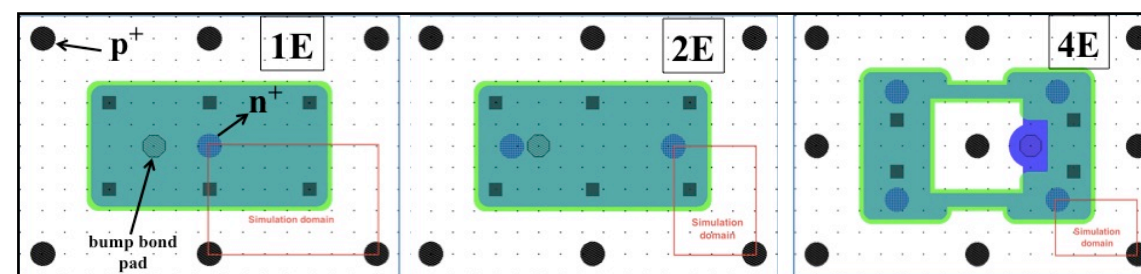
- Single-sided process
- Passing-through columns
- Active edges (*support wafer required*)



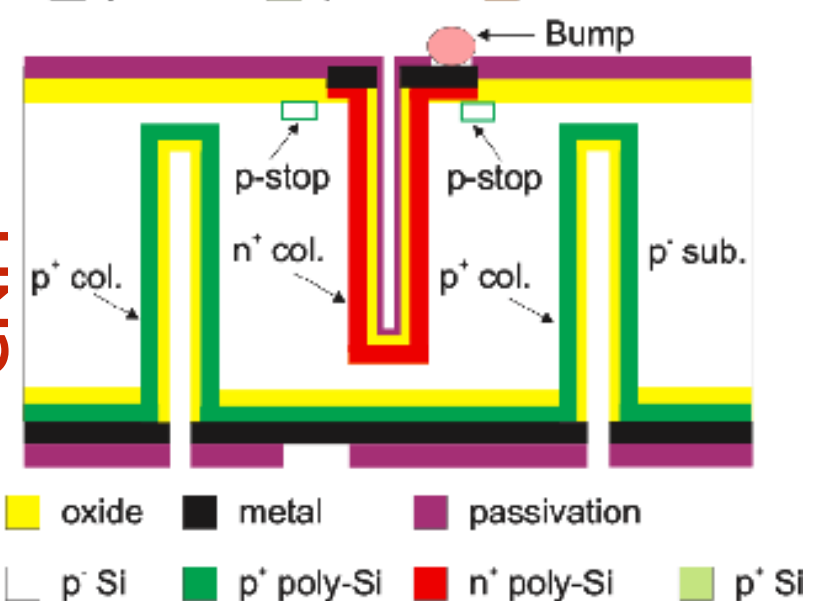
FBK



- Double-sided process
- Passing-through columns (*full*)
- Slim edges ($200 \mu\text{m}$)



CNM



- Double-sided process
- Passing-through columns (*partial*)
- Slim edges ($200 \mu\text{m}$)

Silicon 3D sensors: different processes

FBK Atlas08	$[\Phi = 0]$ charge	$[\Phi = 7 \times 10^{14}$ neq / cm ²] charge	charge loss	$[\Phi = 0]$ S/N	$[\Phi = 7 \times 10^{14}$ neq / cm ²] S/N
1E	14.3 ke ⁻	8.2 ke ⁻	43%	66	33
2E	14.8 ke ⁻	10.5 ke ⁻	29%	55	38
4E	14.2 ke⁻	11.8 ke⁻	17%	36	32
SINTEF					
2E	17.2 ke ⁻	12.9 ke ⁻	25%	60	28

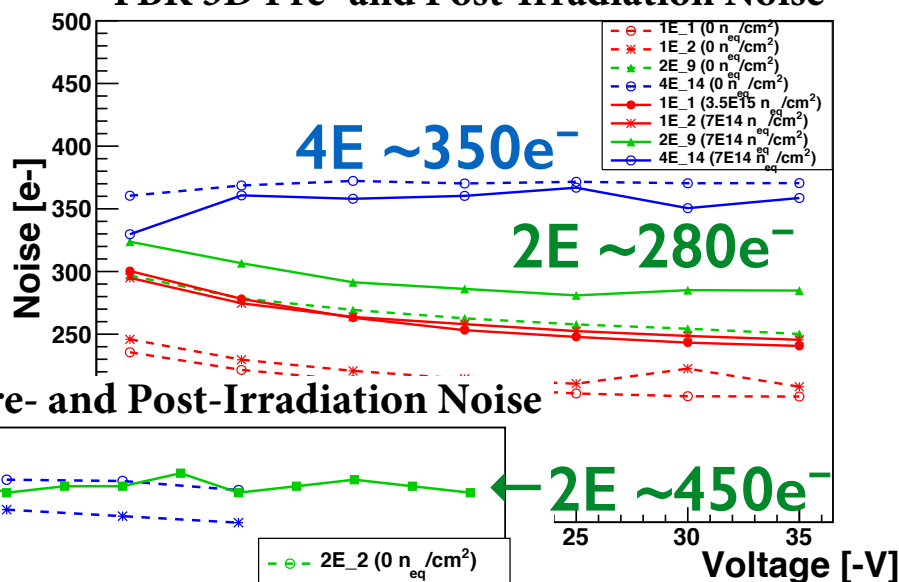
Laboratory and testbeam results from 200 μm thick FBK Atlas08 batch and SINTEF (*active edge* $\sim 20 \mu\text{m}$)

Silicon 3D sensors: different processes

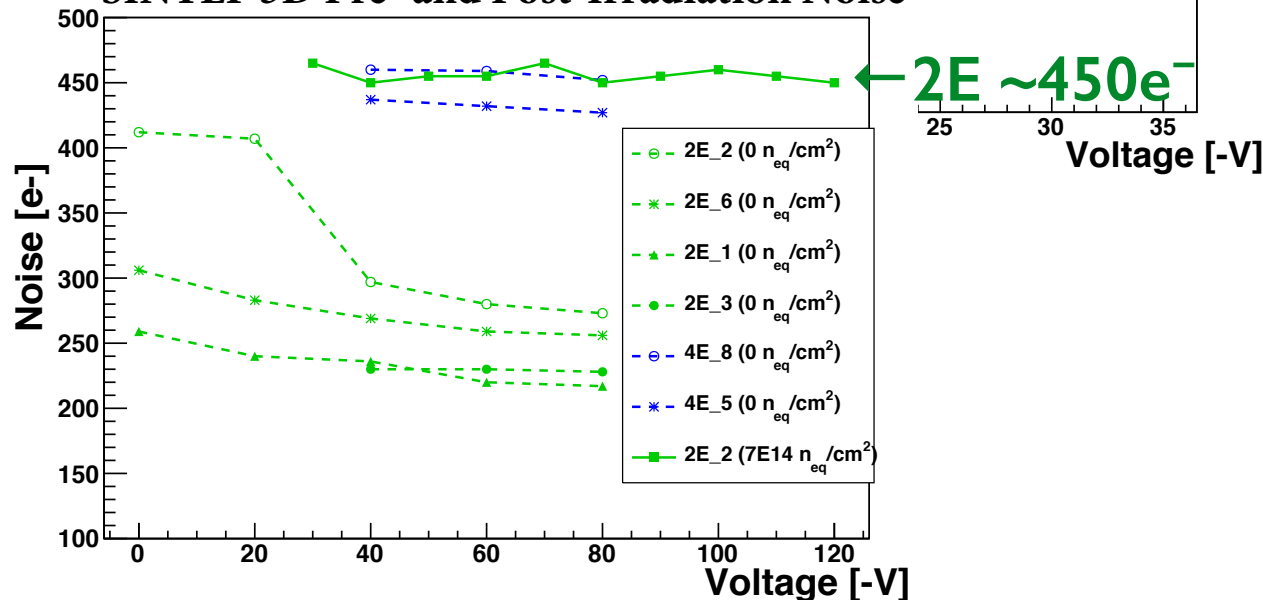
FBK Atlas08	[$\Phi = 0$] charge	[$\Phi = 7 \times 10^{14}$ neq / cm ²] charge	charge loss	[$\Phi = 0$] S/N	[$\Phi = 7 \times 10^{14}$ neq / cm ²] S/N
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Laboratory and testbeam results from 200 μm thick FBK Atlas08 batch and SINTEF (active edge $\sim 20 \mu\text{m}$)

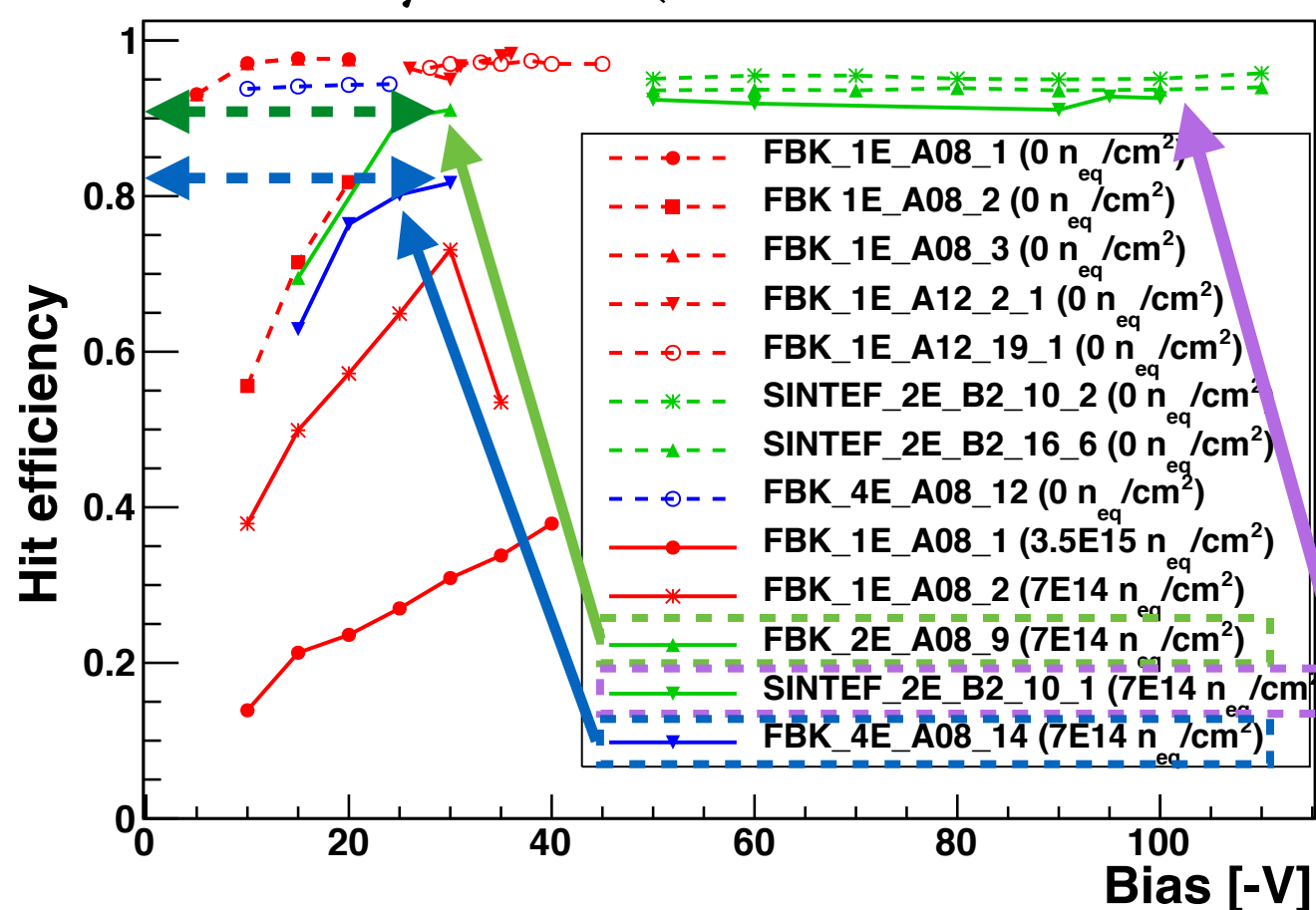
FBK 3D Pre- and Post-Irradiation Noise



SINTEF 3D Pre- and Post-Irradiation Noise



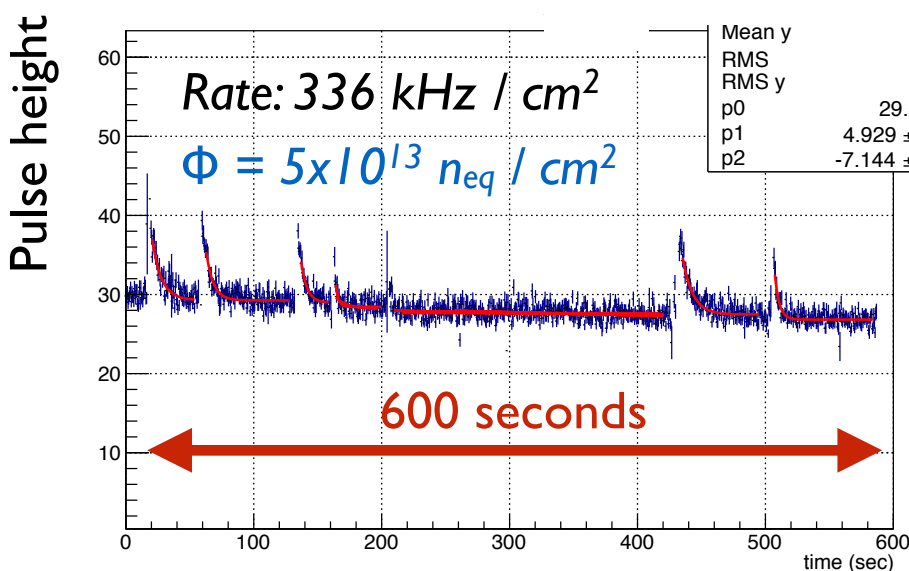
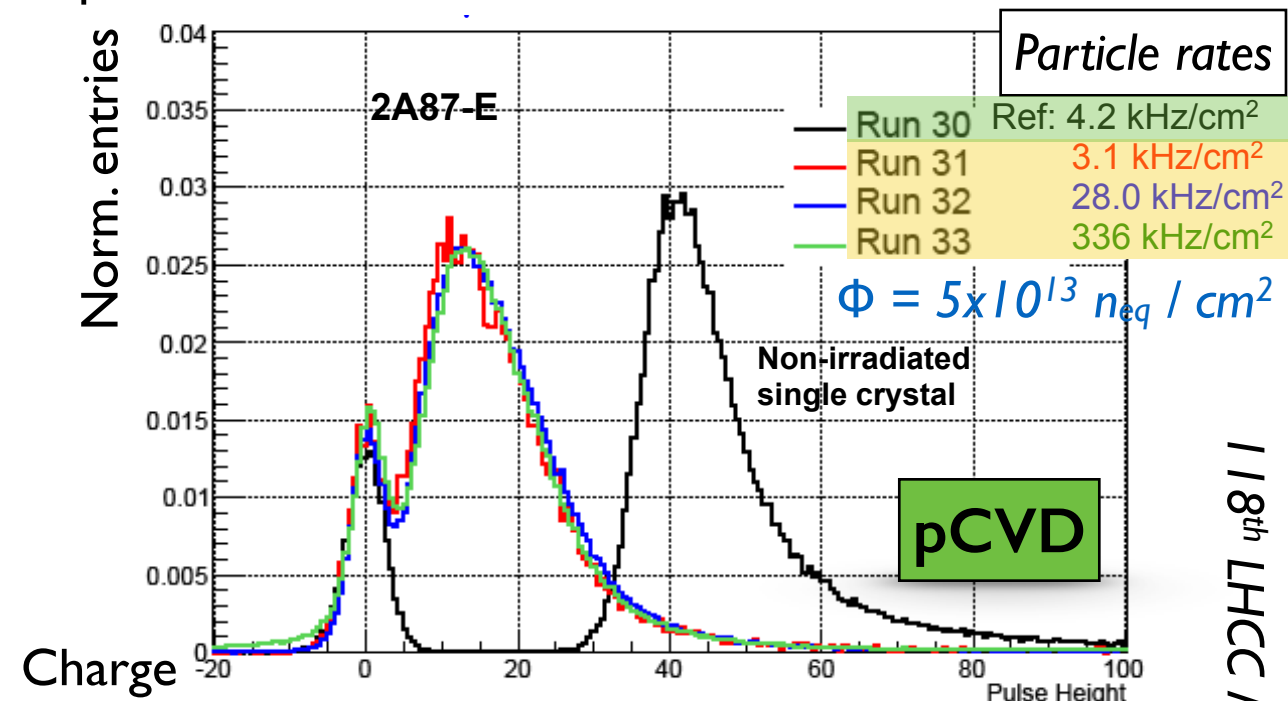
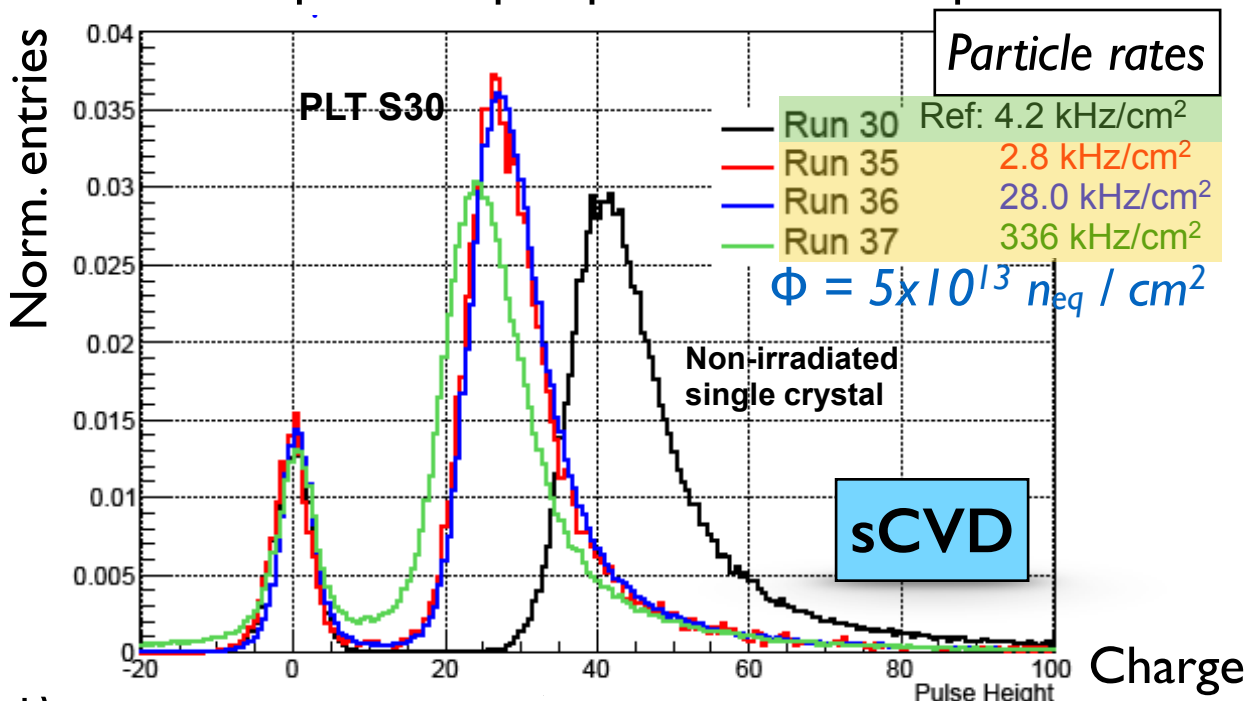
Hit Efficiency vs. Bias (Pre- and Post-Irradiation)



Several problems have still to be overcome

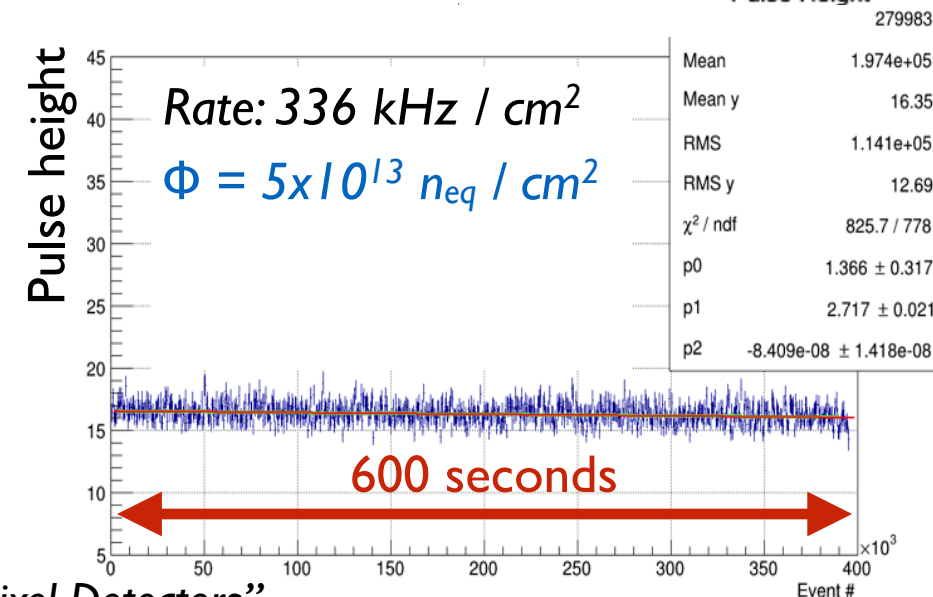
● **Polarisation effects**

- Availability of diamond material in sufficient quantity and quality (*different collection length in samples coming from same production, influence of surface treatment on detector properties, scarceness of diamond material*)
- Improved radiation hardness with respect to Silicon is still to be demonstrated
- Reliable interconnection of diamonds to readout chips on production scale
- No plausible perspective for mass production → no reliable price estimate

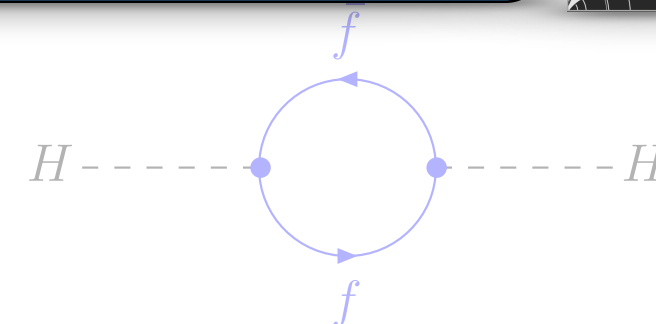


Time and rate dependance

No time nor rate dependance

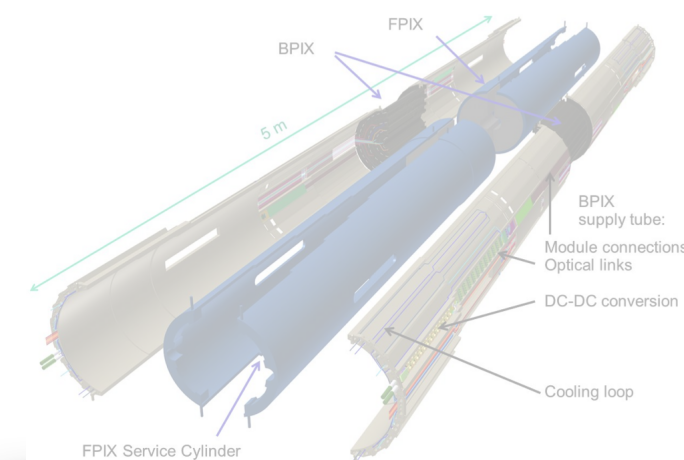


- CMS pixel phase-II upgrade motivations



- Detector operating conditions

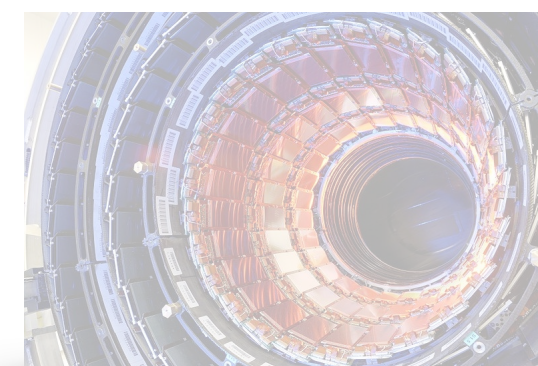
- Detector layout choices



- Readout chip specifications

- Possible sensor choices

- Conclusions



- **Pixel detector operating conditions during phase-II are extremely challenging**
 - $\langle \text{PileUp} \rangle = 140$
 - Radiation @30 mm from IP: $2 \times 10^{16} \text{ n}_{\text{eq}} / \text{cm}^2$
 - Dose @30 mm from IP: 10 MGy (1 Grad)
 - Hit rate: $\sim 2 \text{ GHz} / \text{cm}^2$
- Final **general detector layout** and geometry is almost defined
- **Readout chip development** (*Atlas-CMS collaboration*): 65 nm candidate technology → need to demonstrate radiation hardness up to foreseen 10 years operation at HL-LHC
- **Sensor development**: Silicon thin planar n-in-p (and/or Silicon 3D for innermost layer) candidate technology → need to define sensor process, bias isolation geometry, thickness, electrode geometry
- Still a lot of exciting work ahead (hopefully) leading to future physics discoveries !

Backup

Major achievement of HLC: Higgs discovery in 2012 !

That's not the whole story, there are other questions that need to be answered:

- What's the origin of Higgs mass correction-fine tuning ?
- How do we incorporate gravity ?
- Why such a puzzling spectrum of fermion masses and mixings ?
- What is the nature of Dark Matter ?
- Is there are new sources of CP violation ?

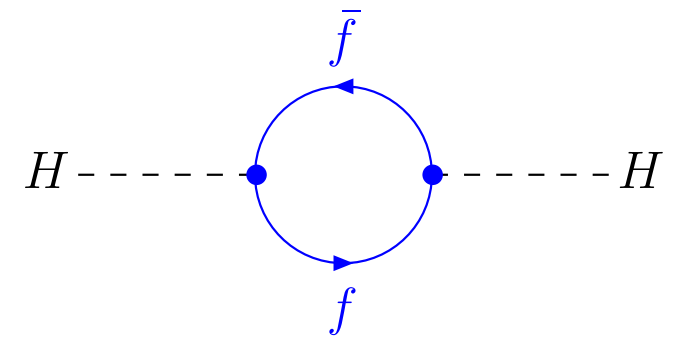
What's the origin of Higgs mass correction-fine tuning ?

- $M^2_H = M^2_{H,0} + \delta M^2_H$ → quadratically divergent

- From fermion loops:

$\delta M^2_{H,f}$ at $\Lambda = M_{\text{Plank}}$ is $\delta M^2_{H,f} \approx 10^{35} \text{ GeV}^2$

$$\delta M^2_{H,f} = -\frac{\lambda_f^2}{8\pi^2} \left[\Lambda^2 - m_f^2 \ln \frac{\Lambda^2}{m_f^2} \right] + \dots$$

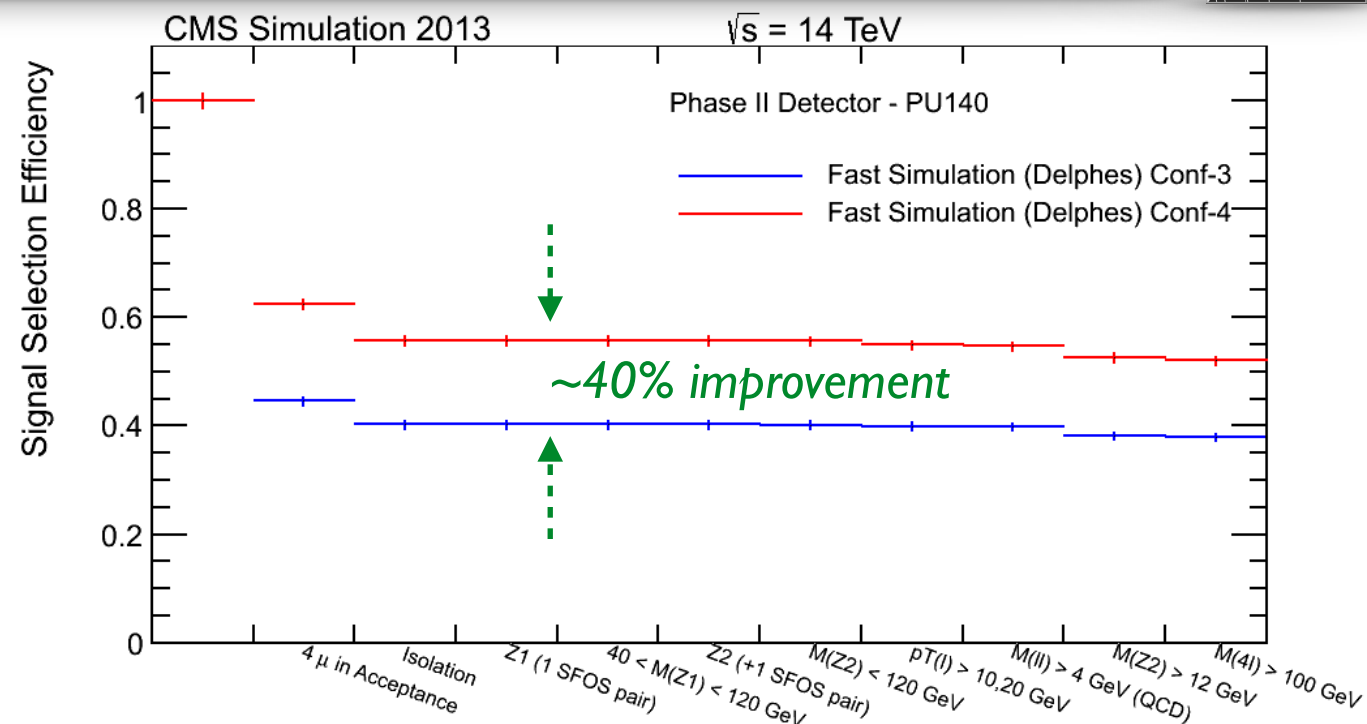


An Higgs mass of $M_H = 126 \text{ GeV}$ requires an *adjustment* between the tree-level mass $M^2_{H,0}$ and $\delta M^2_{H,f}$ of $1/10^{31}$!

There must be a mechanism that cancel out the *adjustment* → precision measurements of Higgs sector should unveil such a mechanism

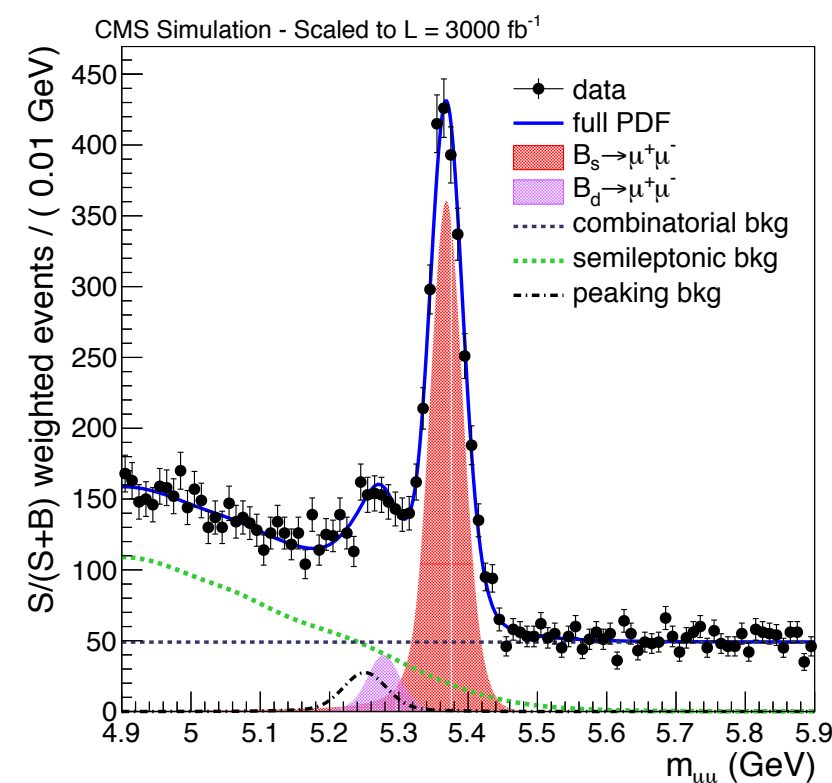
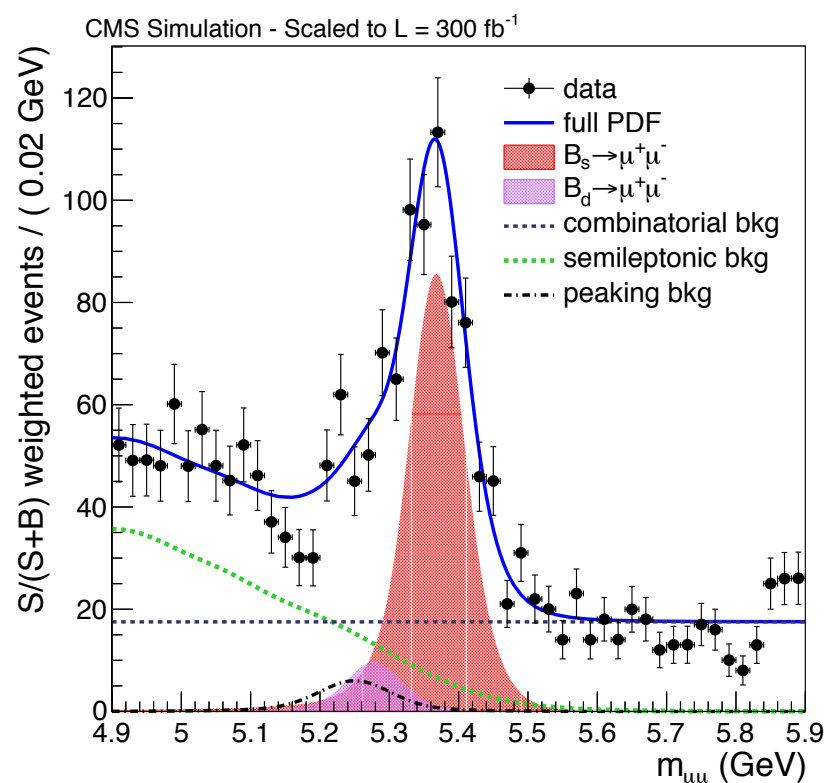
Efficiency cut flow for $H \rightarrow ZZ \rightarrow \mu\mu\mu\mu$

- **Conf-3:** sub-detectors have same **angular acceptance** as **current version**, but central tracking detector and the forward electromagnetic calorimeters are replaced and improved
- **Conf-4:** tracking, electromagnetic and hadronic calorimetry, and muon detector, are **increased in acceptance up to $\eta \approx 4$**

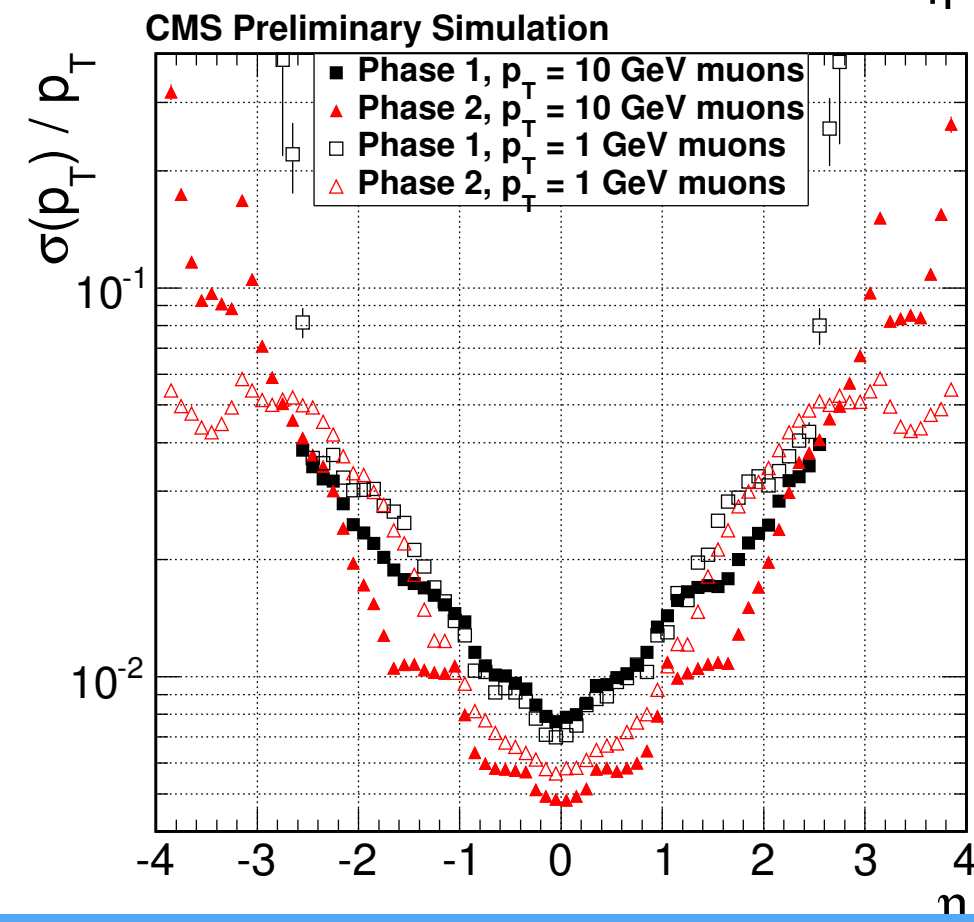
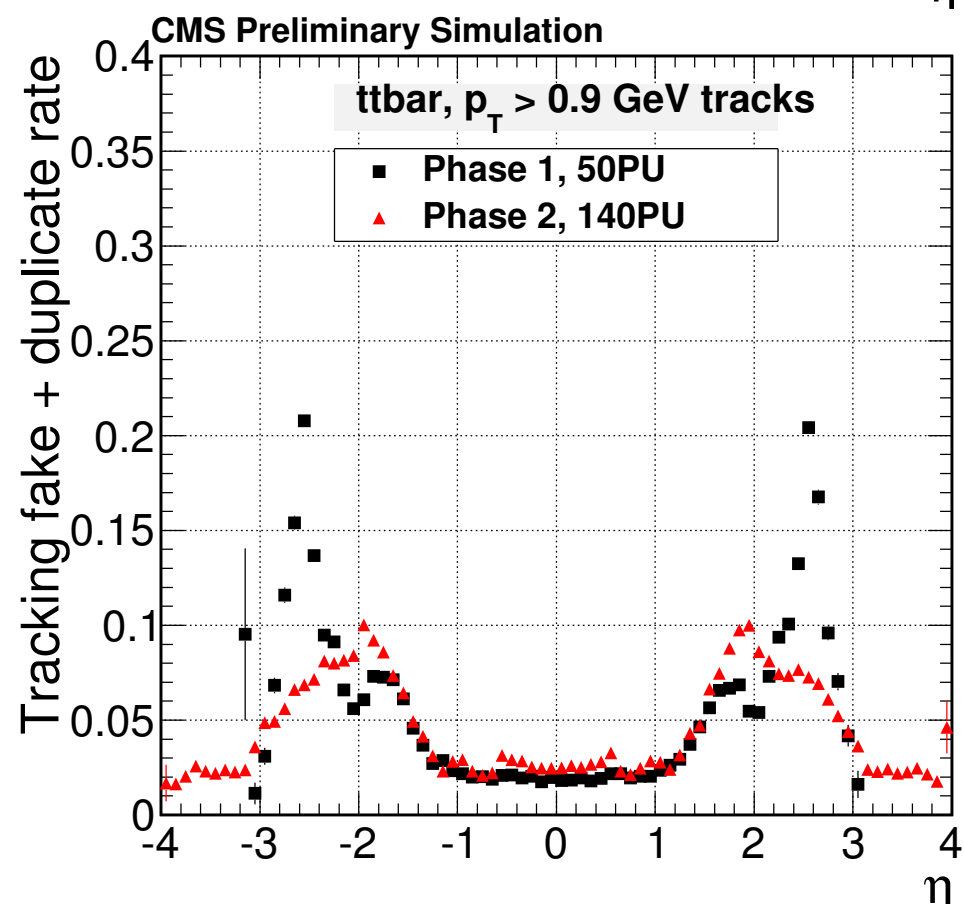
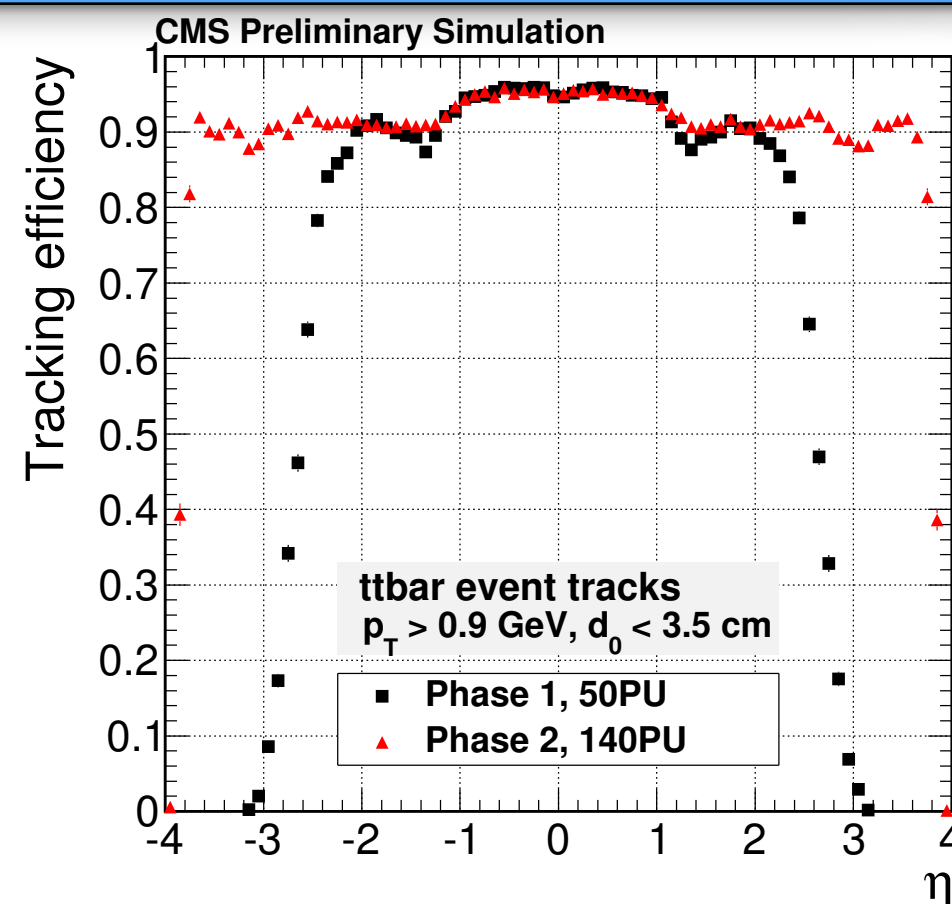
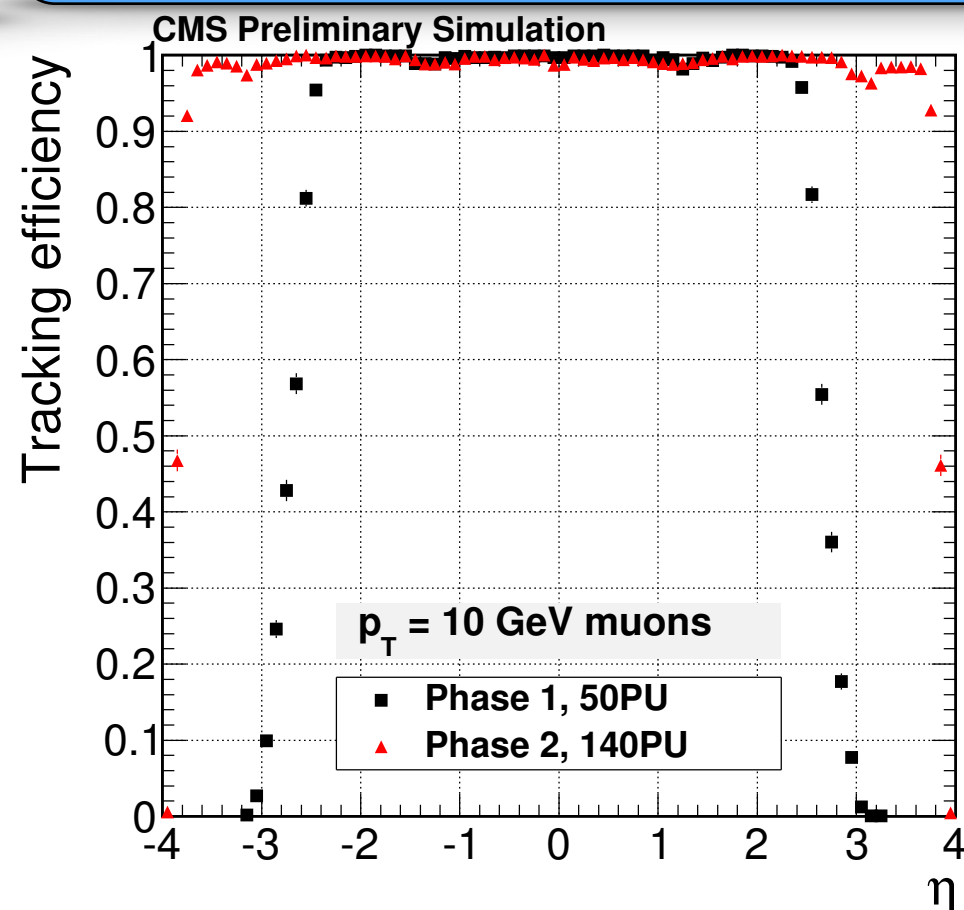


$B_{s/d} \rightarrow \mu\mu$ mass resolution for 300 fb^{-1} and 3000 fb^{-1}

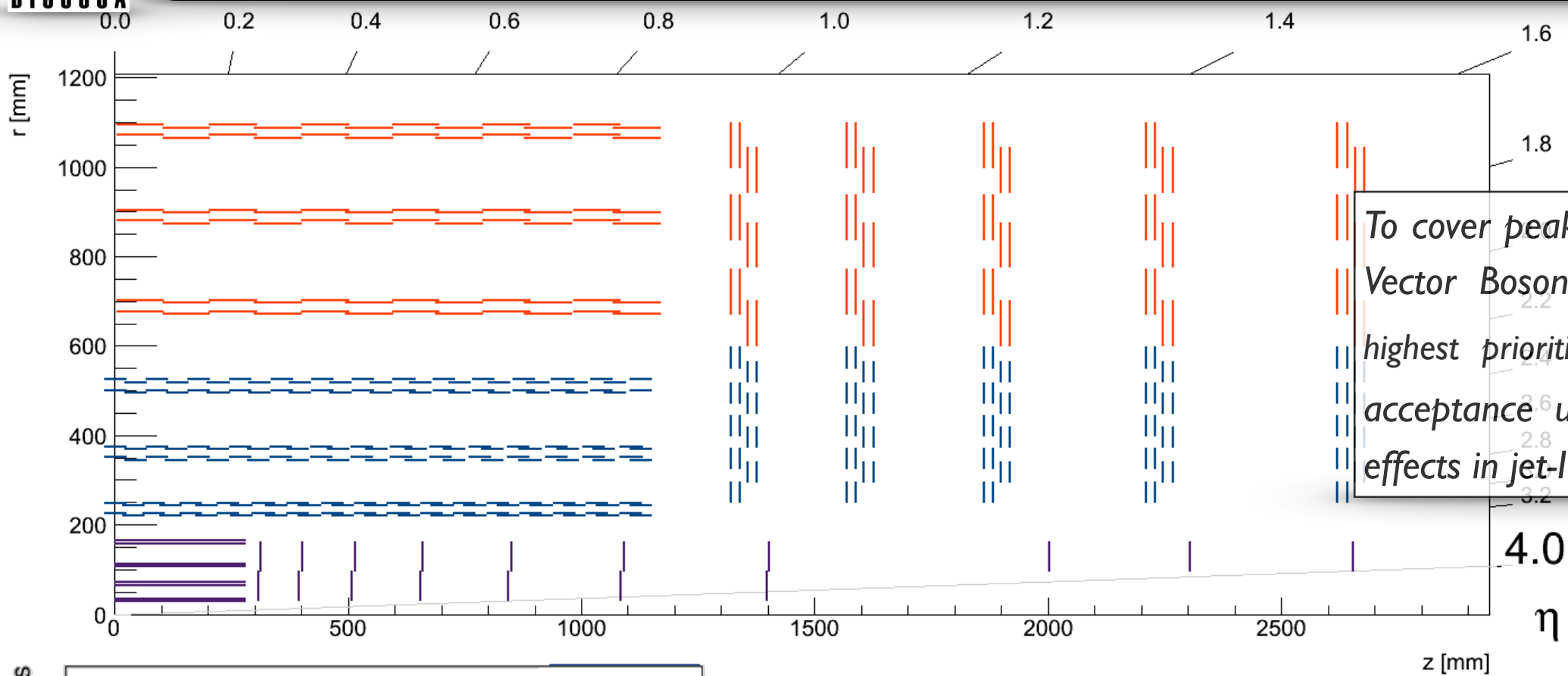
- Improvement in mass resolution for the 3000 fb^{-1} projection expected from improved inner tracking system and by removing end-cap candidates



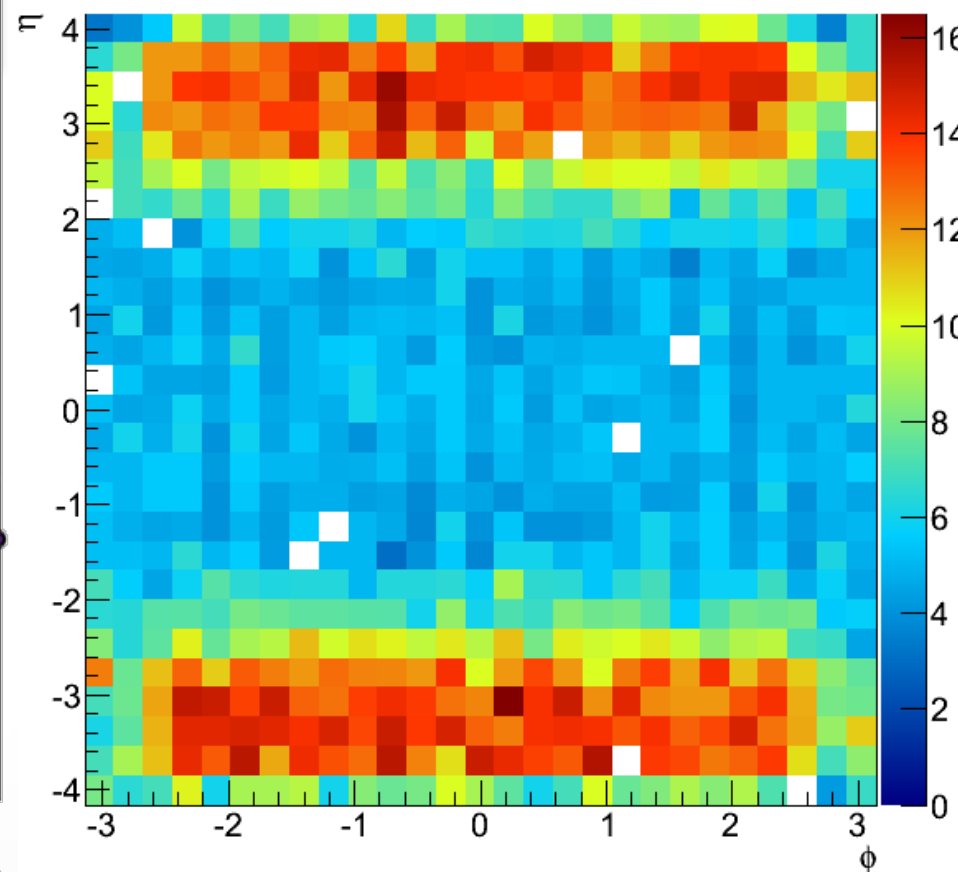
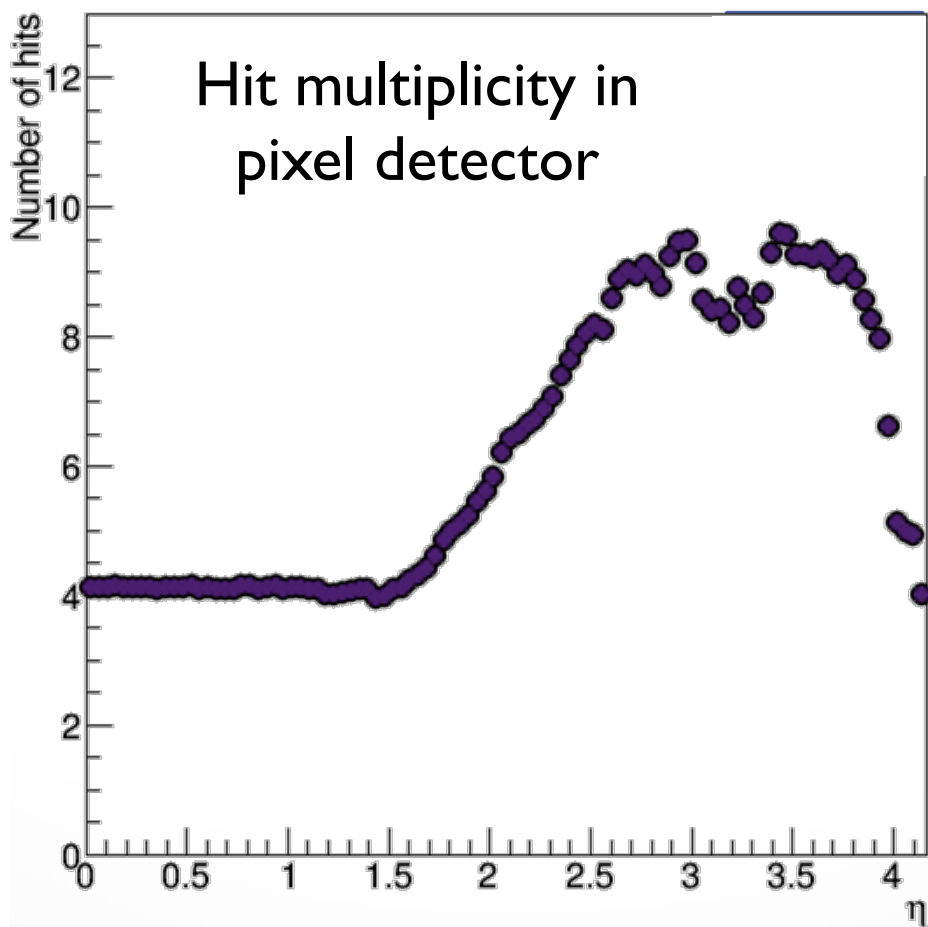
Phase-II tracking performance



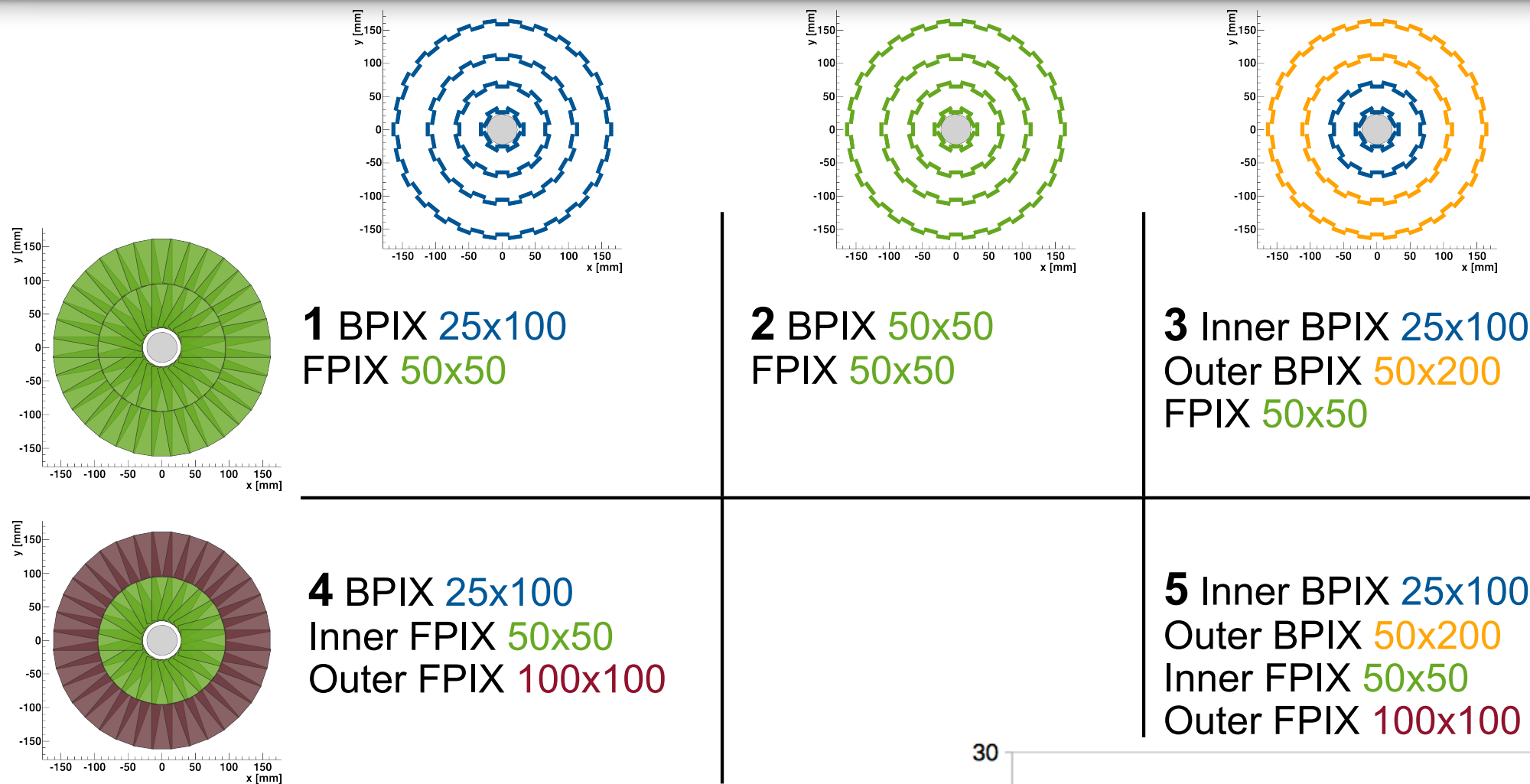
Forward pixel acceptance studies



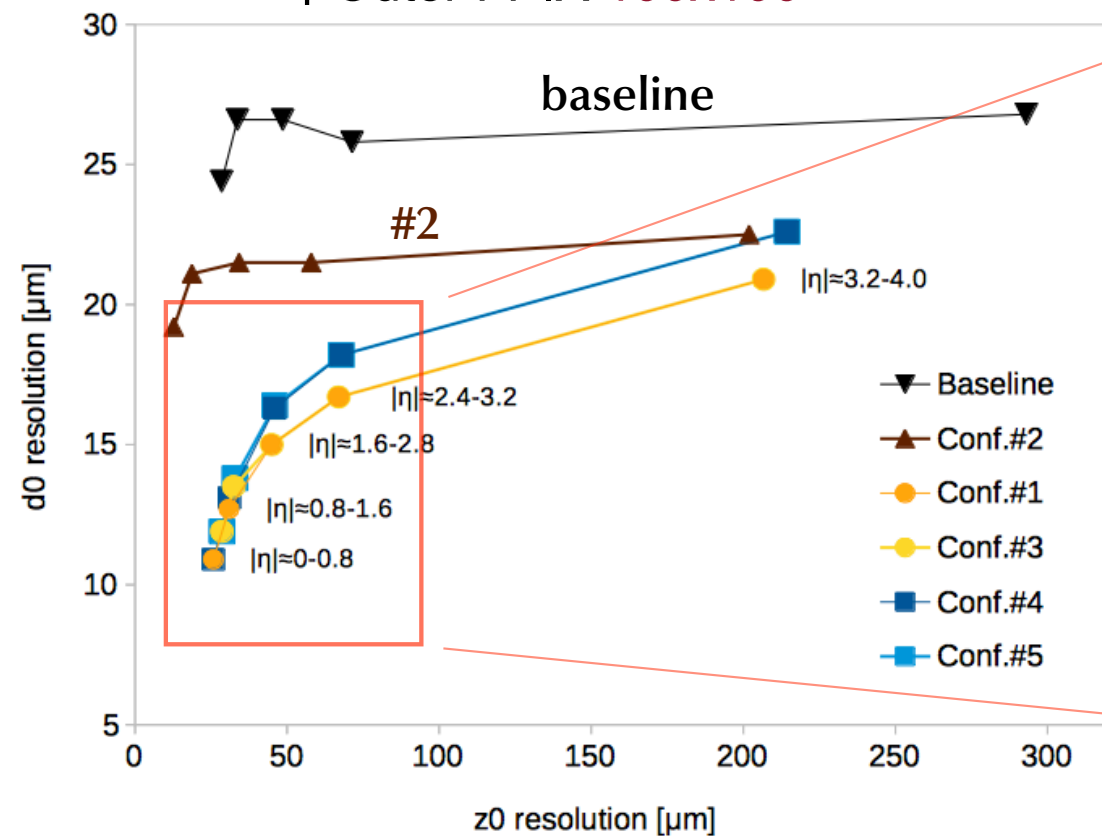
To cover peak production region of jets from Vector Boson Fusion and VBS (among highest priorities of the physics program) → acceptance up to $\eta \approx 4$, to mitigate PU effects in jet-ID and energy measurement



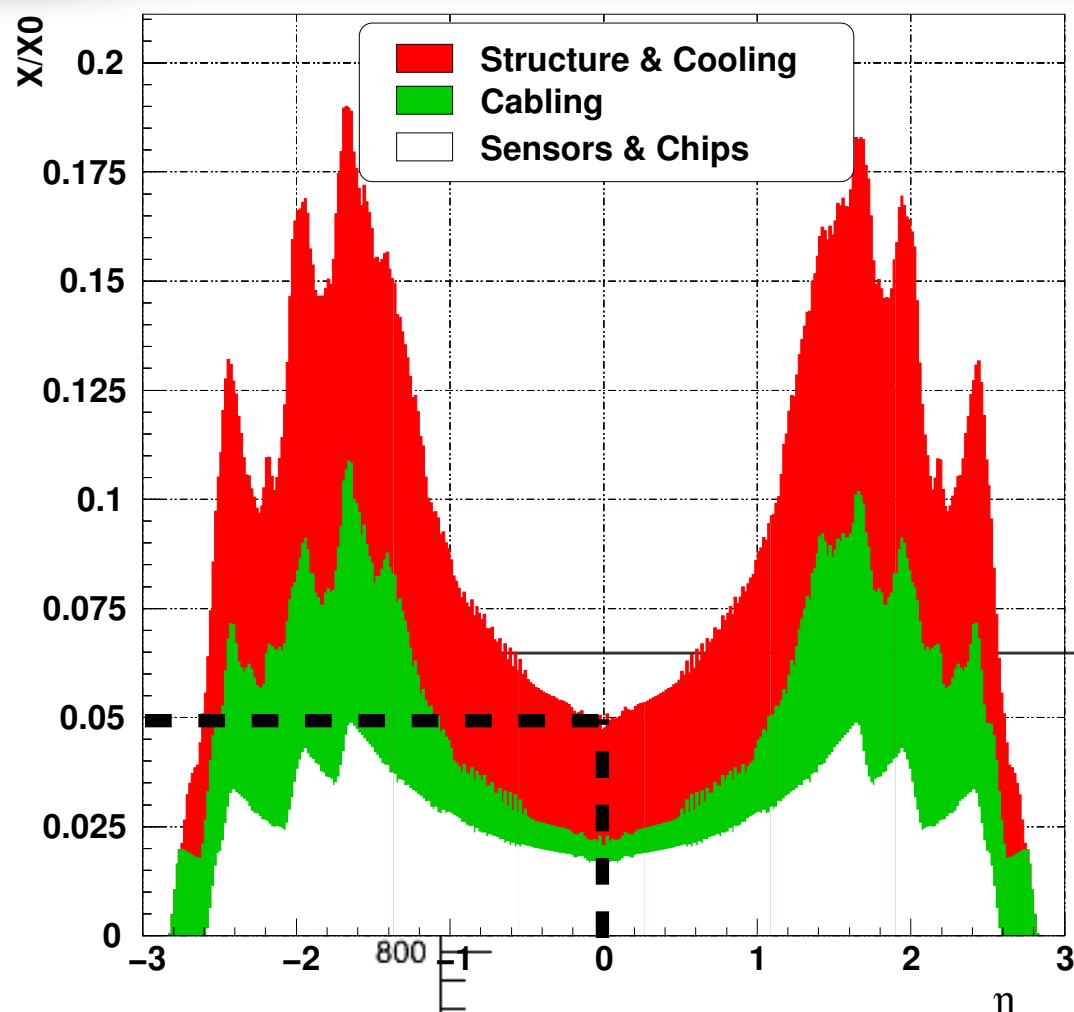
- Barrel**
- pixel size: 50x50 and 100x100 μm^2
 - modules with 4x2 and 4x1 chips
- Forward**
- pixel size: 50x50 and 100x100 μm^2
 - modules with 2x2 and 2x1 chips



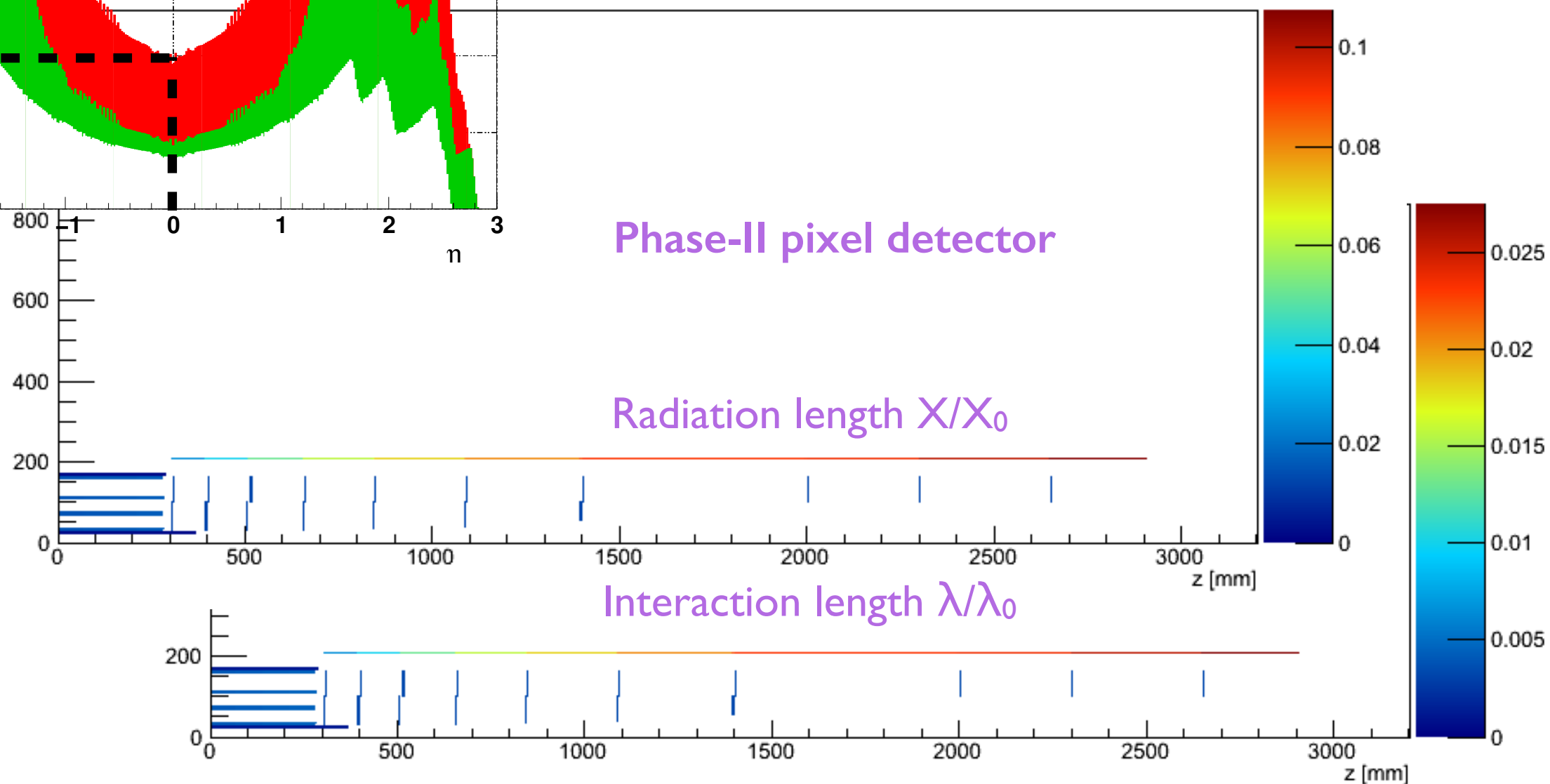
Petal configurations with mixed pixel sizes show better tracking performance than **Petal #2** and **baseline** (phase-I) geometries

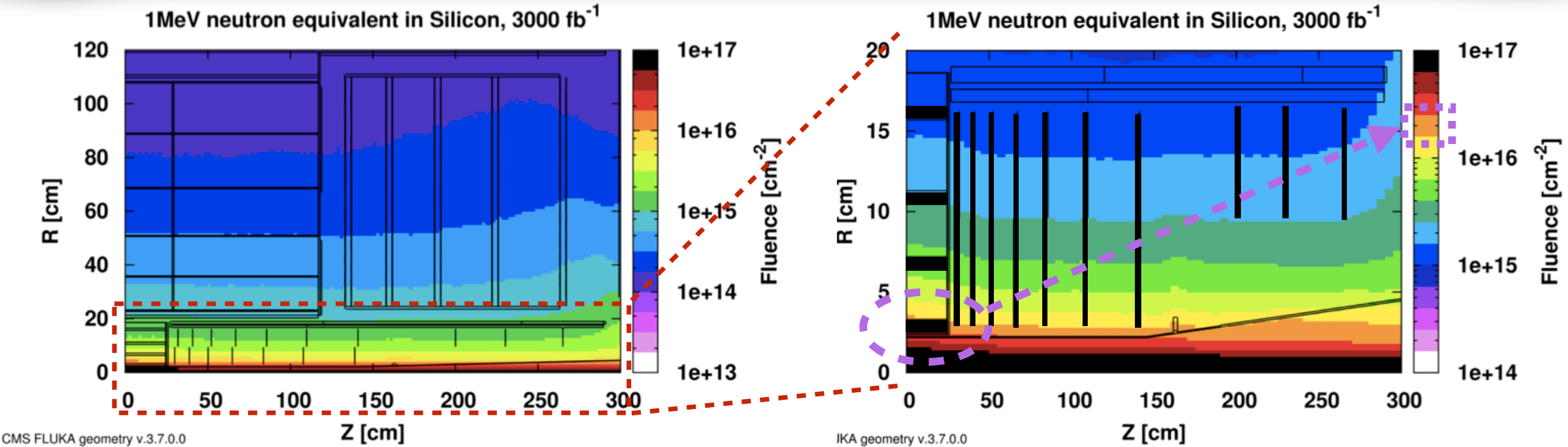


Radiation length for the present pixel detector



The foreseen phase-II pixel detector will be “lighter” than the present one





Radiation fluence after 3000 fb⁻¹ in the tracker (left) and zoom in the pixel (right)

Posible sensors technologies

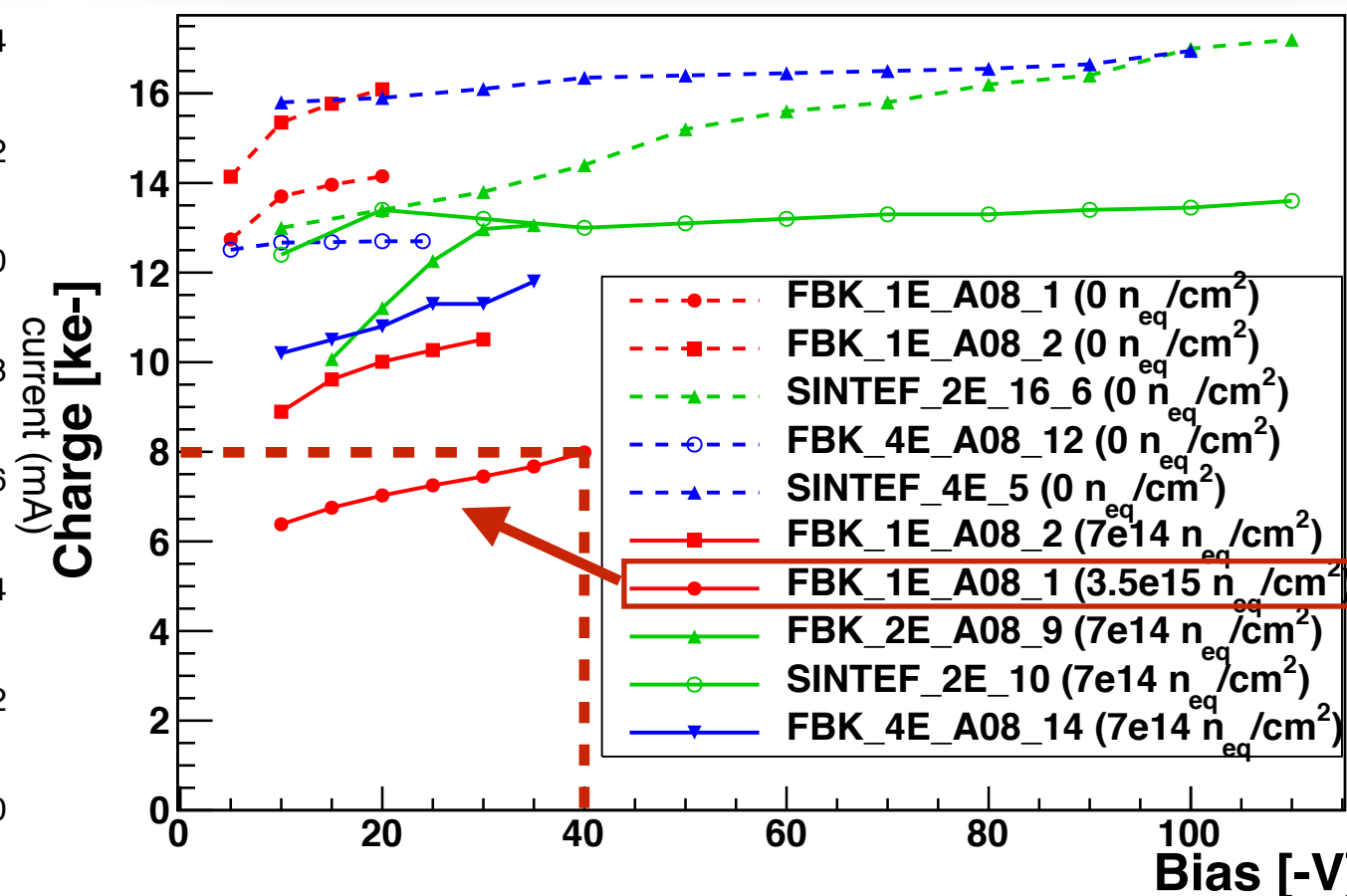
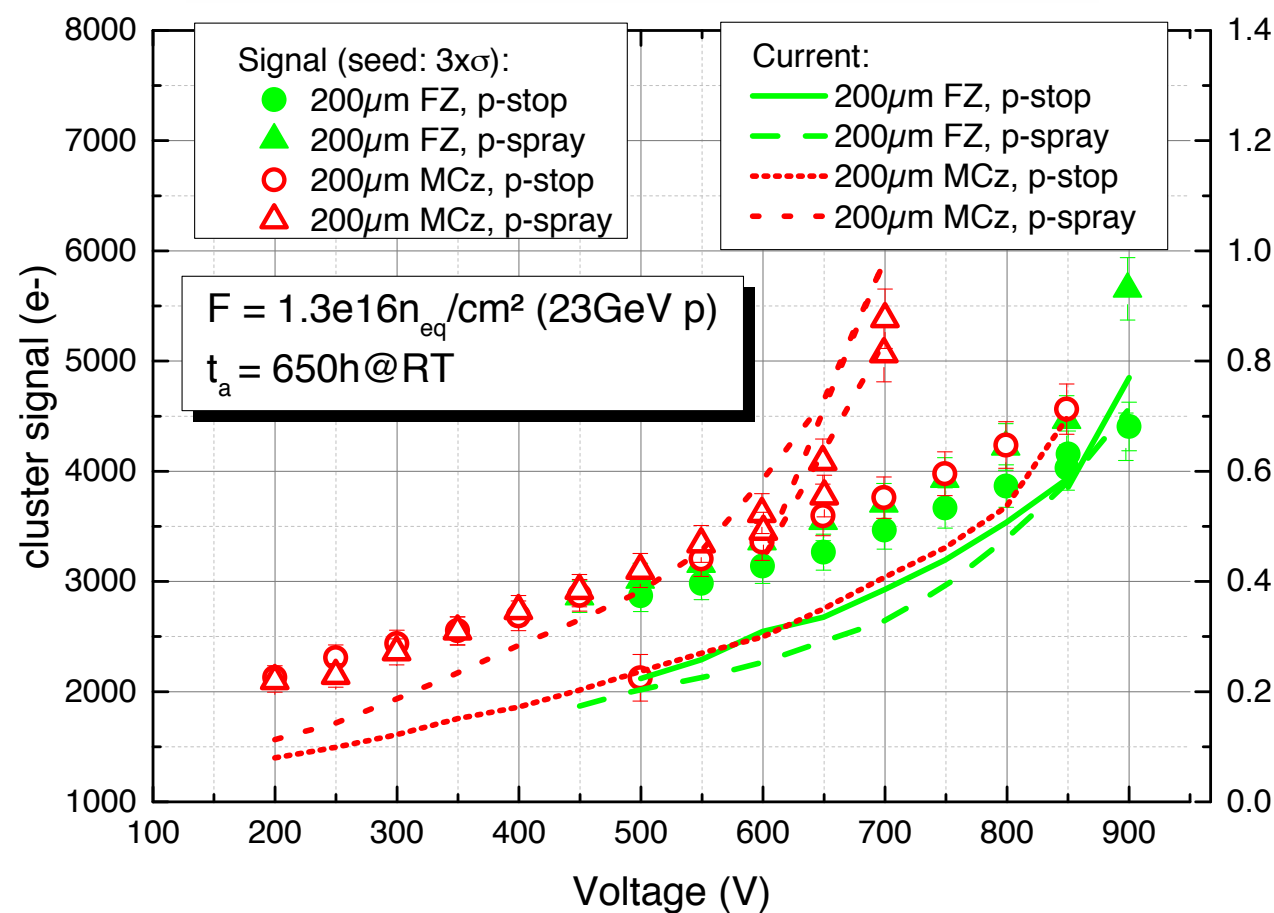
- Favoured technology: **planar Silicon**
 - Define suitable n-in-p process and design (*more cost effective than present n-in-n because single sided process*)
 - Thin thickness
 - Requires robust spark rejection material
- Alternative/complementary for innermost layer: **3D Silicon**
 - Define suitable sensor thickness and electrode geometry
 - Address production issues (*e.g. yield and cost*)

Planar n-in-p need to define

- Sensor thickness
- Sensor process (FZ, MCz, EPI)
- Spark rejection material
- Pixel isolation and bias scheme

Silicon 3D need to define

- Number of columns per cell
- Column size → sensor thickness
- Pad position
- Production process: single/double sided

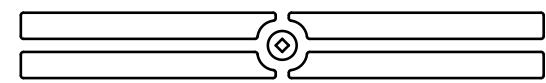
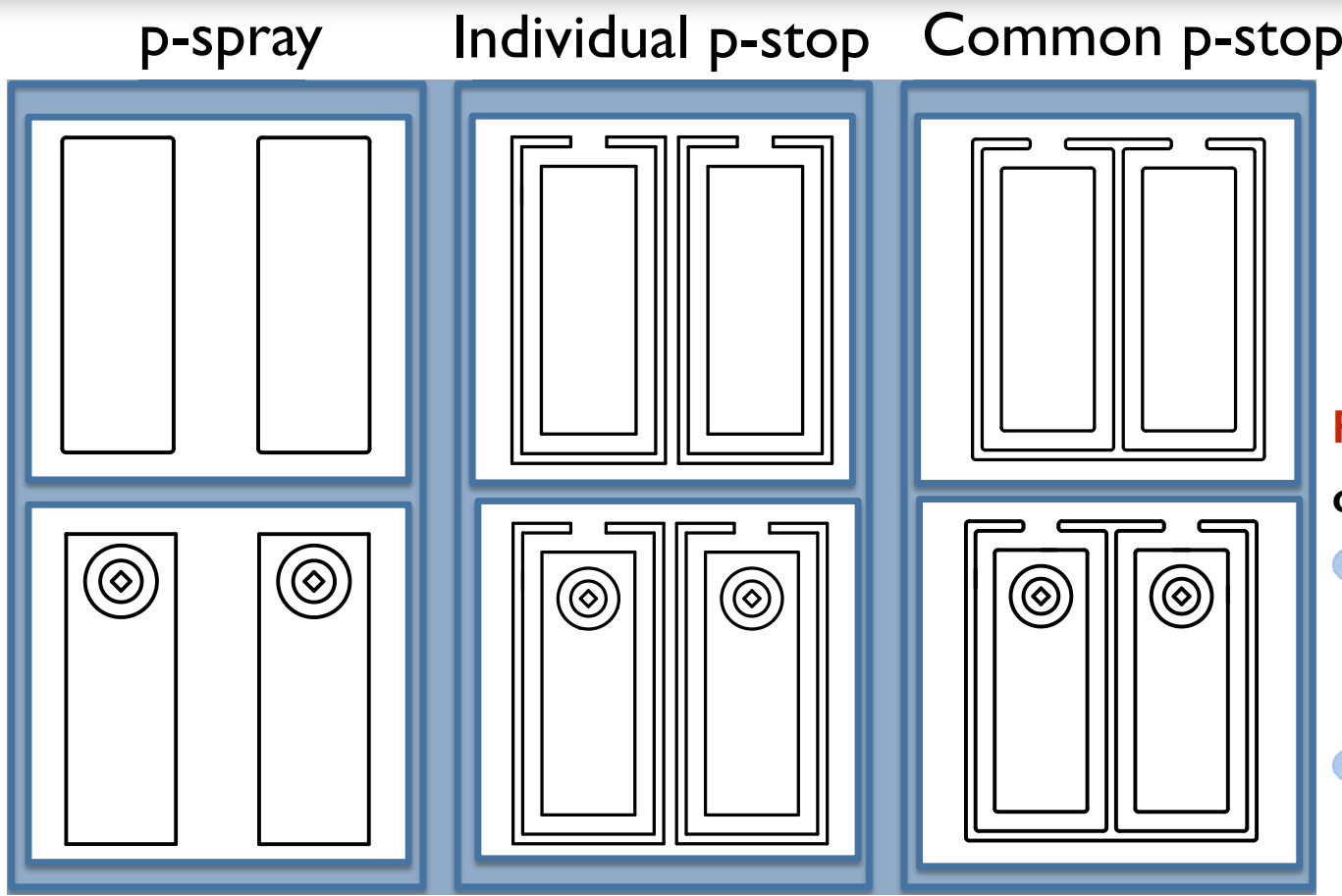


arXiv:1402.6384

Signal charge and leakage current in planar n-in-p Silicon strip structures in different processes and isolations (irradiation $1.3 \times 10^{16} n_{eq} / cm^2$)

Signal charge in 3D n-in-p Silicon pixel structures from different vendors and with different column configurations (*before and after irradiation up to $3.5 \times 10^{15} n_{eq} / cm^2$*)

Thin planar Silicon sensors: isolation and bias scheme



p-spray with common punch through

Forward **PIXel** preliminary measurements on **EPI** and **FZ** designs (*non irradiated*)

- **EPI** FPIX 50 μm with larger implants FPIXE have smaller breakdown ($\sim 350\text{ V}$) compared to larger gap pixel FPIXF layouts ($\sim 500\text{ V}$)
- **FZ** FPIX 120 μm with larger gap pixel FPIXF have smaller breakdown ($\sim 380\text{ V}$) compared to larger implants FPIXE layouts ($\sim 600\text{ V}$)

Barrel **PIXel** preliminary measurements on **EPI** and **FZ** designs (*non irradiated*)

- **EPI** BPIX 50 μm with p-spray isolation and different gap sizes (BPIXA - BPIXD) show breakdown at $\sim 550 - 600\text{ V}$
- **EPI** BPIX 100 μm with p-spray isolation and different gap sizes (BPIXA - BPIXD) show a breakdown $> 1100\text{ V}$
- Leakage current of both **EPI** BPIX 50 μm and 100 μm sensors becomes noisy after 450V - 500V
- **FZ** BPIX 120 μm with p-spray isolation and different gap sizes (BPIXA - BPIXD) show a breakdown $> 1100\text{ V}$

HPK wafer contains 6 different layouts

- **BPIX A-C**: Gap in the bias structure between 14 μm ($\sim 8\%$ affected area) and 22 μm (16% of the area affected), gap between pixels: 36 μm contain p-stop mask and (in principle) work with p-stop isolation also.
- **BPIX D**: No p-stops, small bias structure (10 μm gap, $\sim 5\%$ affected area), gap between pixels: 22 μm (all measures are close – but not identical – to the present BPIX sensor)
- **FPIX E+F**
 - Open p-stop
 - Different gap size (~ 30 and 50 μm)

Available substrates (all n- and p-type)

- FZ 320, 200, (120) μm
- mCz 200 μm
- Epi 100 (70), 50 μm
- FZ 200 μm , 2 metal layers (still to)