



宮崎大学  
University of Miyazaki



 Imaging Devices Laboratory

# Evaluation of SOI Pixel Detector with Charge Sensitive Amplifier Circuit for Event-Driven X-ray Readout

PIXEL2014 @ Niagara Falls, Canada 2014.09.01-05

Ayaki Takeda (Kyoto Univ.)

atakeda @cr.scphys.kyoto-u.ac.jp

T.G.Tsuru, T.Tanaka, H.Matsumura (Kyoto Univ.), Y.Arai (KEK/IPNS),  
S.Nakashima (JAXA), K.Mori, Y.Nishioka, R.Takenaka (Miyazaki Univ.),  
T.Kohmura (Tokyo Univ. of Scie.), S.Kawahito, K.Kagawa, K.Yasutomi,  
H.Kamehama, S.Sumeet (Shizuoka Univ./Imaging Devices Lab.),

and

SOIPIX Group.

# Outline

---

## - Introduction

-> SOI Pixel Detector for Future X-ray Astronomy (XRPIX)

## - XRPIX Design Description

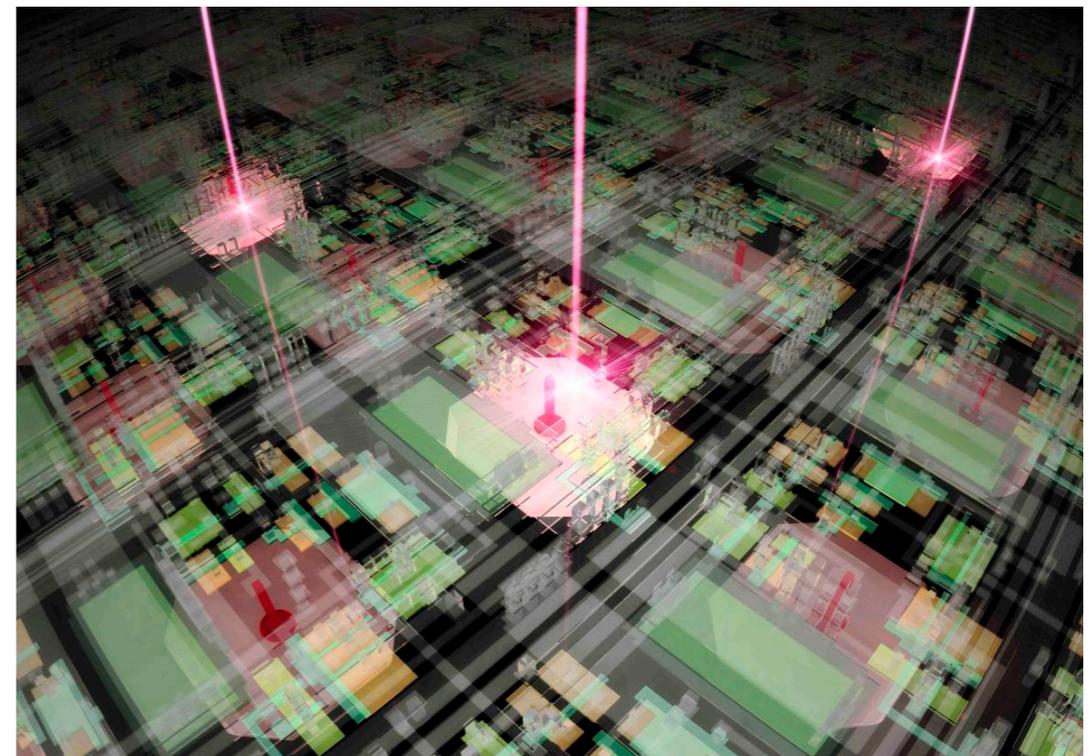
-> XRPIX2b : for Event-Driven Readout

-> XRPIX3b : for Pixel Circuit with Charge Sensitive Amplifier (CSA)

## - XRPIX Performance Tests

-> Evaluation of Event-Driven Readout and CSA Circuit

## - Summary



# Standard Imaging Spectrometer of modern X-ray astronomical satellites X-ray CCD

---

- Fano limited spectroscopy with the readout noise  $\sim 3 e^-$  (rms).
- Wide and fine imaging with the sensor size of  $\sim 20 - 30$  mm, pixel size of  $\sim 30 \mu\text{m}$  sq.
- High QE by BI and thick depletion ( $200 \mu\text{m}$  for ASTRO-H).

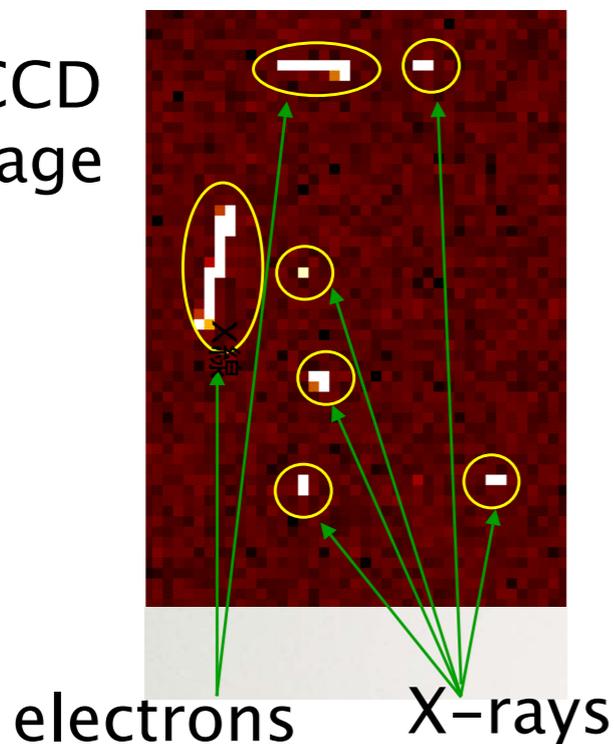
# Standard Imaging Spectrometer of modern X-ray astronomical satellites X-ray CCD

- Fano limited spectroscopy with the readout noise  $\sim 3 e^-$  (rms).
- Wide and fine imaging with the sensor size of  $\sim 20 - 30$  mm, pixel size of  $\sim 30 \mu\text{m}$  sq.
- High QE by BI and thick depletion ( $200 \mu\text{m}$  for ASTRO-H).

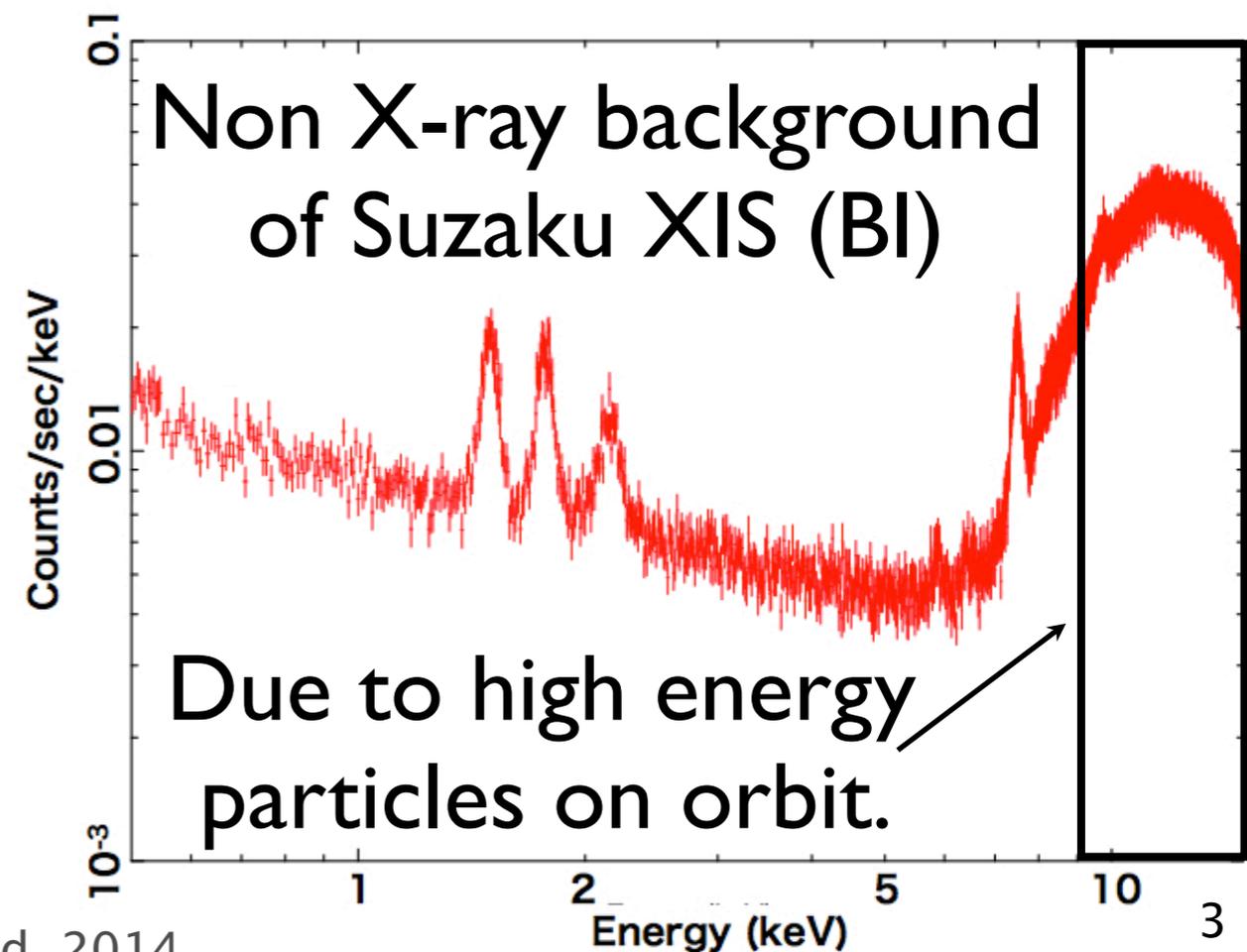
## However ...

- **Non X-ray background** above 10 keV is too high to study faint sources.
- **The time resolution** is too poor ( $\sim \text{sec}$ ) to make fast timing observation of time variable source.

X-ray CCD Raw Image



Particle : Track  
X-ray : One or adjacent pixels.



# SOI Pixel Detector for Future X-ray Astronomy

The performance required of a future X-ray astronomical satellite is the following ...

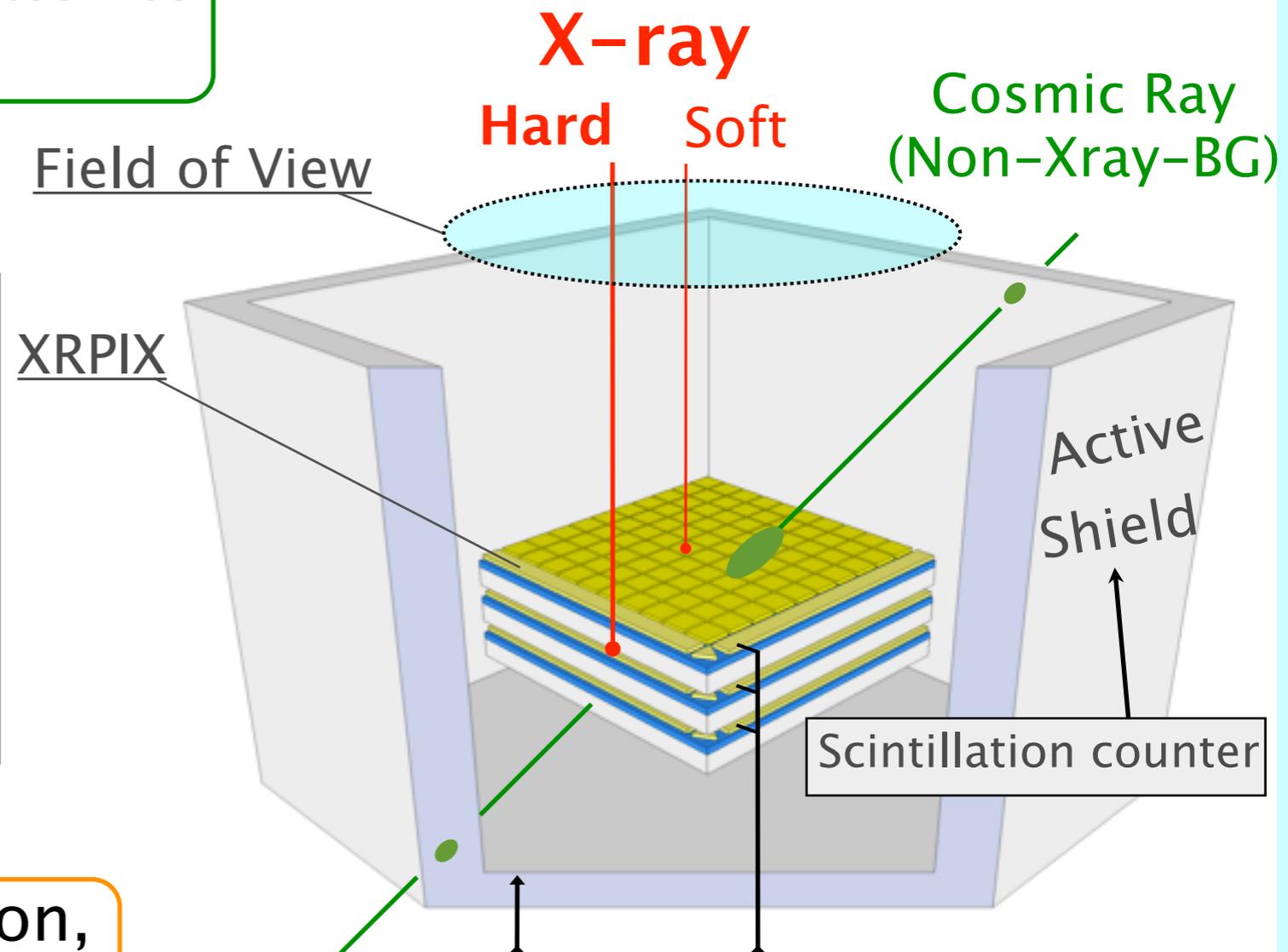
## Target Specification

- (1) FWHM  $\leq 140$  eV at 6 keV  
Readout Noise :  
req.  $\leq 10$  e<sup>-</sup> / goal  $\leq 3$  e<sup>-</sup>
- (2)  $< 100$   $\mu\text{m}$  pitch pixel
- (3)  $\sim 10$   $\mu\text{s}$  per event readout  
(Trigger, Direct Pixel Access)
- (4) Wide energy range : 0.3– 40 keV  
(Thick Depletion Stacks)

In order to achieve specification, we have been developing X-ray SOI Pixel Detector (XRPIX).

**XRPIX has self-trigger function !**  
**-> Realization of Event-Driven**

## X-ray SOIPIX with Active Shield



## Onboard Processor

- Anti-coincidence (NXB rejection)
- Hit-pattern Selection (NXB rejection)
- Direct Pixel Access (X-ray Readout)

# Introduction of SOI Pixel Detector

- A monolithic pixel detector with Silicon-on-Insulator (SOI) CMOS Technology -> 0.2  $\mu\text{m}$  fully-depleted (FD) - SOI pixel process
- SOI Pixel Detector (SOIPIX) : Processed by LAPIS Semi. Co., Ltd.

## SOIPIX Advantages

- No mechanical bump bonding
- > High Density, Low Parasitic Capacitance, High Sensitivity
- Standard CMOS circuit can be built
- Based on industrial standard technology

## Basic Components

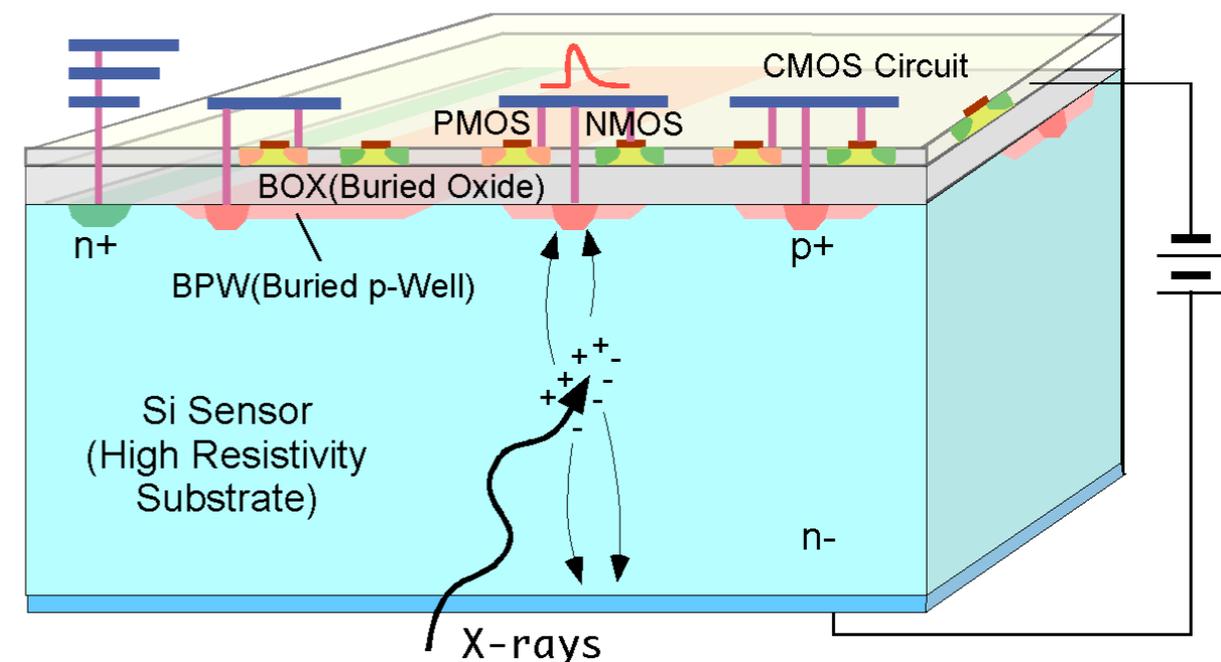
Circuit Layer : ~40 nm  
Buried Oxide (BOX) : 200 nm  
Sensor Layer : 100 - 725  $\mu\text{m}$

## SOI Pixel Process

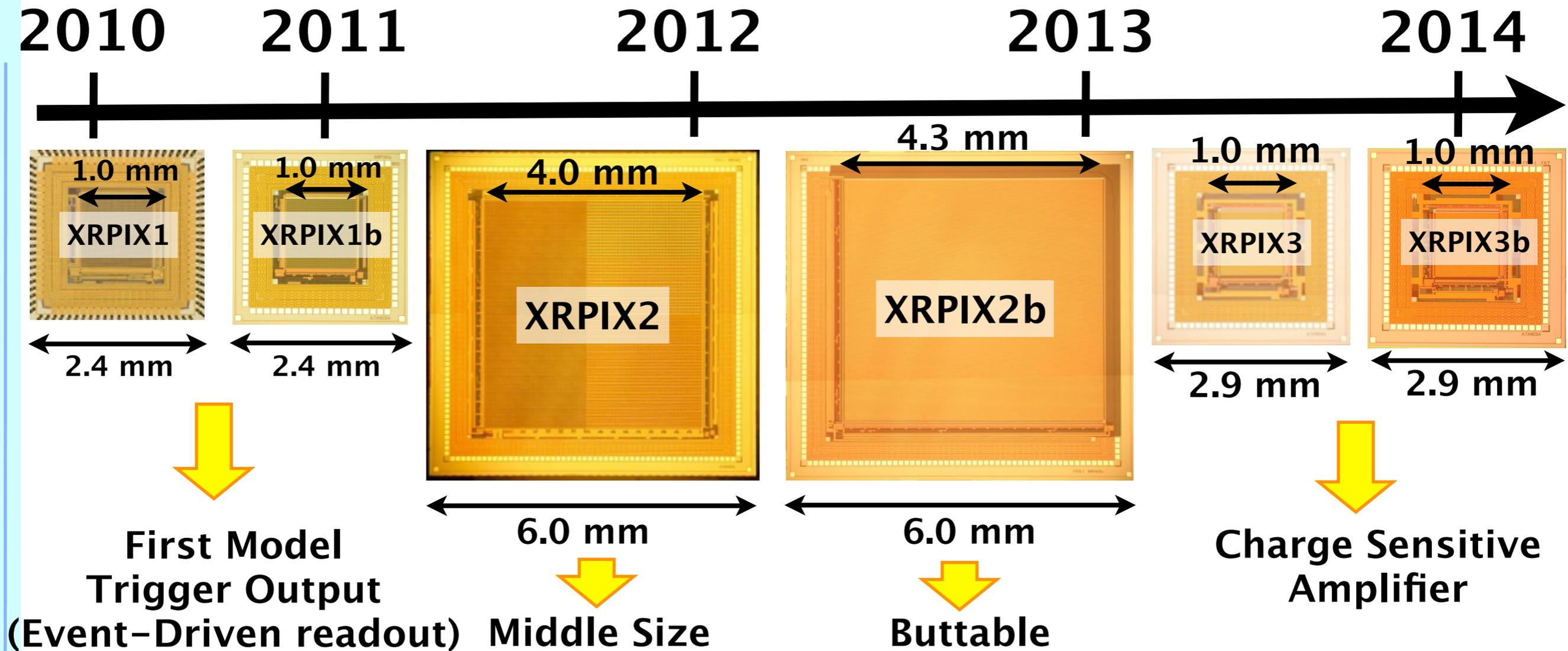
New Process to make pixel detector with SOI technology joint development with LAPIS Semi. Co., Ltd.

## Our group presentations:

Miho Yamada (1st day),  
Makoto Motoyoshi (4th day)

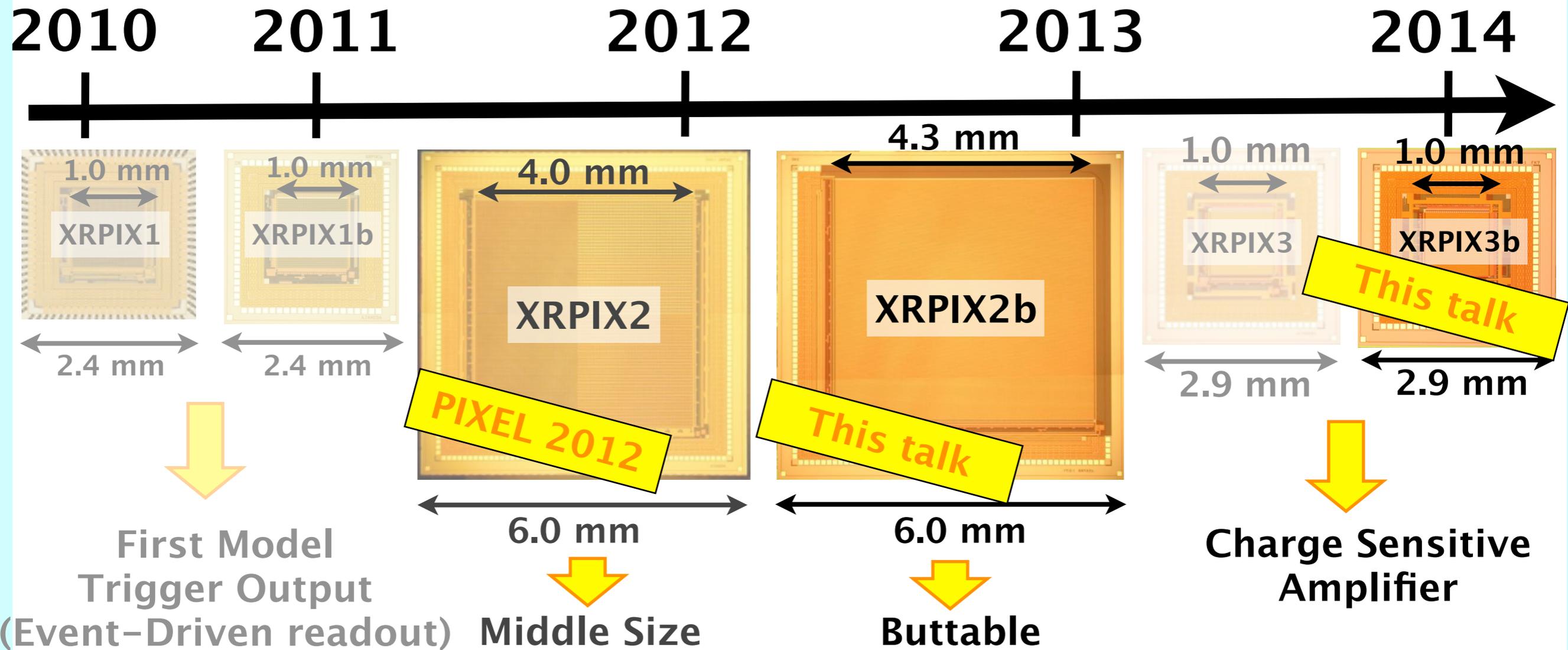


# XRPIX Series



- The XRPIX series has designed six devices: XRPIX1/1b/2/2b/3/3b.
- > The spectroscopic performance and event-driven readout are tested and improved.

# XRPIX Series



## PIXEL 2012

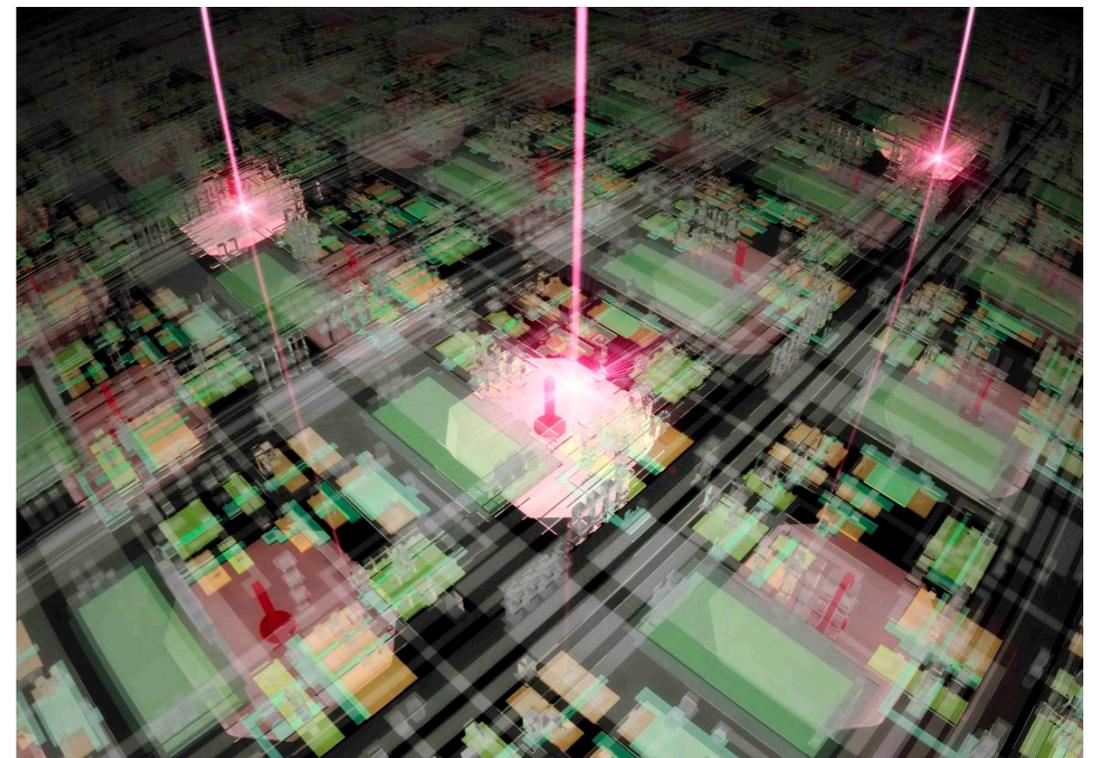
XRPIX2 : Reported by S.Nakashima

## PIXEL 2014

XRPIX2b : for Event-Driven Readout

XRPIX3b : for CSA pixel circuit

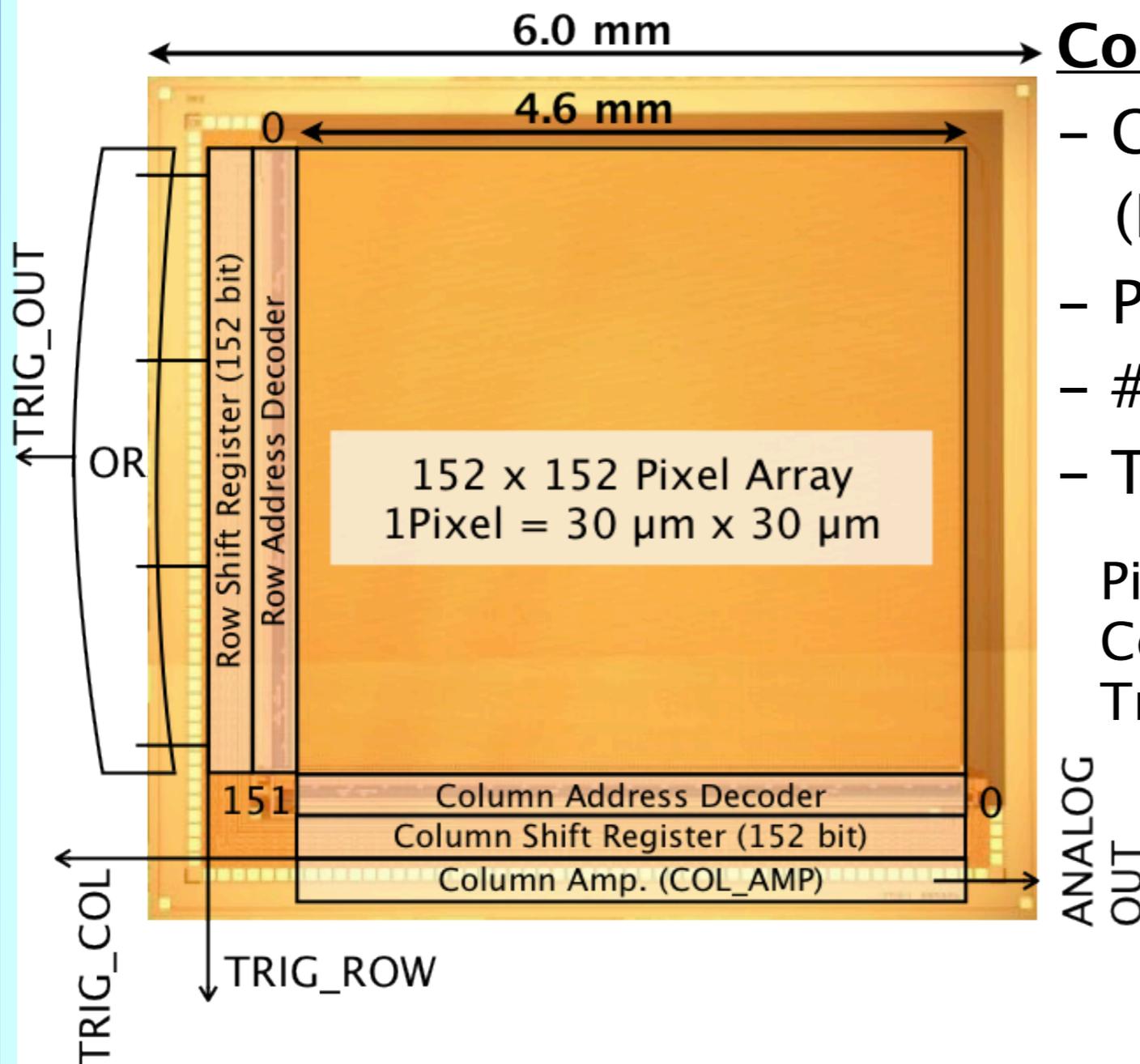
# Evaluation of Event-Driven Readout



© Rey.Hori

# Design Specification : XRPIX2b

- Optimization of a pixel design / Confirmation of uniformity
  - > It is based on the design of XRPIX1/1b/2.



## Components

- Chip size : 6.0 mm sq.  
(Effective area : ~ 4.6 mm sq.)
- Pixel size : 30 μm sq.
- # of pixel : 152 x 152 (~ 23k)
- Thickness of sensor layer : 260 μm

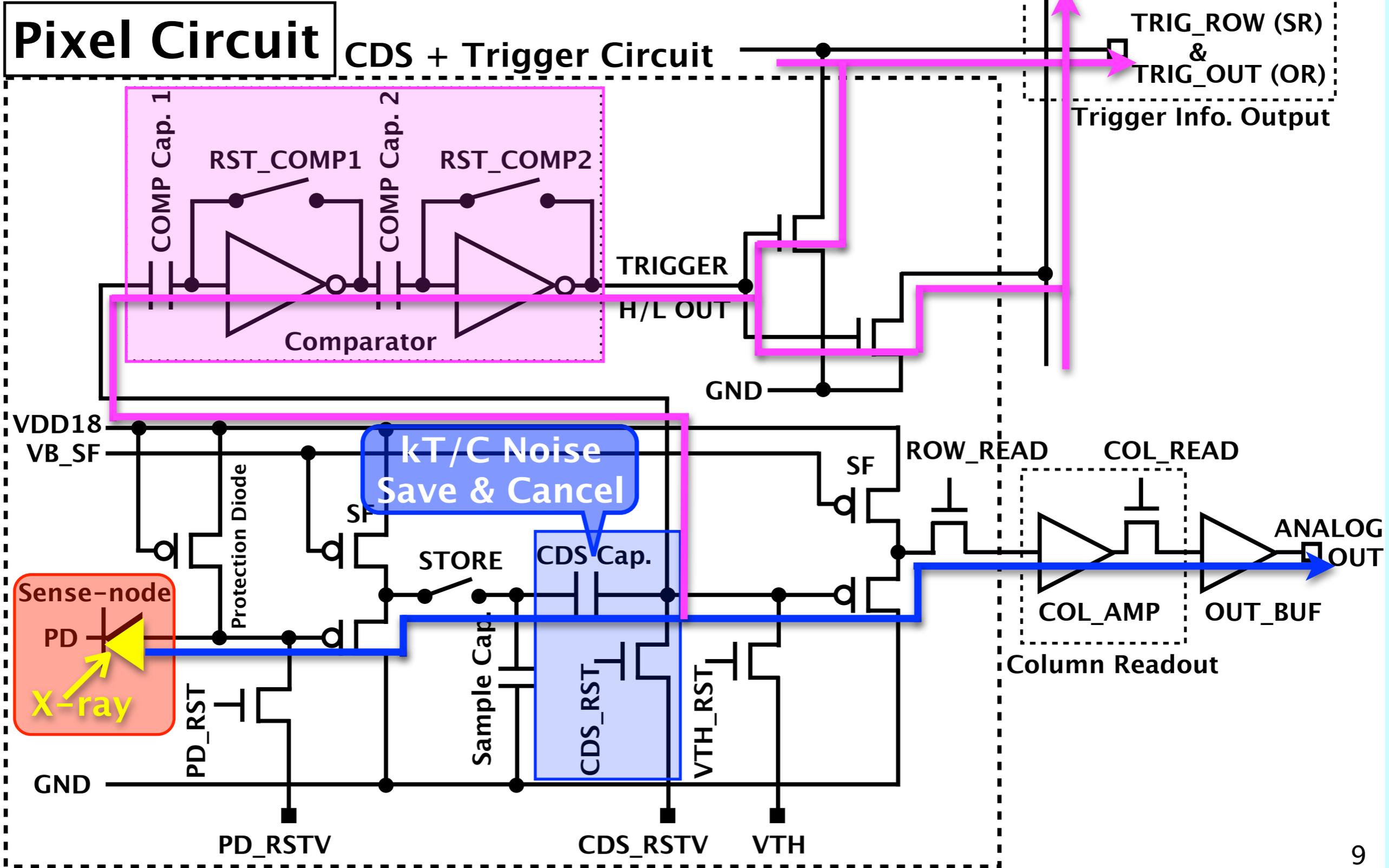
Pixel Circuit :

Correlated Double Sampling (CDS),  
Trigger information output function.

# Design Specification : Pixel Circuit

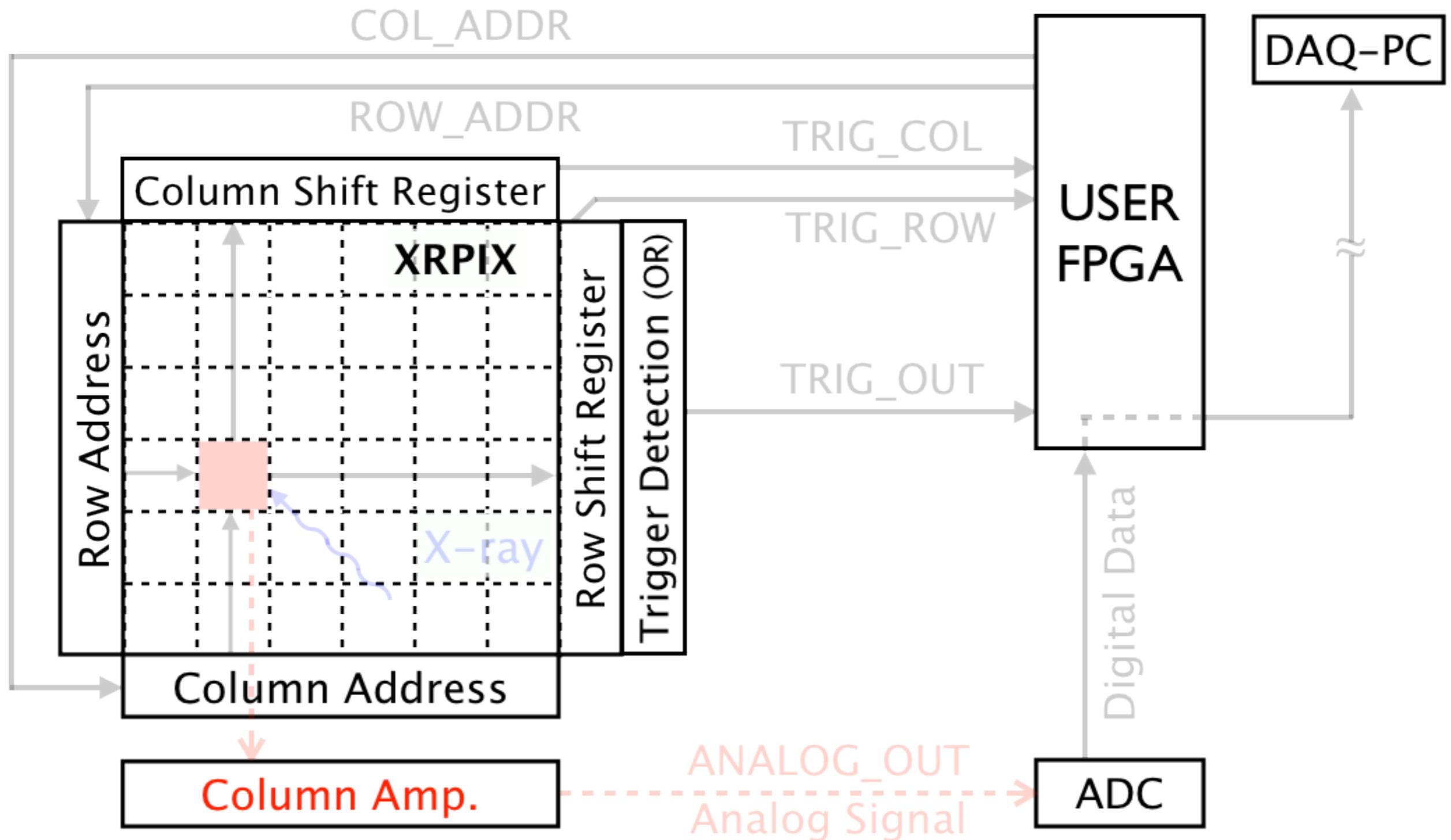
Blue : Sensor Signal (with CDS)

Magenta : Trigger Signal



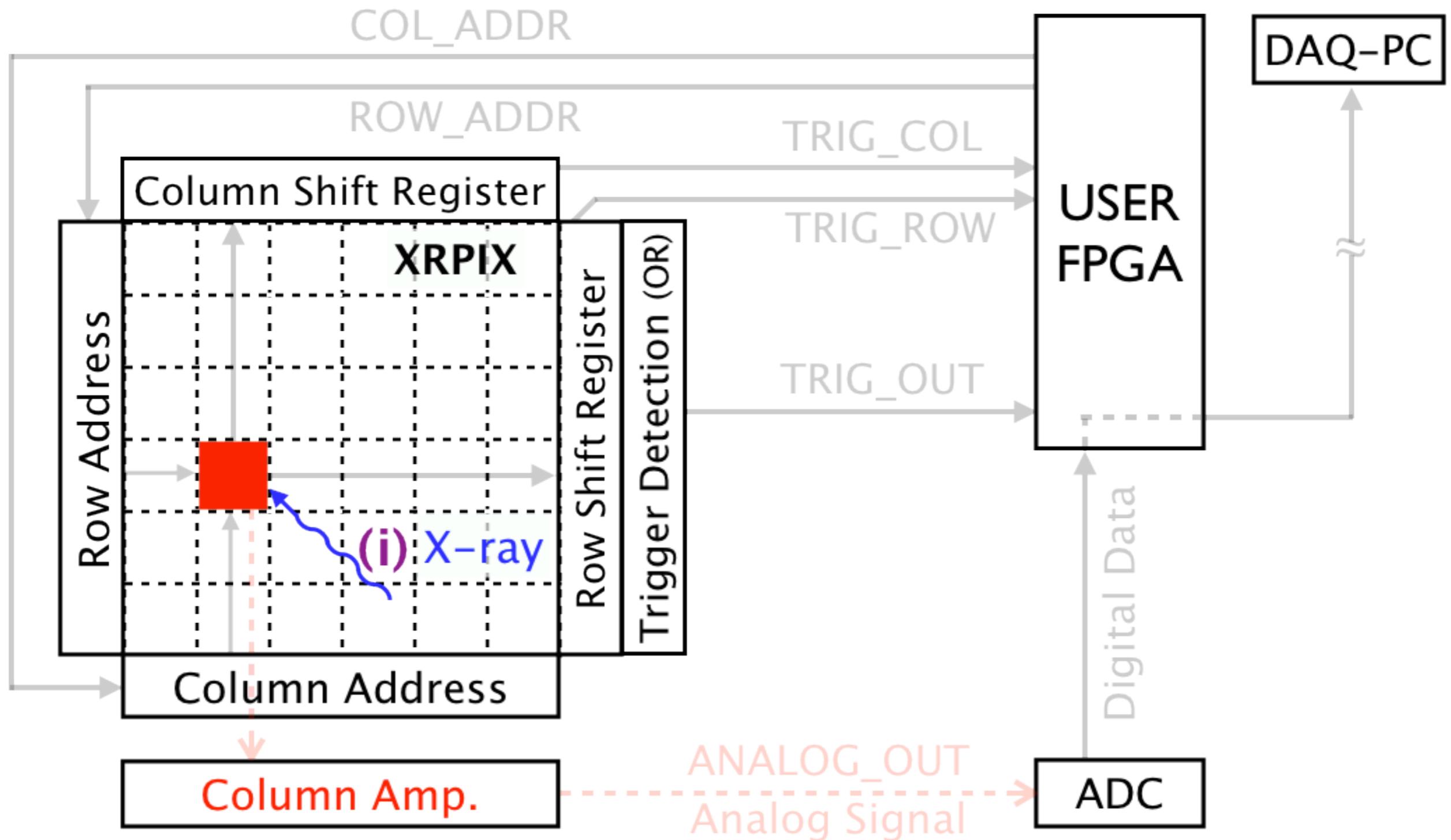
# Event-Driven Readout Mode

- The following figure show the flow chart.



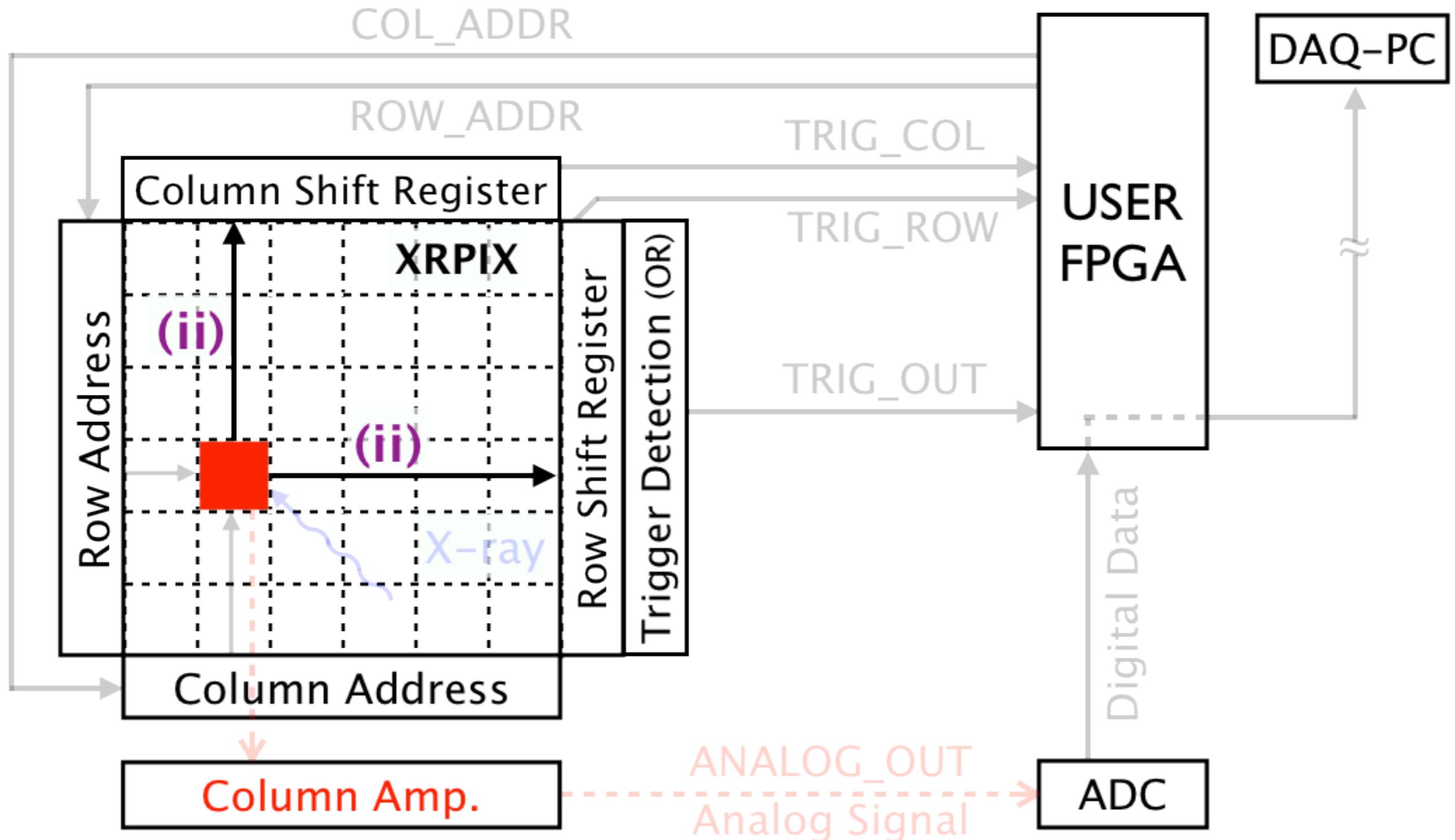
# Event-Driven Readout Mode

( i ) X-ray signal is detected by a pixel.



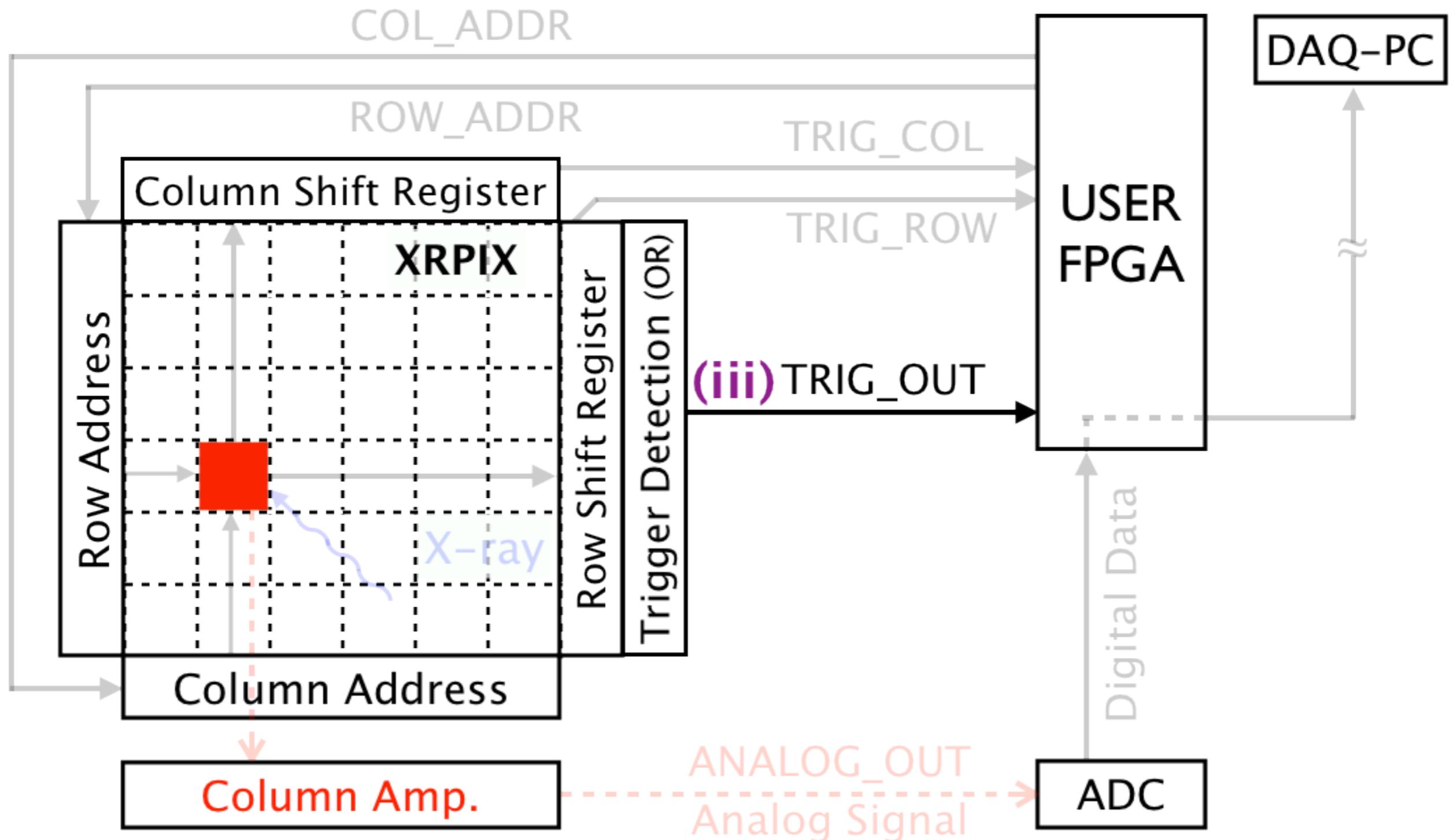
# Event-Driven Readout Mode

- ( ii ) If the X-ray signal exceeds a threshold voltage, trigger signals are transferred to row and column direction.



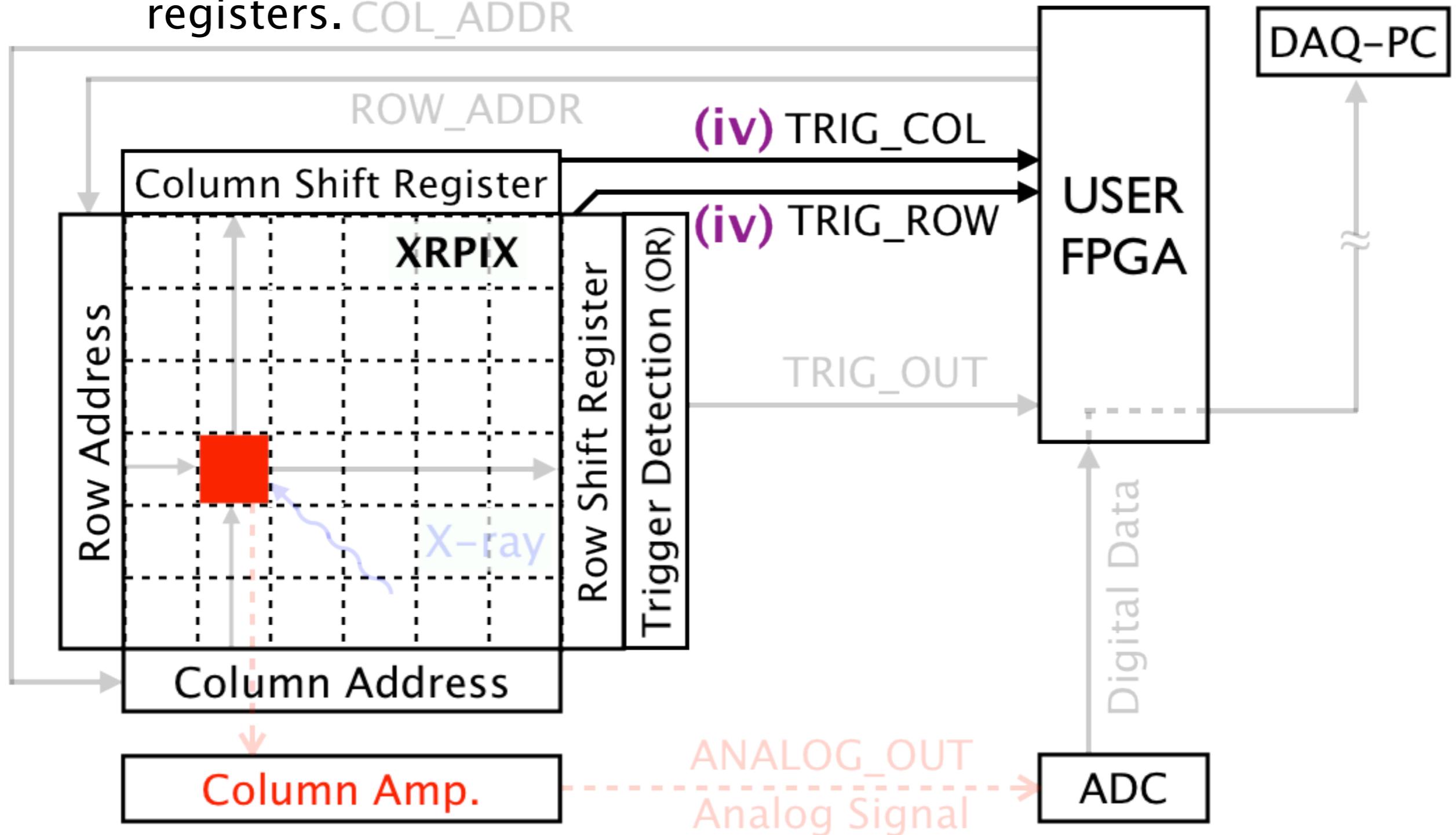
# Event-Driven Readout Mode

( iii ) OR'ed signal (TRIG\_OUT) of the trigger is generated.



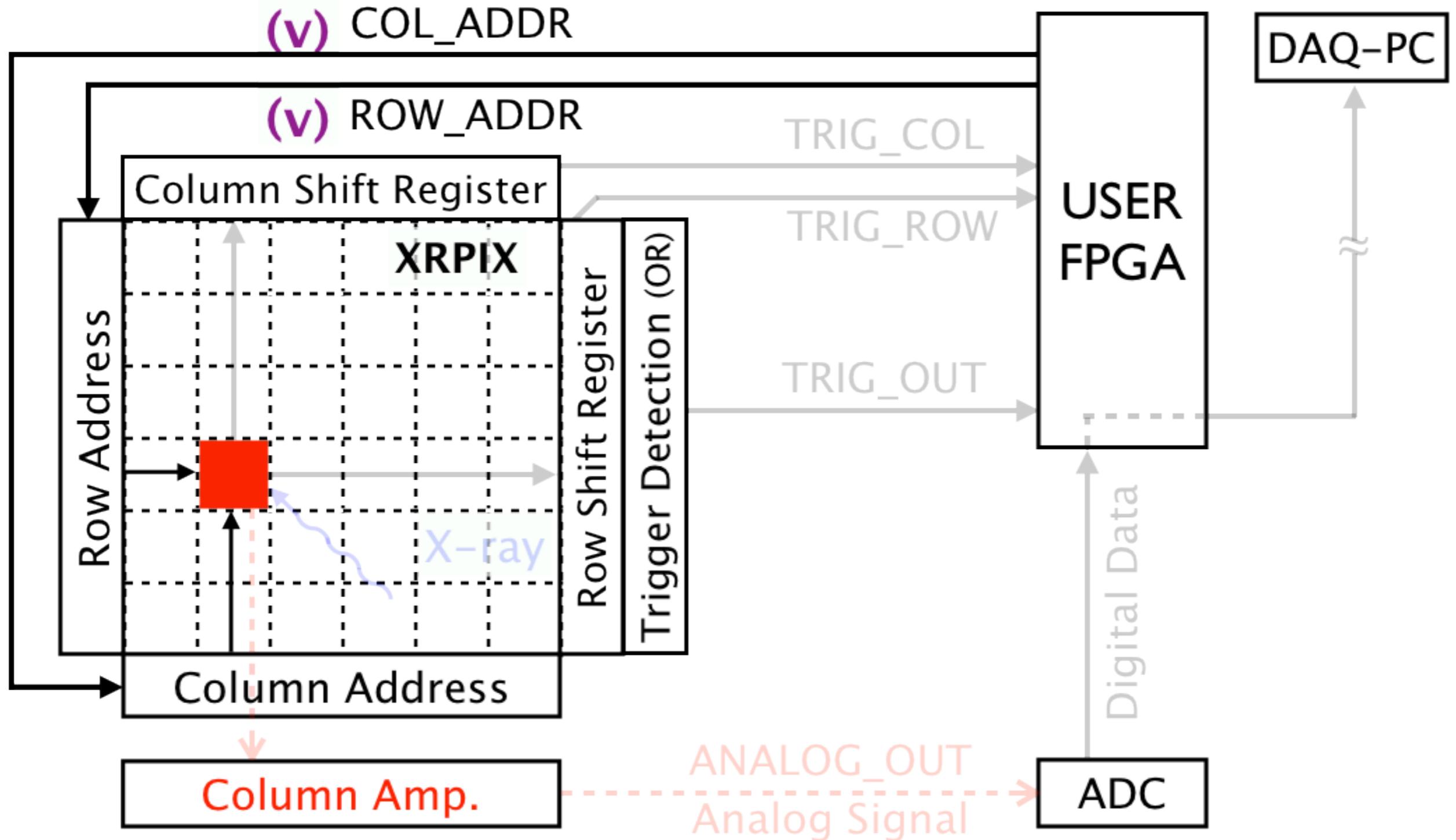
# Event-Driven Readout Mode

- (iv) By receiving the TRIG\_OUT signal, USER-FPGA start to read the hit address information from the row and column shift registers. COL\_ADDR



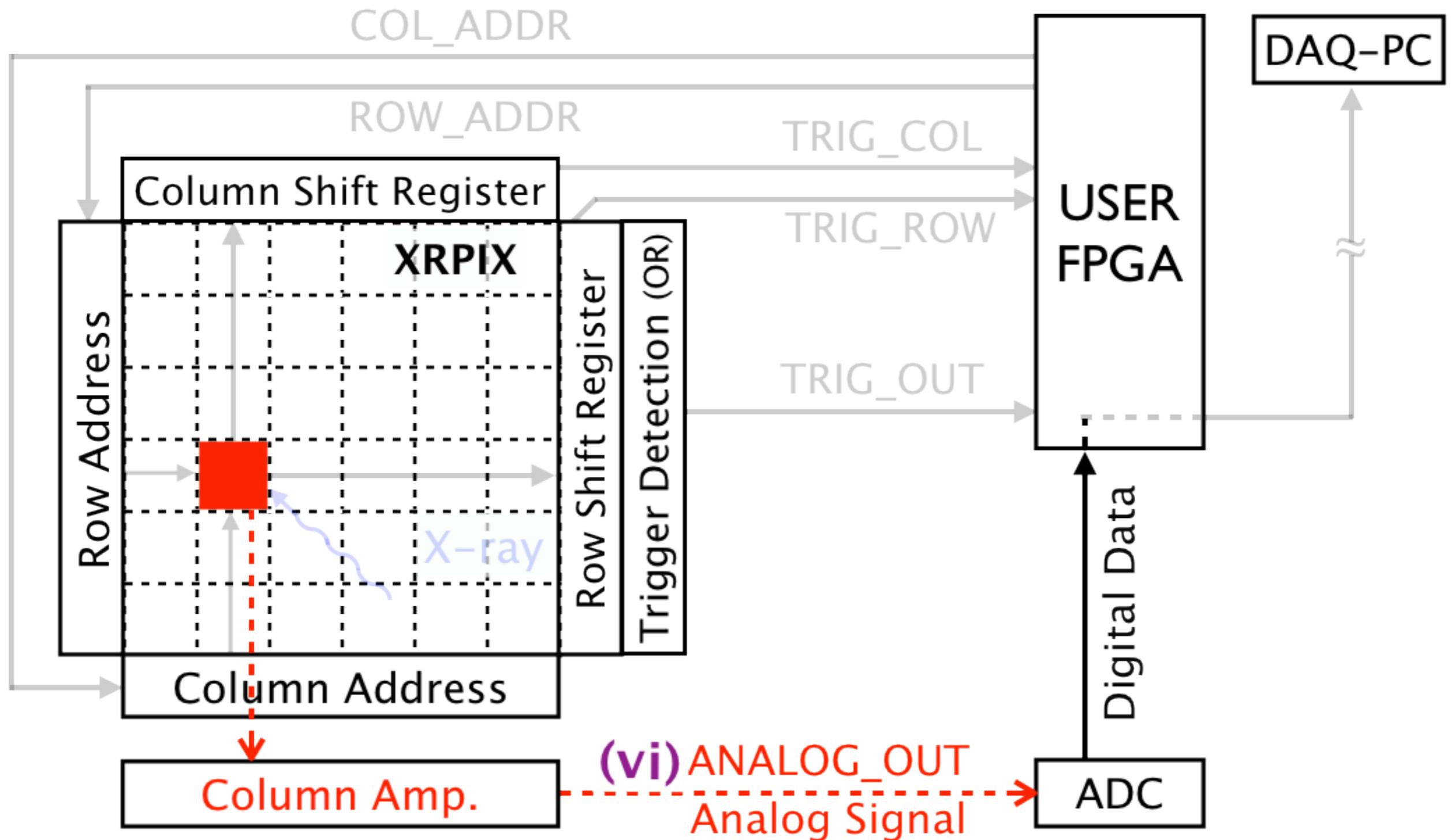
# Event-Driven Readout Mode

(v) The USER-FPGA accesses the hit pixel directly by asserting the obtained address.



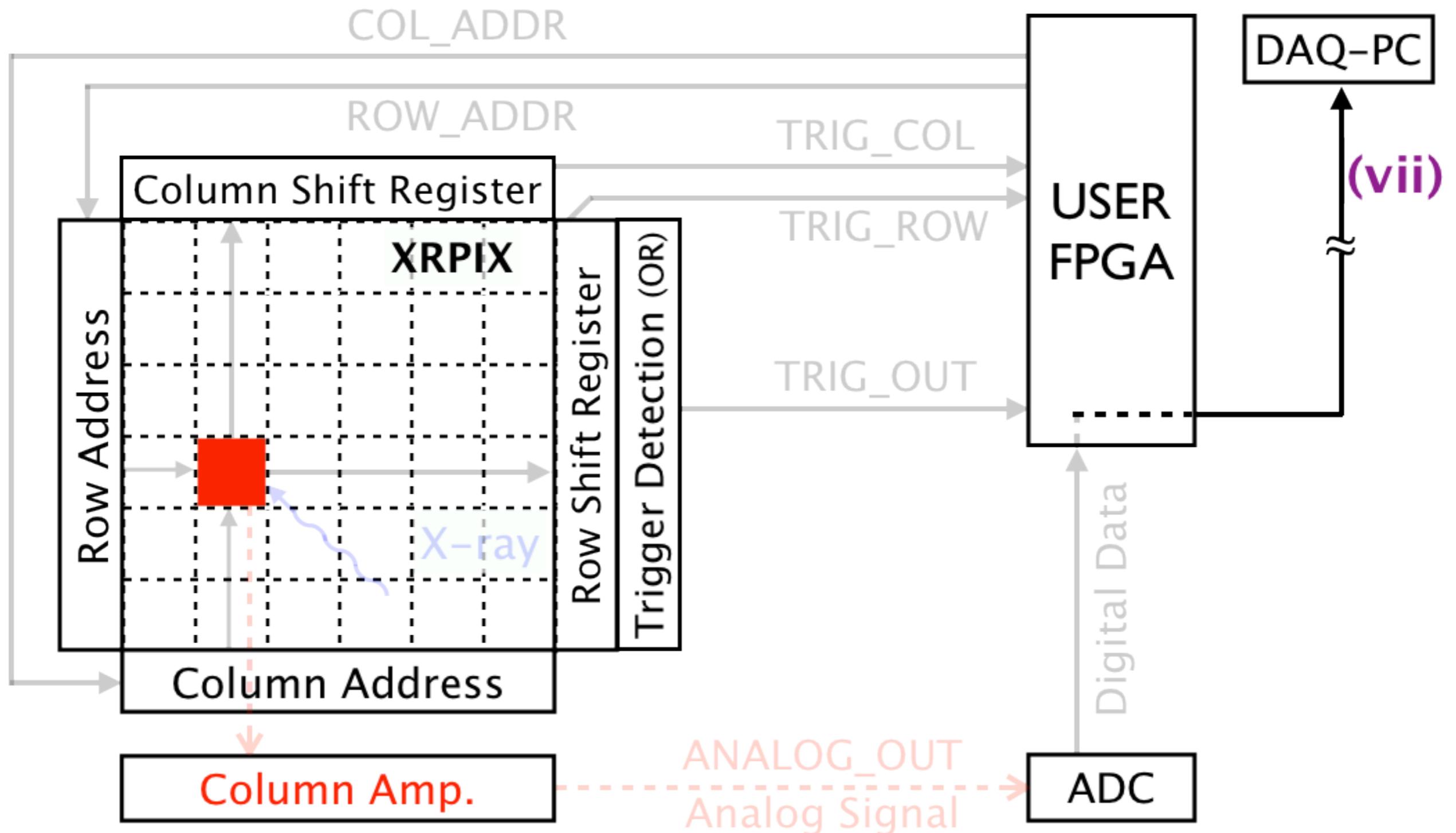
# Event-Driven Readout Mode

- (vi) The USER-FPGA reads out the analog voltage (signal and pedestal levels) through the ADC.



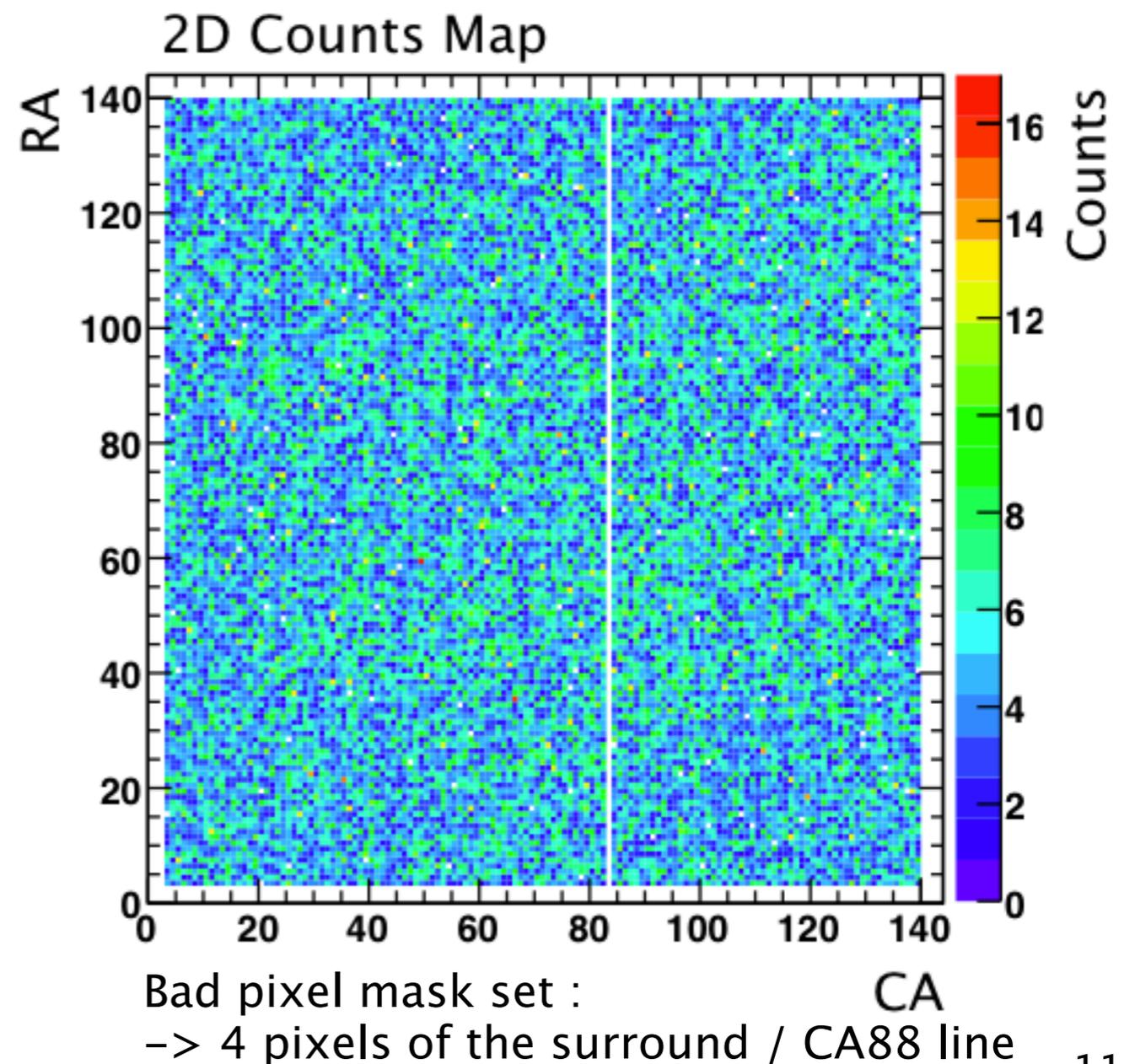
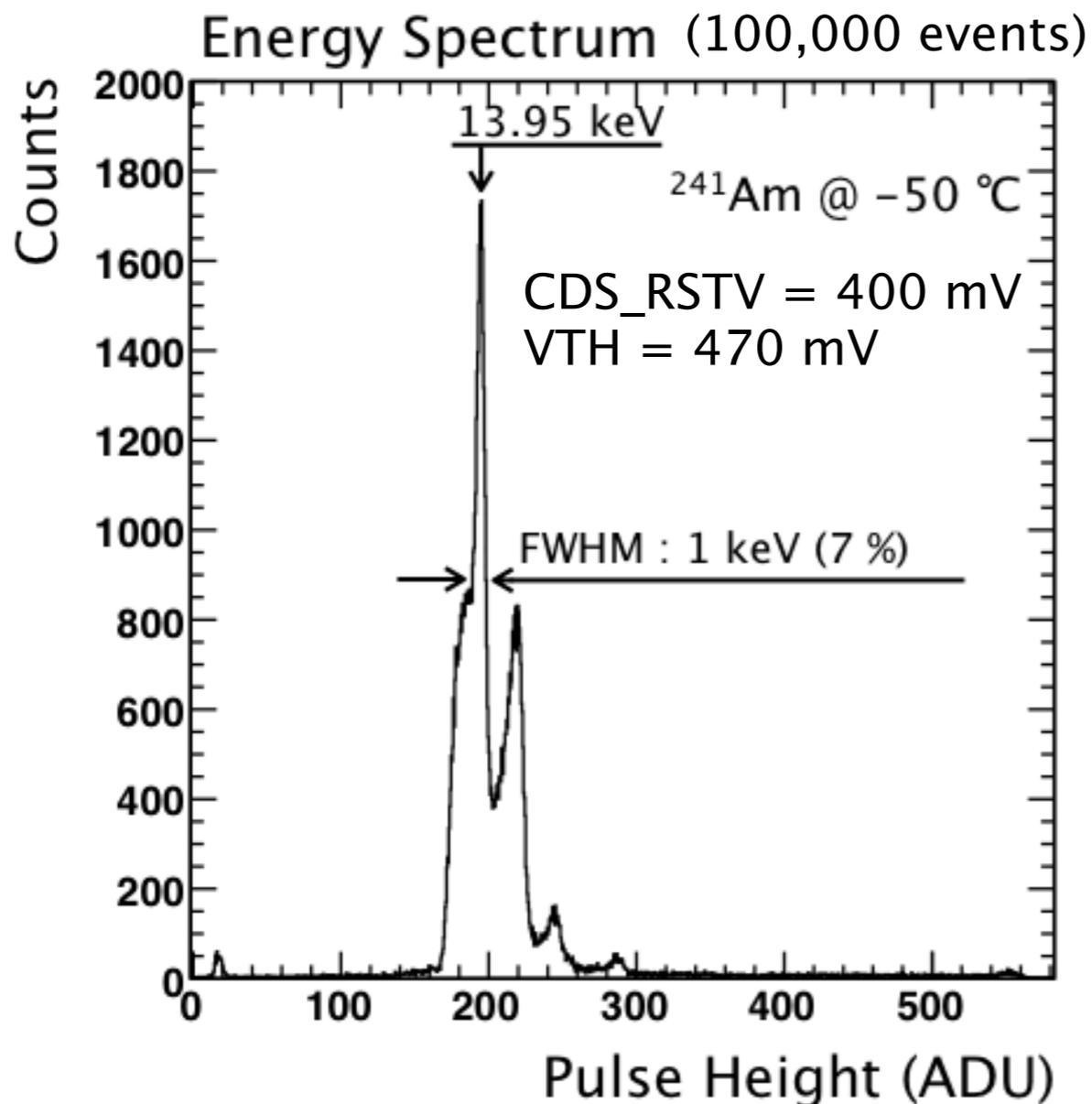
# Event-Driven Readout Mode

(vii) Finally, the obtained digital data is transmitted to the DAQ-PC.



# Event-Driven Spectrum by XRPIX2b

- X-ray spectrum by event-driven readout mode.
  - > Capacity of event rate : ~1 kHz.
- FWHM : 1 keV (7 %) @ 13.95 keV
  - > This is not good compared with the frame readout mode. (650 eV at FWHM at the same line)

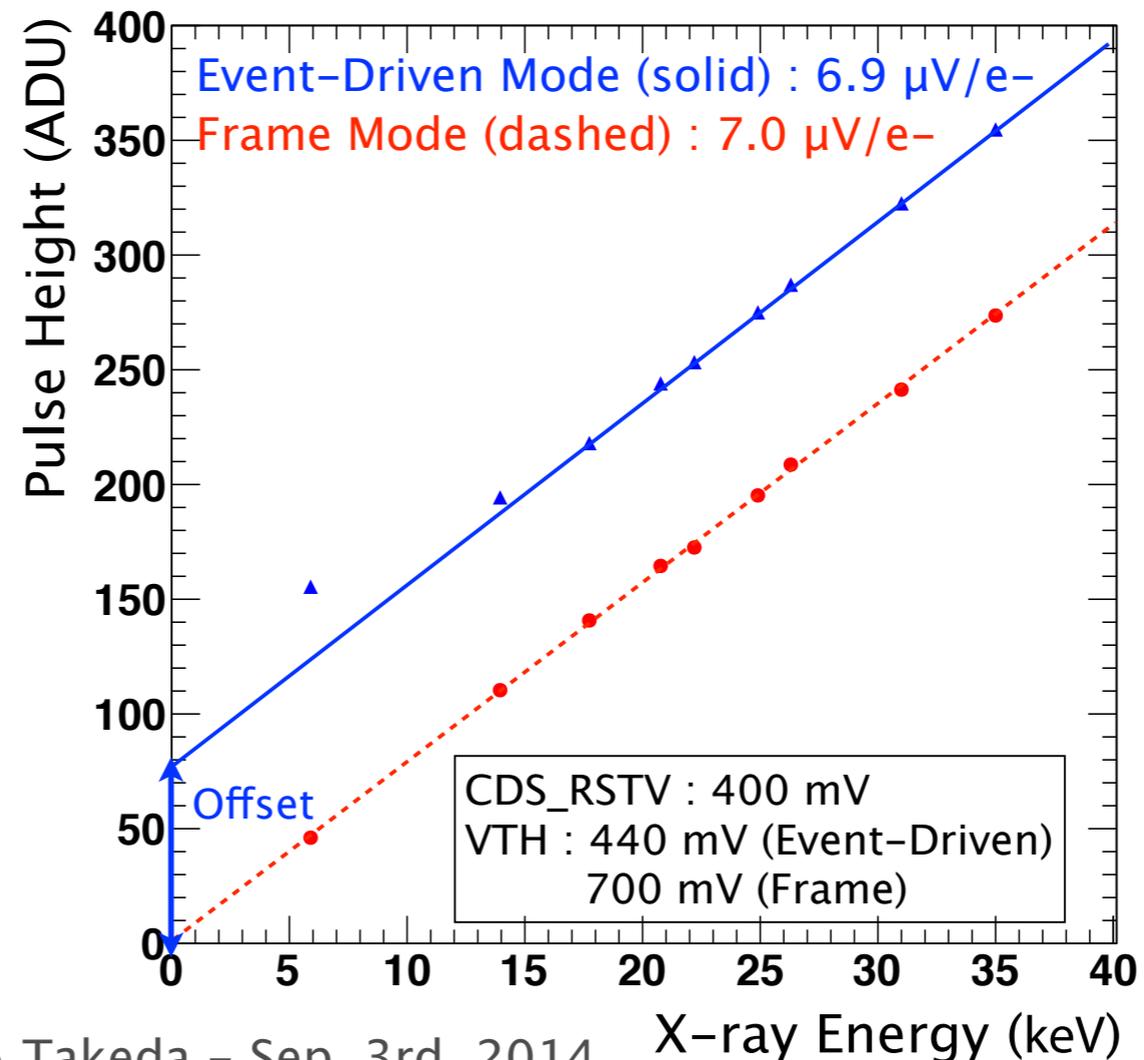


# Event-Driven Calibration

– Calibration plot using the  $^{55}\text{Fe}$ ,  $^{241}\text{Am}$ ,  $^{109}\text{Cd}$ , and  $^{133}\text{Ba}$  X-ray lines.

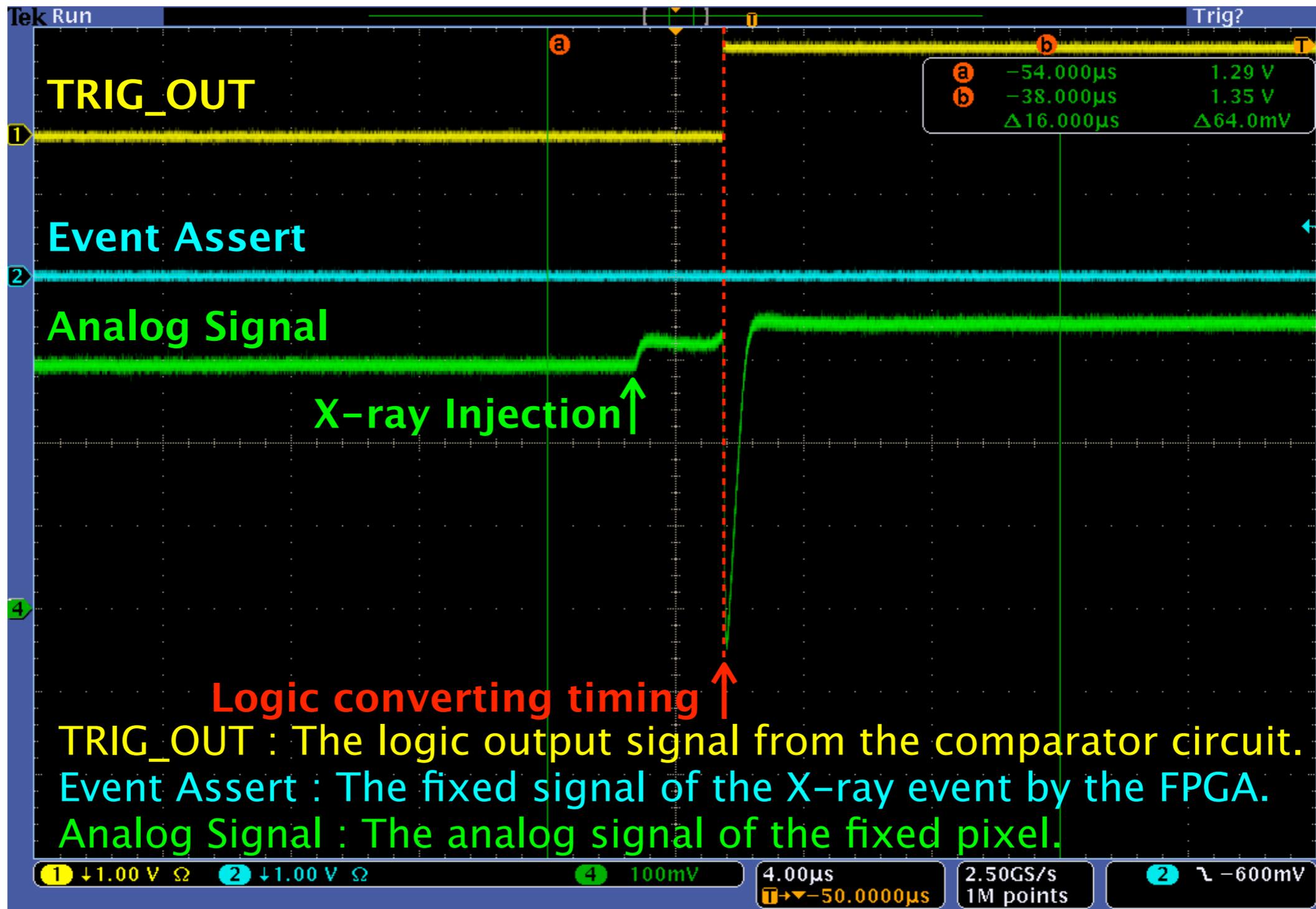
## Two problems

1. The plot has an offset of  $\sim 80$  ADU (i.e.  $\sim 20$  mV).
  2. The pulse height of the output shifts from linearity at low energy.
    - > In this case, 5.9 keV of  $^{55}\text{Fe}$  line is clearly shifted from the fitting line.
- These differences are caused by the operation of the comparator circuit.  
– It is necessary to investigate these causes and to understand the phenomena.



# What happens by X-ray injection?

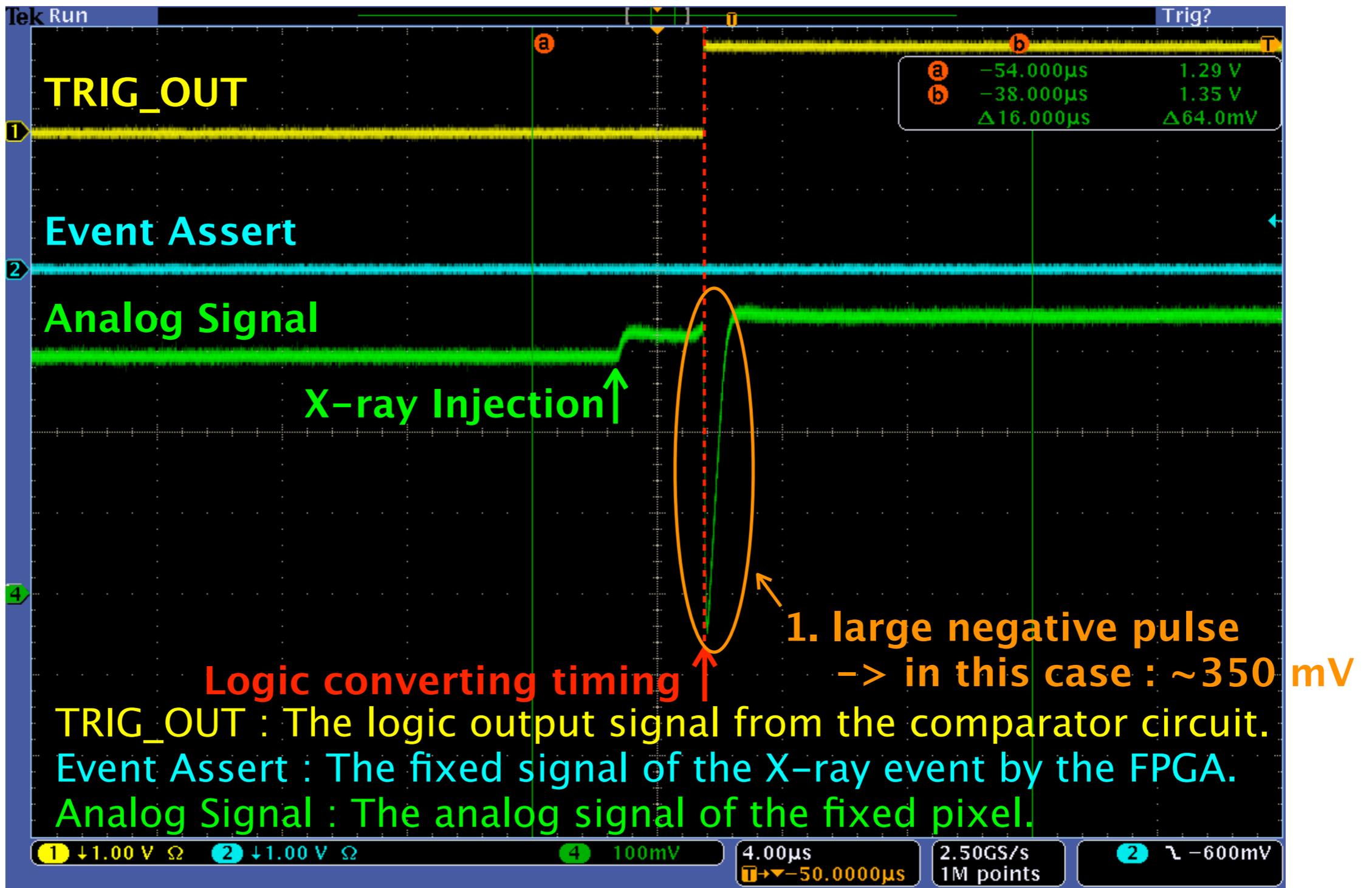
- The waveform of an oscilloscope when X-rays enter ( $^{109}\text{Cd}$  : 22.2 keV).  
-> The analog signal has 4 problems.



**Logic converting timing** ↑  
TRIG\_OUT : The logic output signal from the comparator circuit.  
Event Assert : The fixed signal of the X-ray event by the FPGA.  
Analog Signal : The analog signal of the fixed pixel.

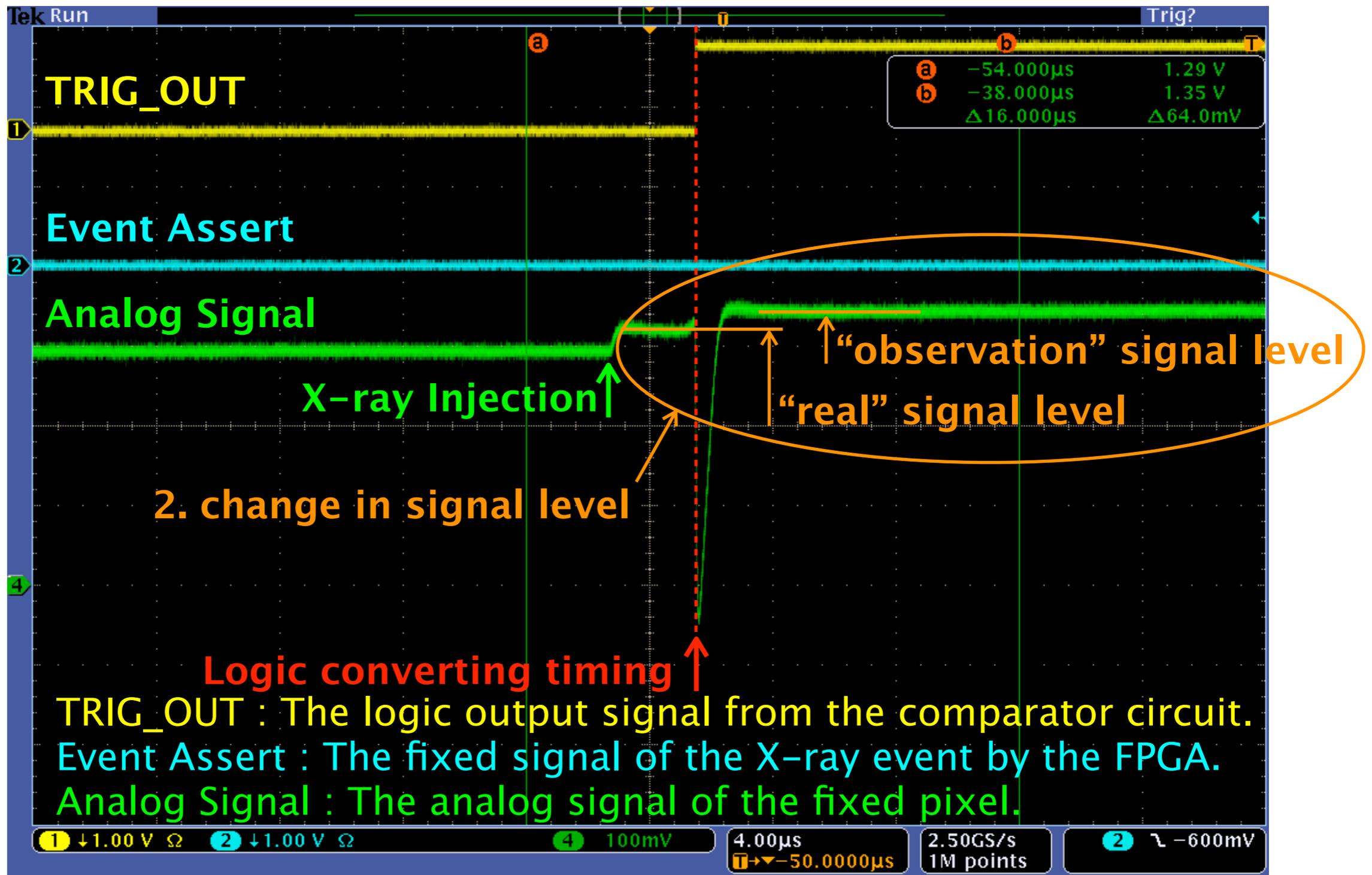
# What happens by X-ray injection?

- The waveform of an oscilloscope when X-rays enter ( $^{109}\text{Cd}$  : 22.2 keV).  
-> The analog signal has 4 problems.



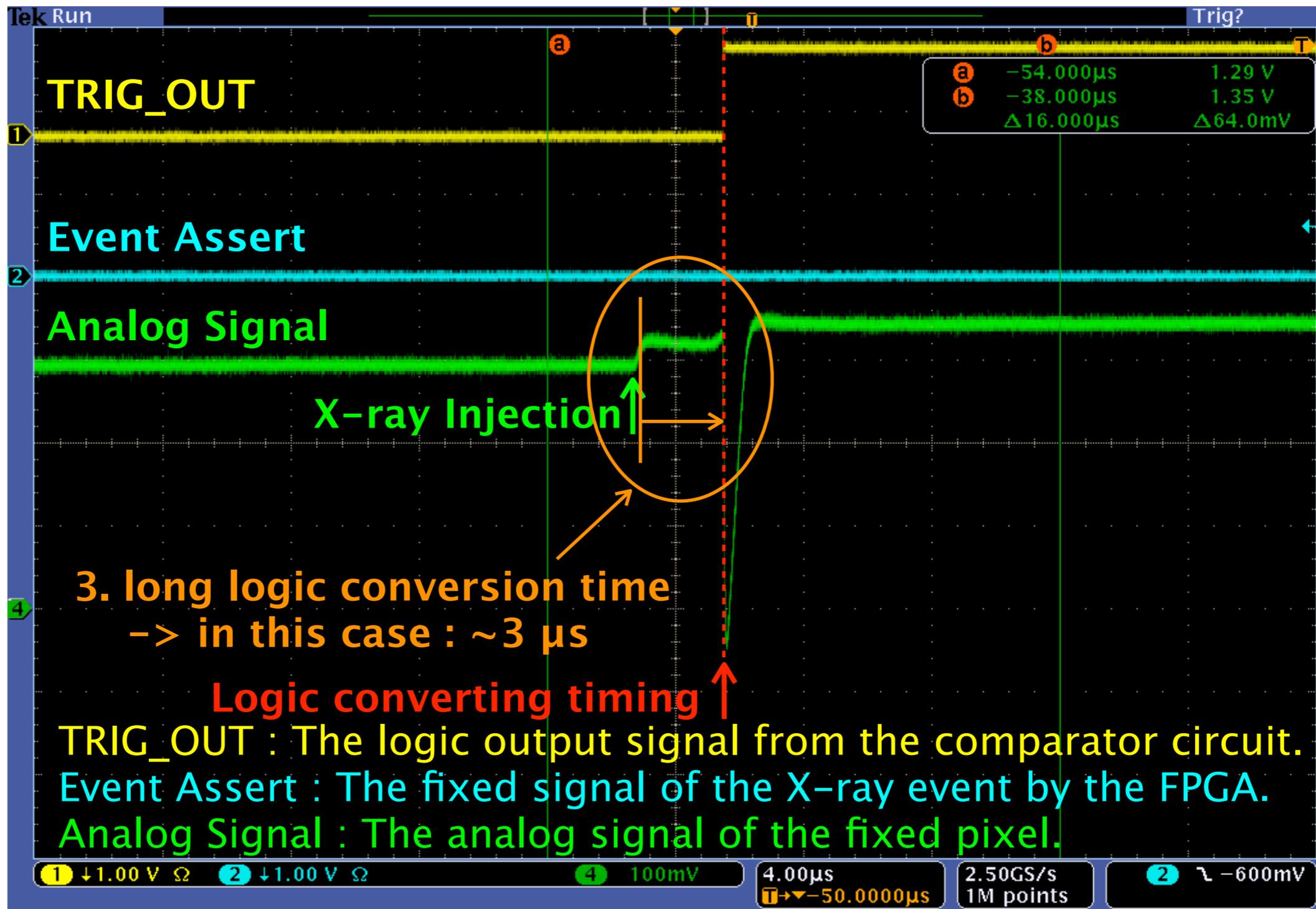
# What happens by X-ray injection?

- The waveform of an oscilloscope when X-rays enter ( $^{109}\text{Cd}$  : 22.2 keV).
- > The analog signal has 4 problems.



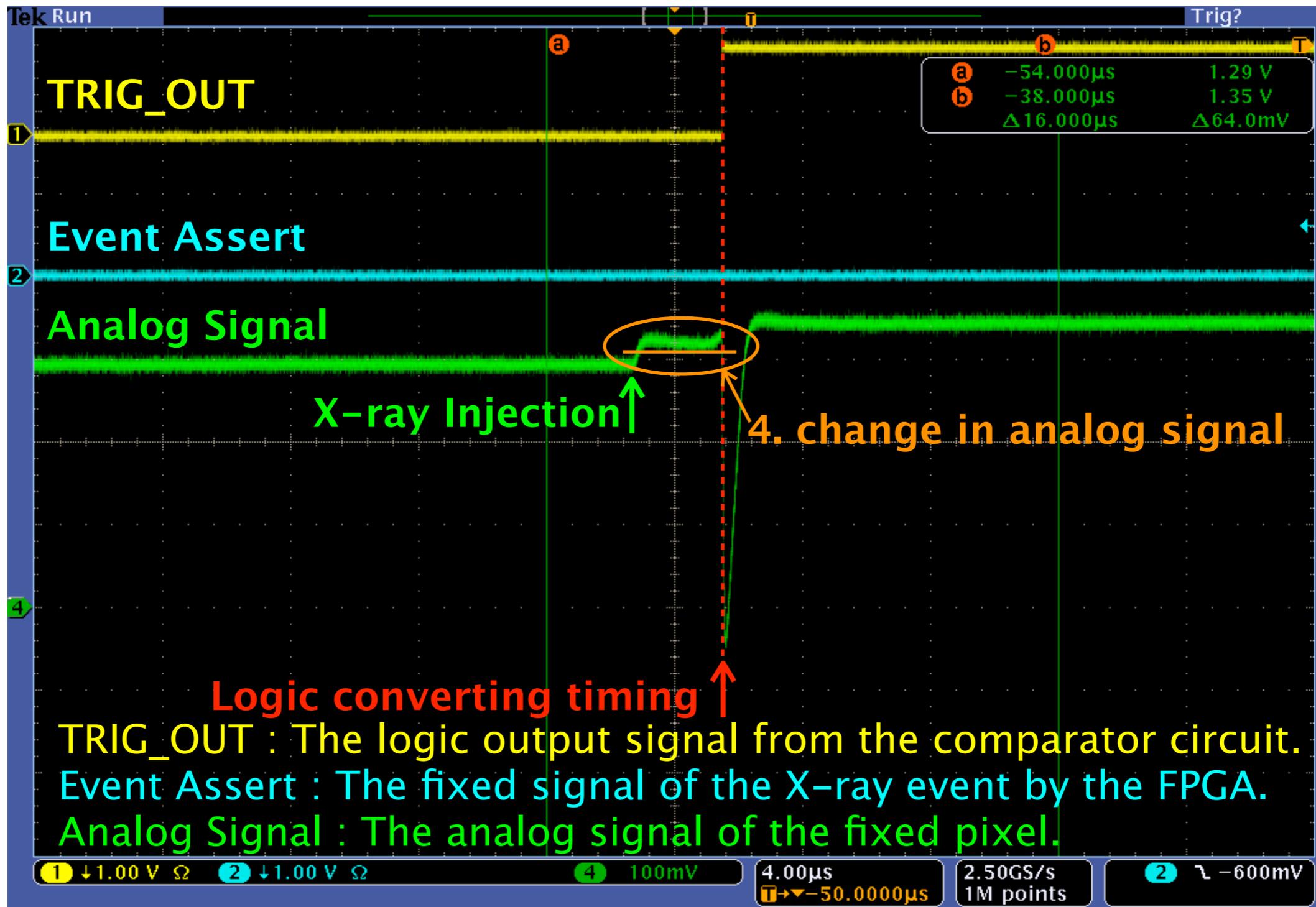
# What happens by X-ray injection?

- The waveform of an oscilloscope when X-rays enter ( $^{109}\text{Cd}$  : 22.2 keV).  
-> The analog signal has 4 problems.



# What happens by X-ray injection?

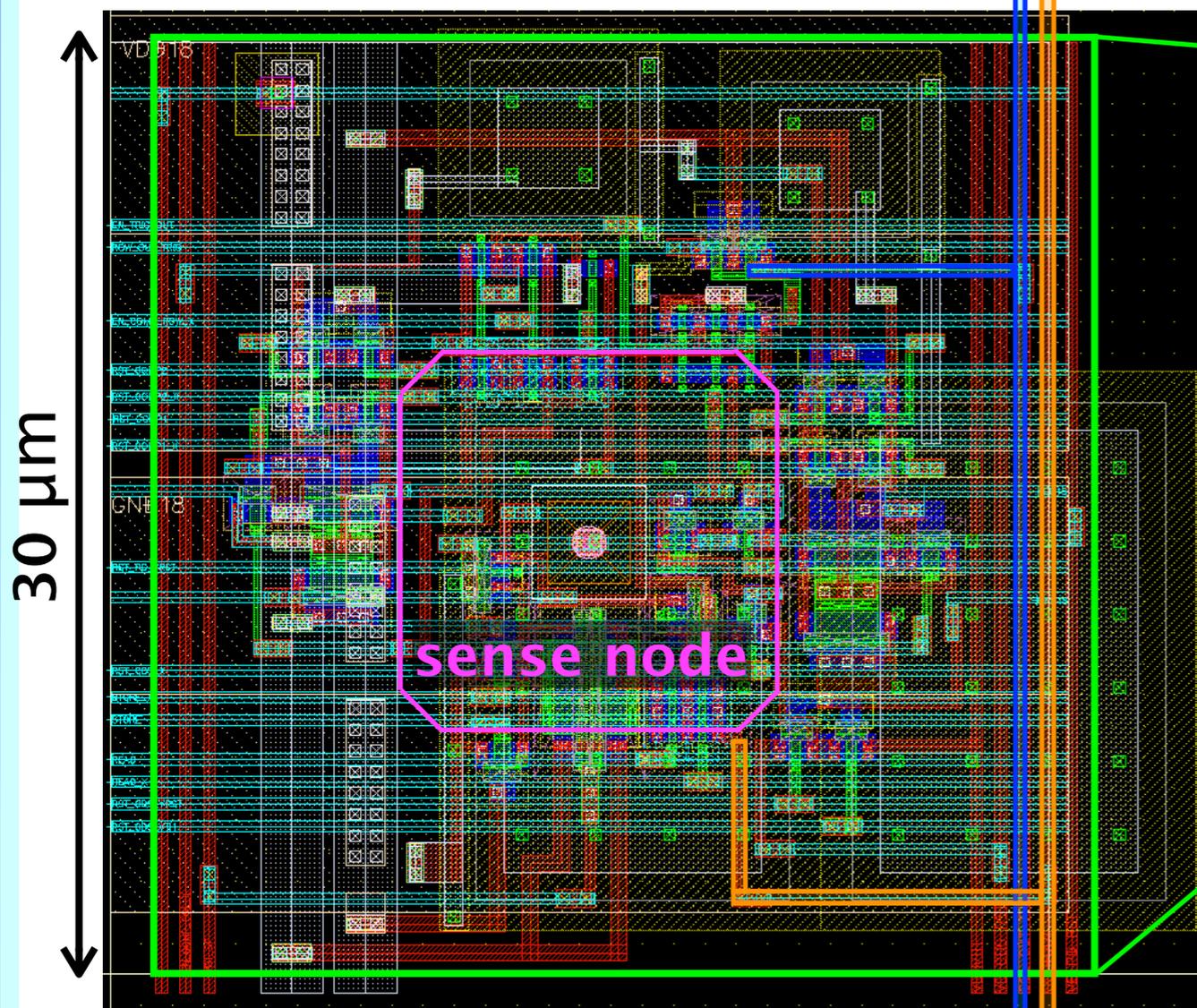
- The waveform of an oscilloscope when X-rays enter ( $^{109}\text{Cd}$  : 22.2 keV).  
-> The analog signal has 4 problems.



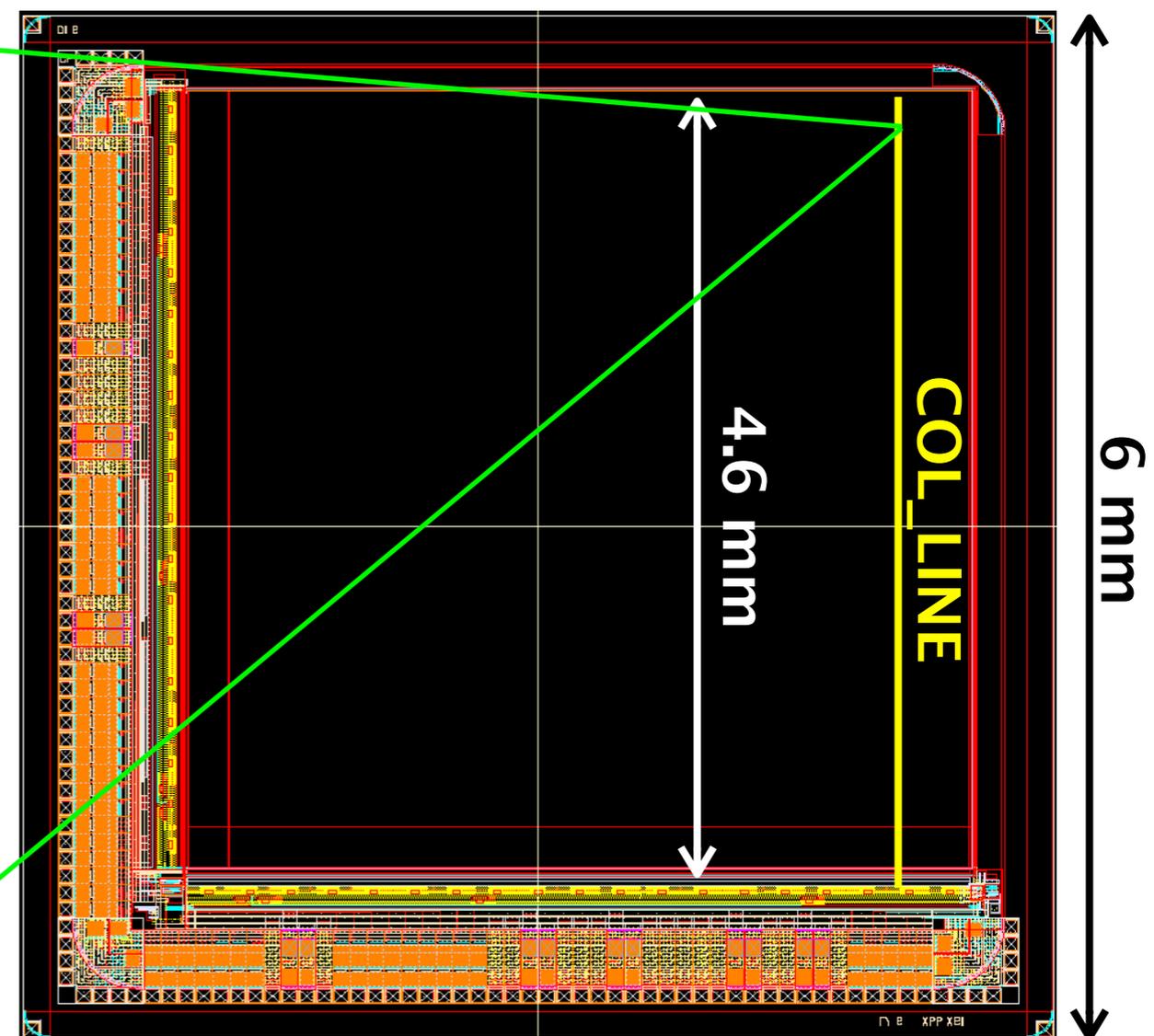
# 1. Reason for Negative Pulse

- Wiring of an analog signal line (COL\_OUT) and a trigger signal (COL\_TRIG\_OUT) adjoined each other with the pixel layout. (Distance :  $0.4\ \mu\text{m}$ , Length :  $4.6\ \text{mm}$ )
  - > This has large parasitic capacitance by wiring ( $\sim 250\ \text{fF}$ ).
- This is the phenomenon of appearing only when a pixel is specified and observed.
  - > It has checked also by HSpice simulation.

COL\_TRIG\_OUT → ← COL\_OUT(Analog Signal)



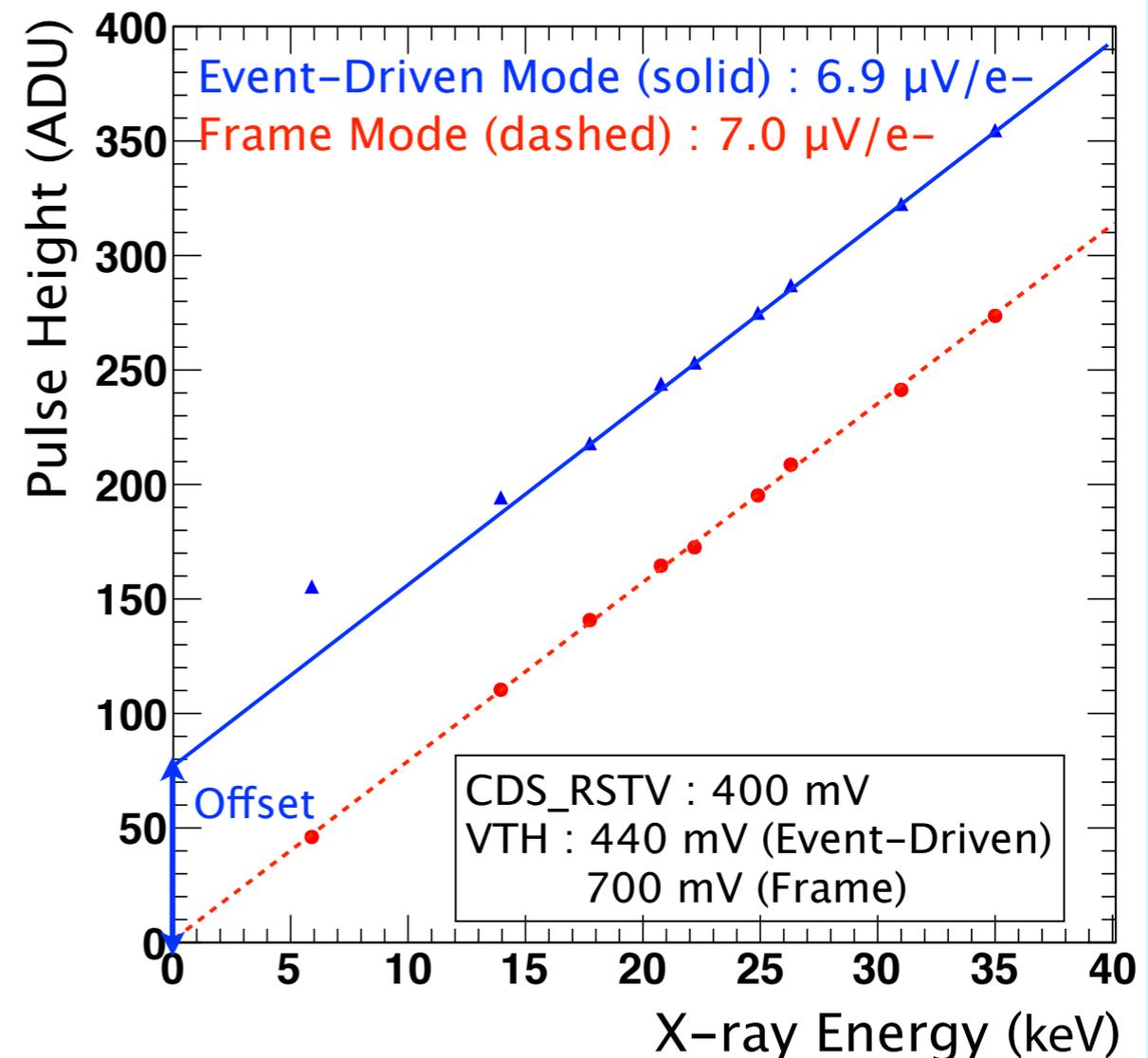
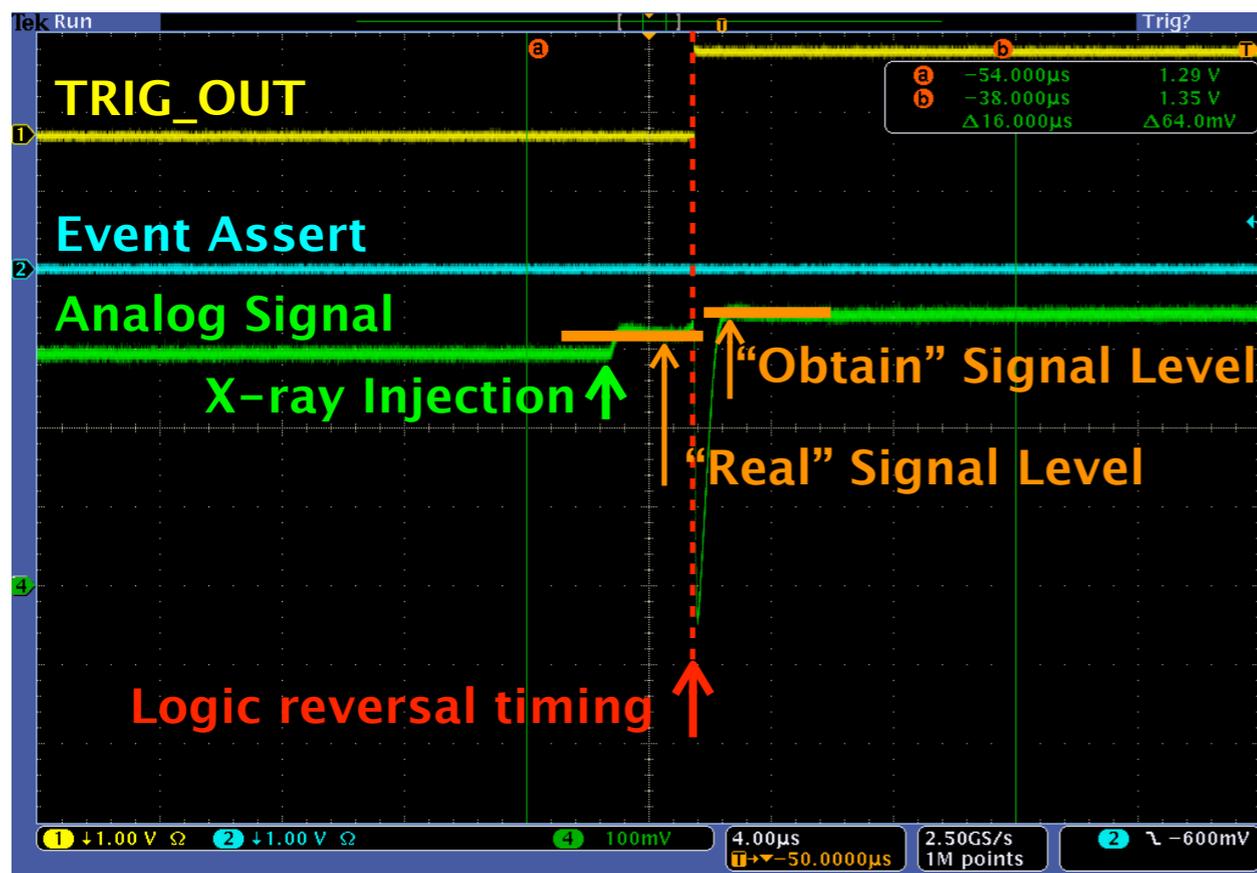
XRPIX2b / Pixel Layout



XRPIX2b / Chip Layout

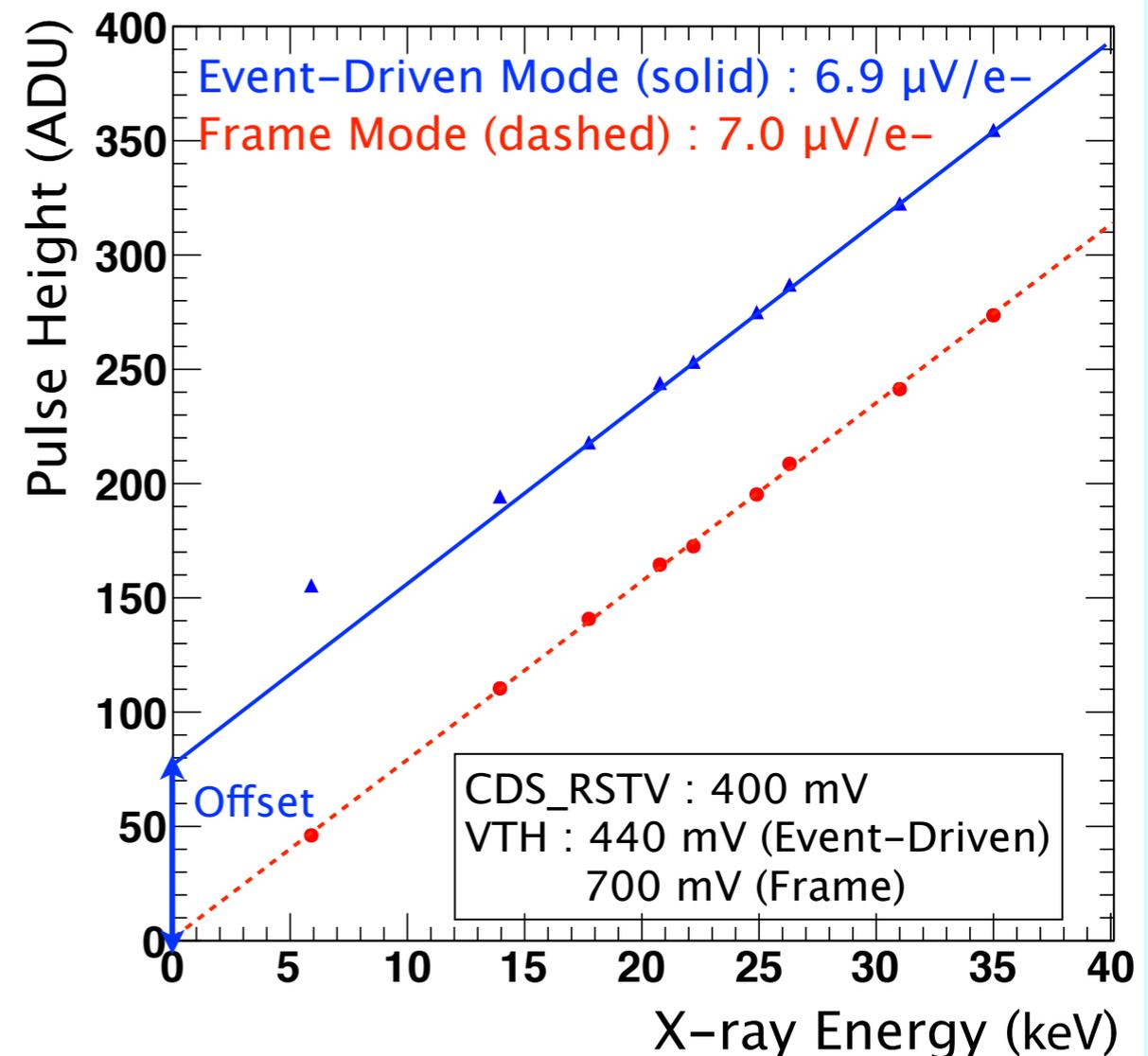
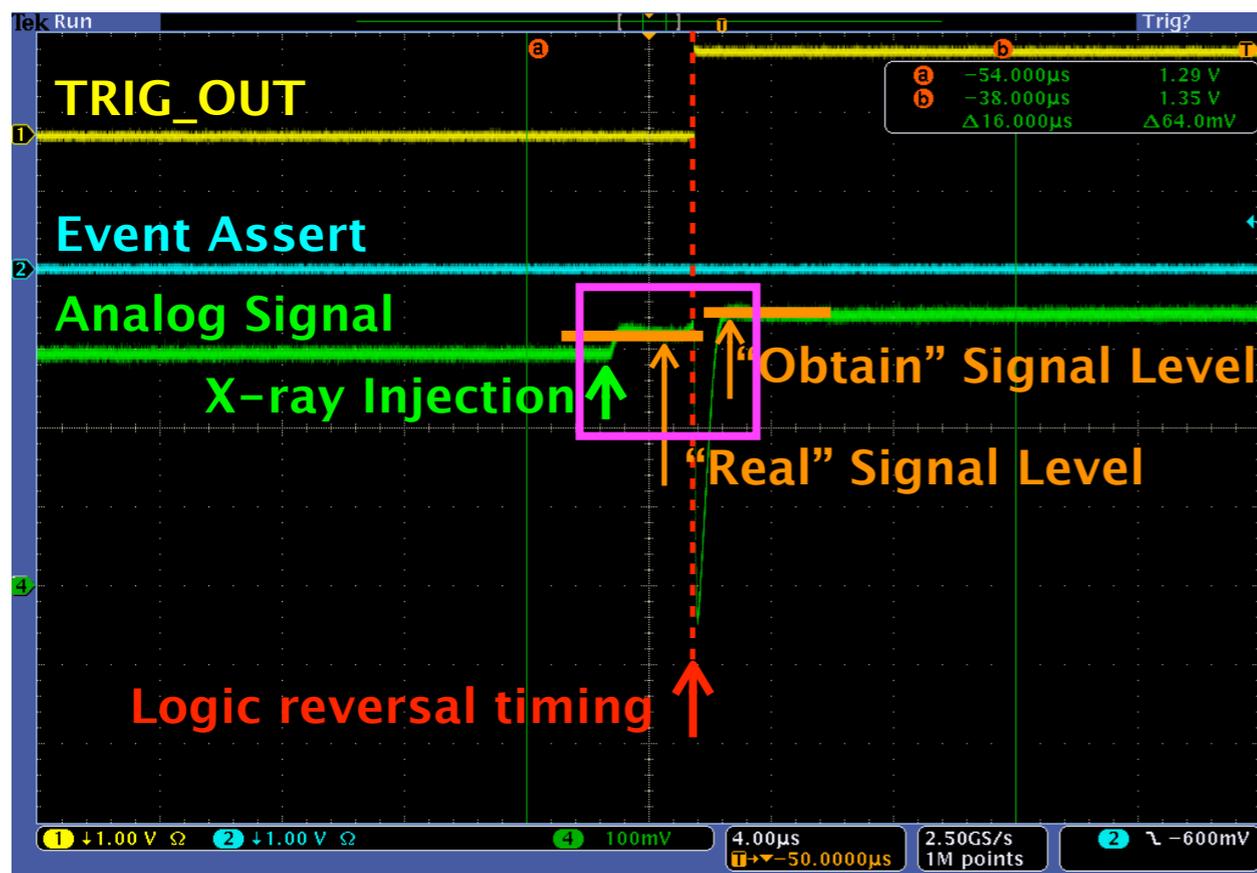
# 2. About the Difference in a Signal Level

- The difference between “real” and “observation” signal levels because of the capacitive coupling of the trigger signal line and sense node.
- This is visualized by abrupt increase in the analog signal level that does not return to the original level.



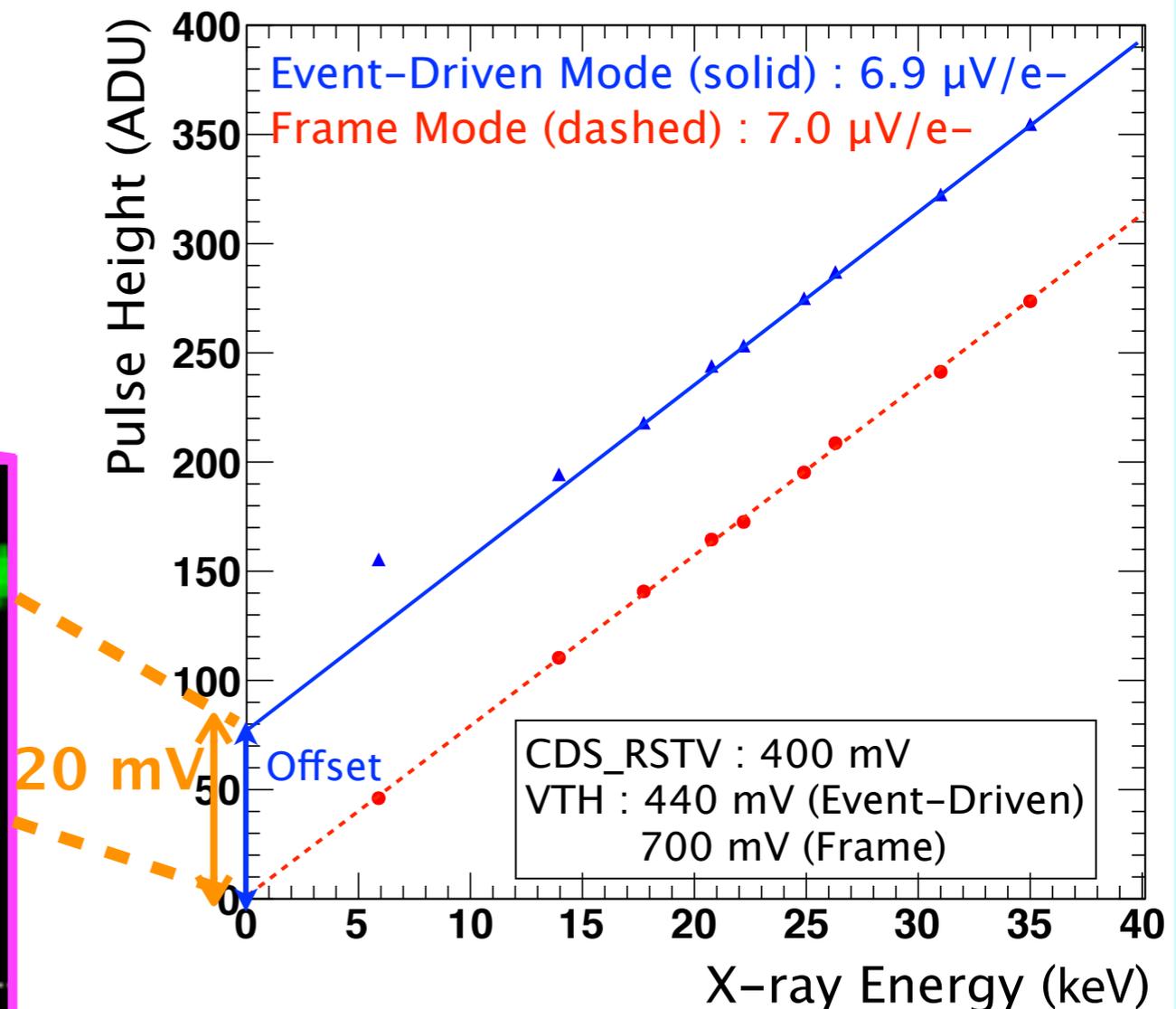
# 2. About the Difference in a Signal Level

- The difference between “real” and “observation” signal levels because of the capacitive coupling of the trigger signal line and sense node.
- This is visualized by abrupt increase in the analog signal level that does not return to the original level.



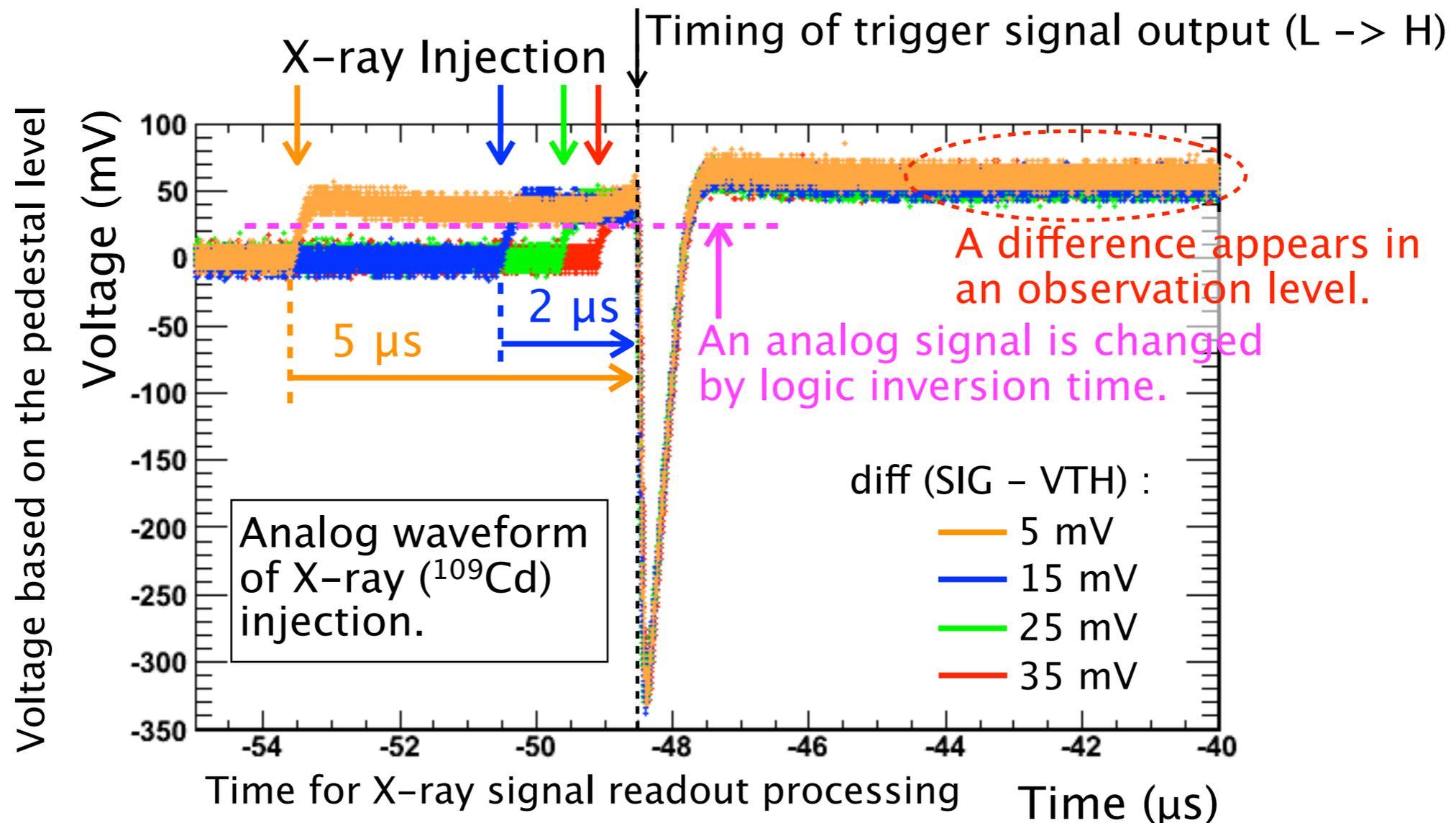
# 2. About the Difference in a Signal Level

- The difference between “real” and “observation” signal levels because of the capacitive coupling of the trigger signal line and sense node.
- This is visualized by abrupt increase in the analog signal level that does not return to the original level.
- However, it is equivalent to offset of a calibration plot ( $\sim 20$  mV).
  - > This is not a serious problem.



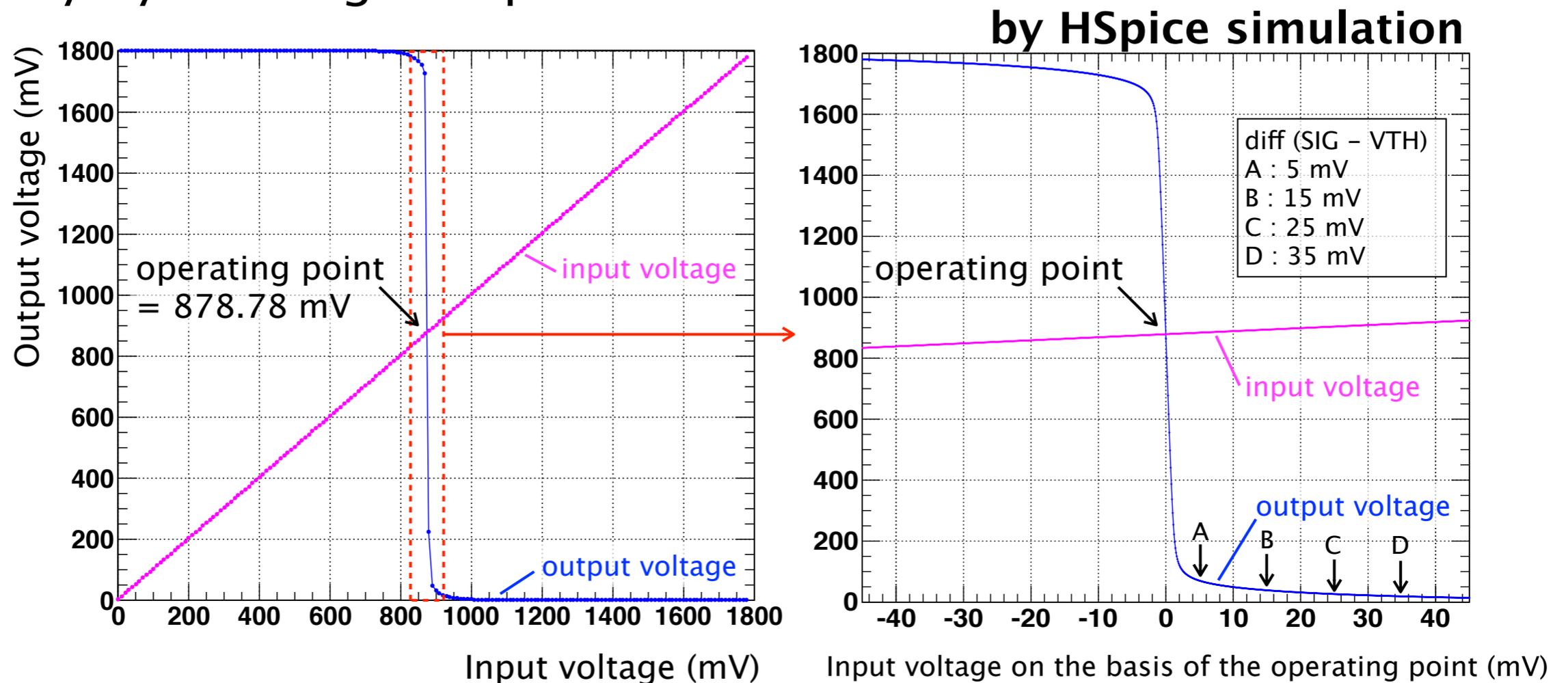
# 3. Long Logic Converting Time

- The long logic conversion time appear with the characteristic of a comparator circuit.
- The time is required for logic reversal such that the difference between the signal level and the VTH is small.
- This is exactly the characteristic of a comparator circuit (i.e., an inverter circuit in this case), as confirmed by HSpice circuit simulation.



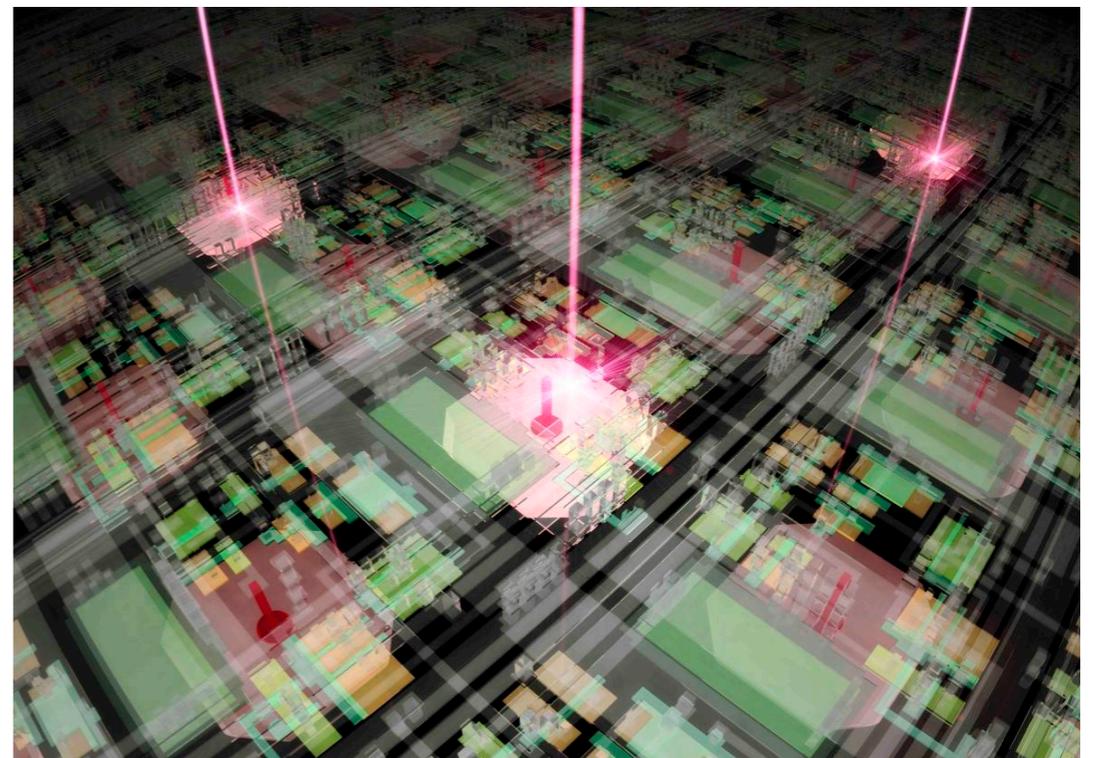
# 4. Change in the Analog Signal

- The change in the analog signal appears from the behavior and wiring composition of a comparator circuit.
- A large through current is obtained for a small value of  $\text{diff}(\text{SIG}-\text{VHT})$ .
- Because of the analog and digital power supply lines are not separated in the pixel, the consumption of local current influences the analog circuitry by a voltage drop.



The input-output characteristics of the first stage of the comparator circuit. The right graph shows a magnified view near the operating point. In the right graph, the x-axis is re-zeroed at the operating point.

# Evaluation of CSA Pixel Circuit



© Rey.Hori

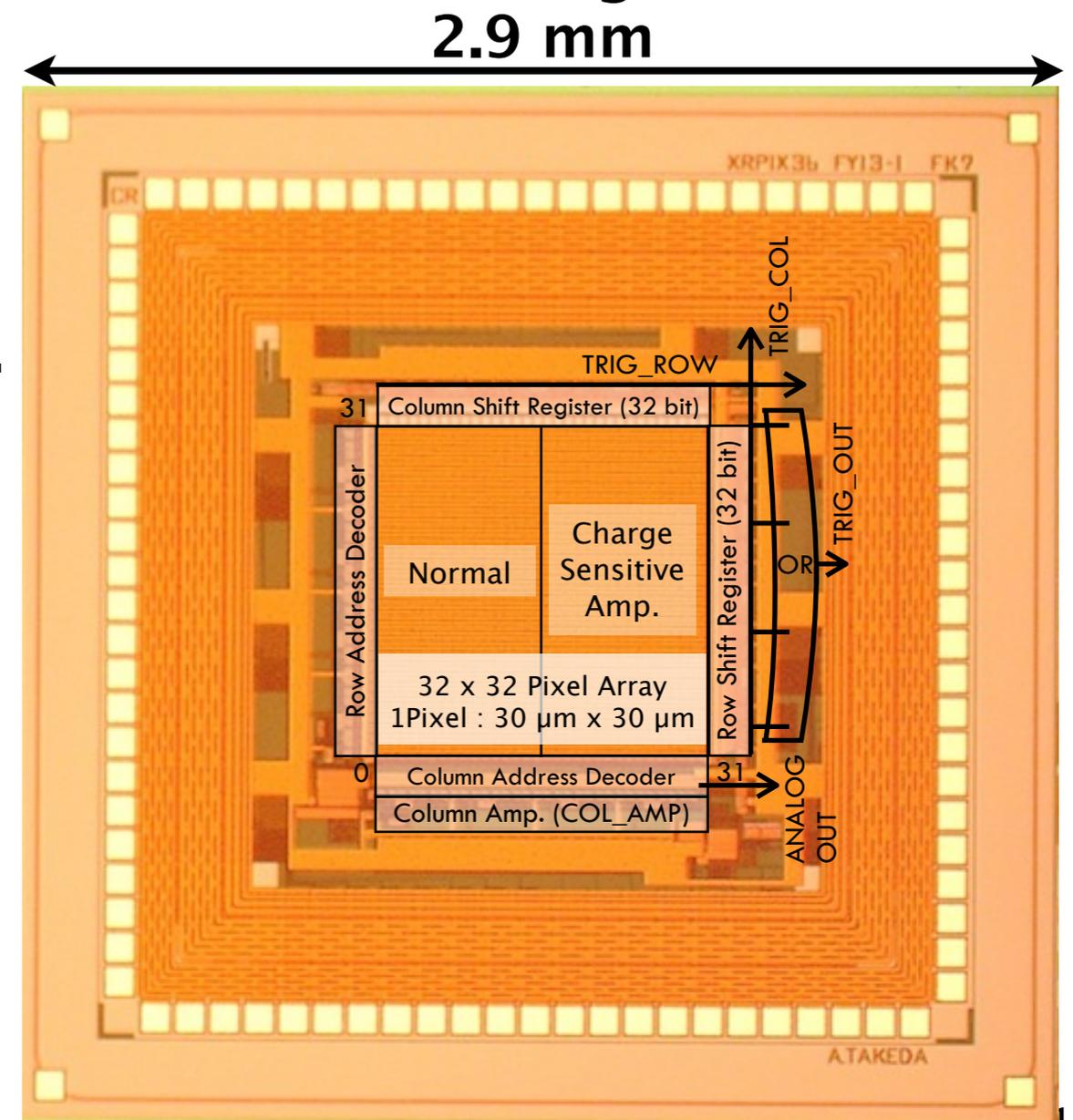
# Design Specification : XRPIX3b

## Components

- Chip Size : 2.9 mm sq. (Effective Area : 1.0 mm sq.)
- Pixel Size : 30  $\mu\text{m}$  sq.
- # of Pixel : 32 x 32 (= 1,024)
  - > Normal : 32 x 16 (Left) , CSA : 32 x 16 (Right)

Modification of XRPIX3 which is first prototype of XRPIX CSA circuit.

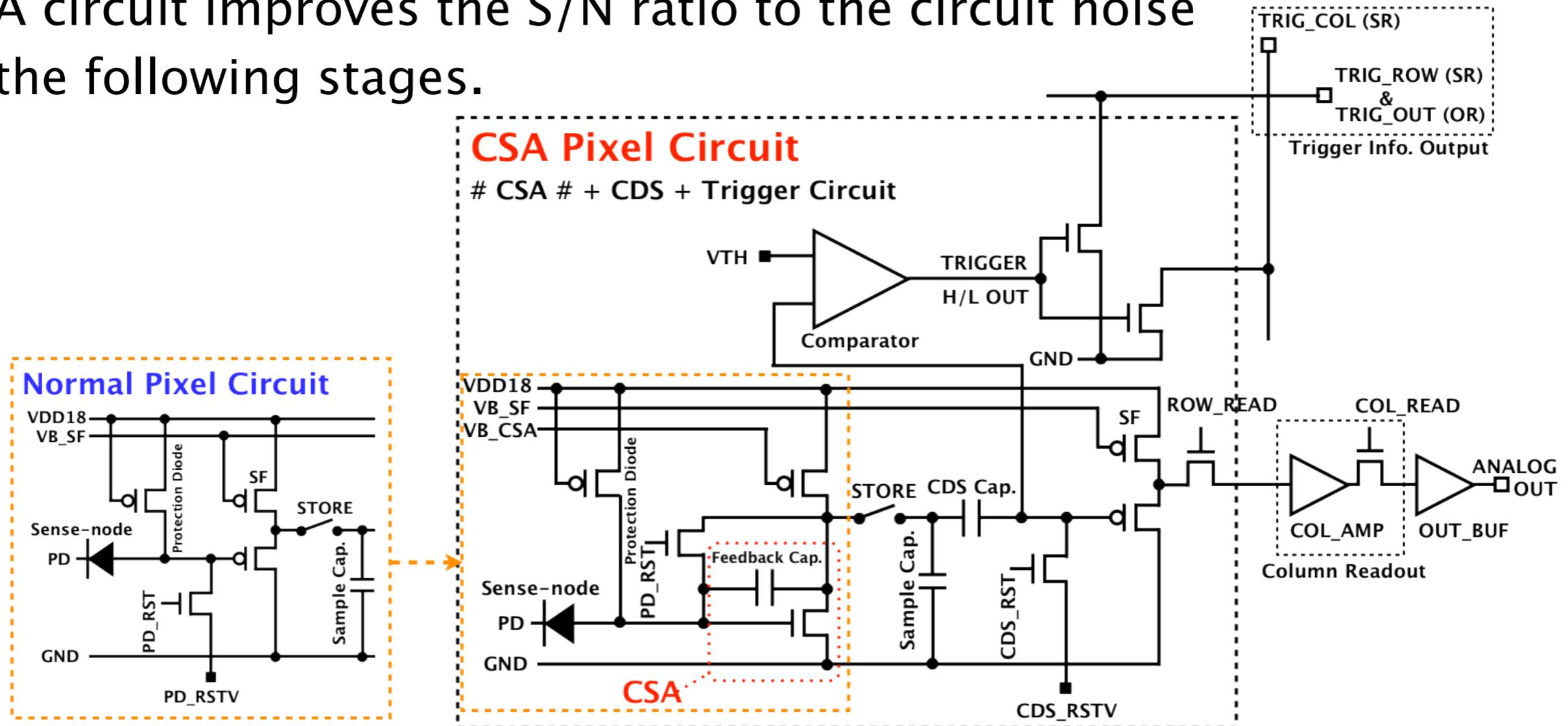
Comparison of **Normal** and **CSA** pixel.  
(Fabricated Jun, 2014)



# Pixel Circuit : XRPIX3b

- **Normal** and **CSA** pixels have different circuit configuration of preceding stage.
  - > **Normal** : Source Follower (SF) by Common-Drain of a PMOS transistor (**the same circuit as XRPIX2b**)
  - > **CSA** : pre-amplifier by Common-Source of a NMOS transistor and a feedback capacitance (1 fF)

CSA circuit improves the S/N ratio to the circuit noise in the following stages.



# Normal and CSA Circuit Calibration

- Calibration plot by  $^{55}\text{Fe}$  and  $^{241}\text{Am}$ .
- The pixel circuit with CSA works good. (3.3 times higher gain)

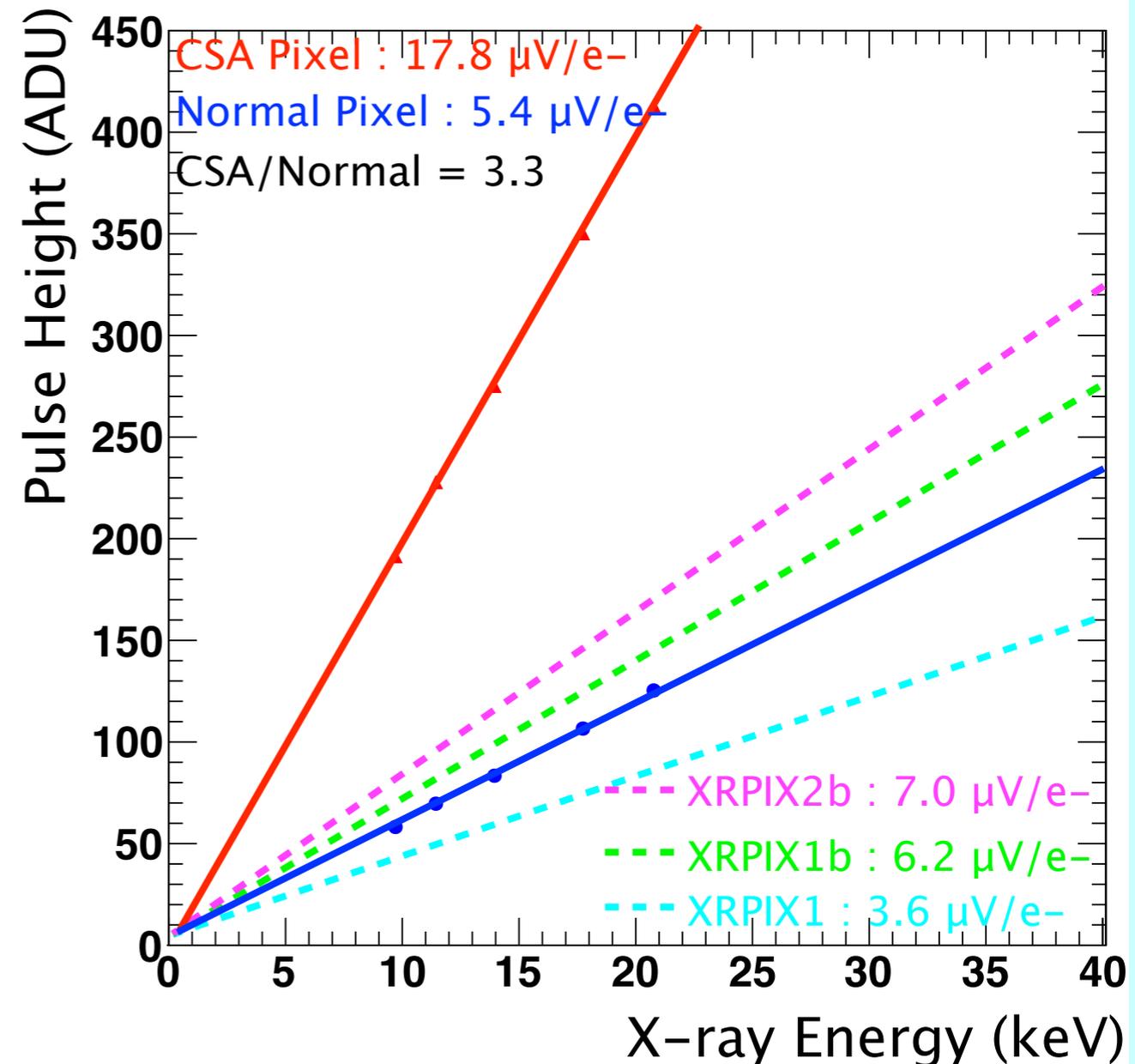
## Gain

Normal :  $5.4 \mu\text{V}/e^-$

CSA :  $17.8 \mu\text{V}/e^-$

Since parasitic capacitance of sense node increased, the gain fell from XRPIX2b by XRPIX3b.

Observed gain ( $17.8 \mu\text{V}/e^-$ ) is lower than the design ( $50 \mu\text{V}/e^-$ ), which would be due to parasitic capacitance.



One Analog Digital Unit (ADU)  
=  $244 \mu\text{V}$  (=  $1 \text{ V} / 12 \text{ bit}$ )

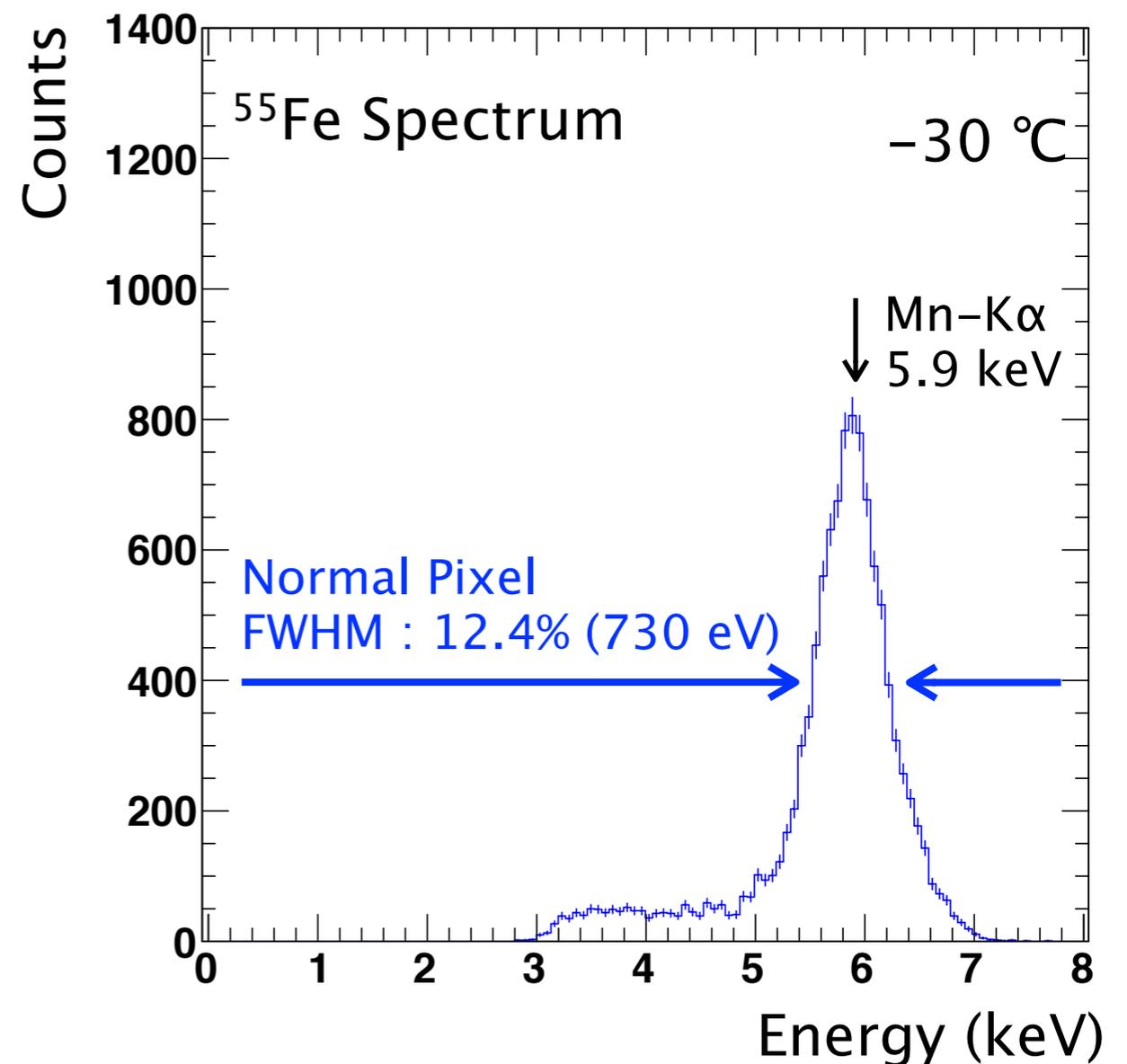
# Comparison of Normal and CSA Pixel

- The CSA Pixel succeeded in improvement of energy resolution. Comparison of  $^{55}\text{Fe}$  energy spectrum at Normal and CSA (obtain by Frame readout mode, not use Event-Driven)
  - > Readout noise (-> obtained from the pedestal peak)

**Normal** : 82 e- (rms)

- > Mn-K $\alpha$  @ 5.9 keV

**Normal** : 730 eV/12.4% (FWHM)



# Comparison of Normal and CSA Pixel

- The CSA Pixel succeeded in improvement of energy resolution. Comparison of  $^{55}\text{Fe}$  energy spectrum at Normal and CSA (obtain by Frame readout mode, not use Event-Driven)

-> Readout noise (-> obtained from the pedestal peak)

**Normal** : 82 e- (rms)

**CSA** : 35 e- (rms)

-> Mn-K $\alpha$  @ 5.9 keV

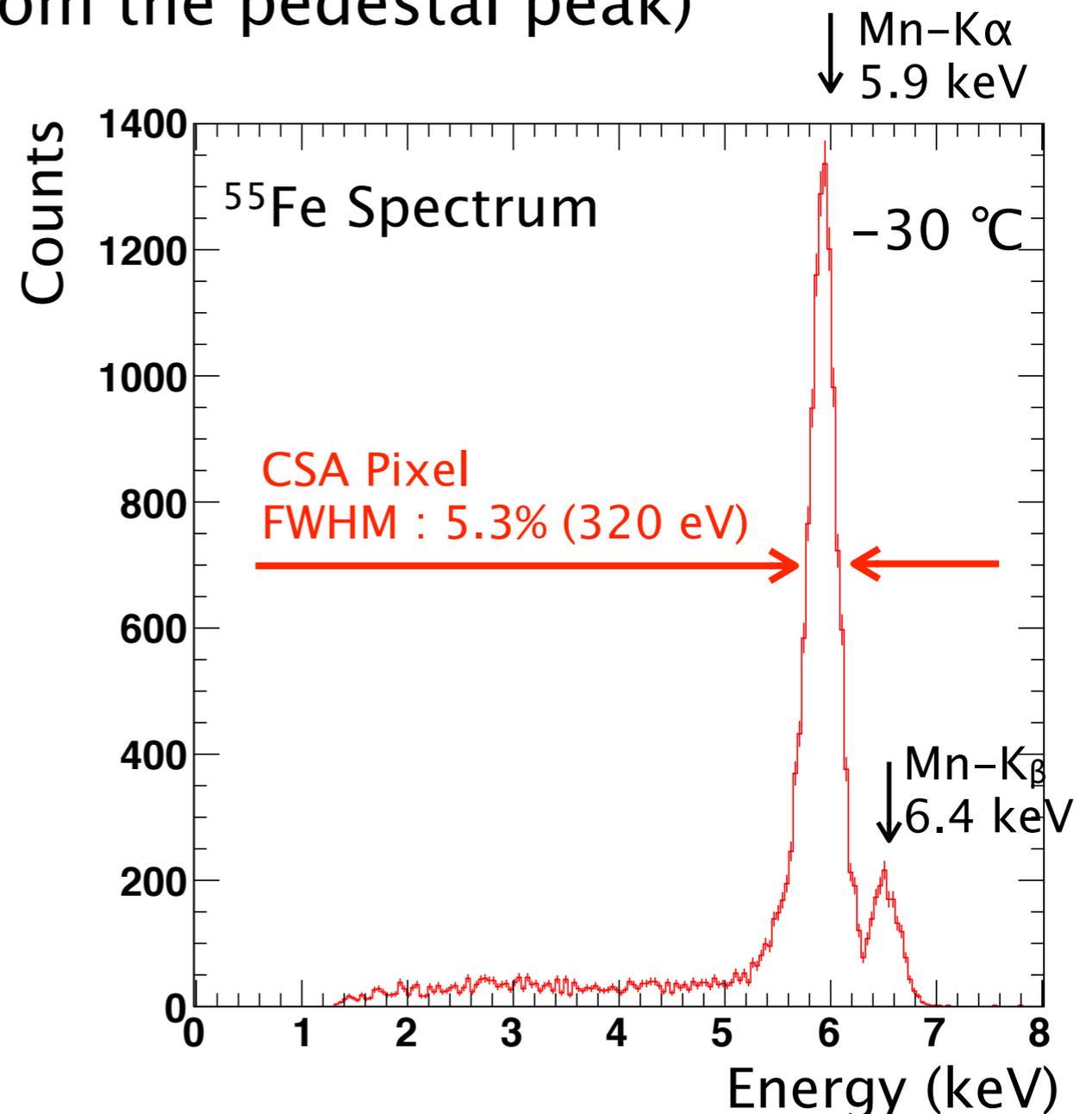
**Normal** : 730 eV/12.4% (FWHM)

**CSA** : 320 eV/5.2% (FWHM)

**Resolved Mn-K $\alpha$  and Mn-K $\beta$  successfully by CSA circuit !**

**-> Improvement of spectrum performance**

We achieve the target readout noise 10 e- (rms) by optimization of CSA circuit.



# Summary

---

- We have been developing Event-Driven SOIPIX sensor, “XRPIX”, for future X-ray astronomical satellite mission.
- Realize the Event-Driven readout mode and very low non-X-ray background by the function of the trigger signal output.
- We already successfully obtained X-ray data in Event-Driven mode.
  - > However, it has 4 problems.
  - > It has been understood that these problems were two main causes.
    - The cross talk including the circuit layer and a sense-node.
    - The characteristic of an inverter-chopper-type comparator circuit.
  - > The comparator circuit modification is required.
- By CSA pixel circuit, we improved energy resolution successfully.
  - > The readout noise : 35 e<sup>-</sup> (rms)  
Mn-K $\alpha$  @ 5.9 keV : 320 eV / 5.2 % (FWHM)
- We will improve the next design on the basis of these phenomena and optimize the CSA circuit.