Near Future Upgrades of the CMS Pixel Detector

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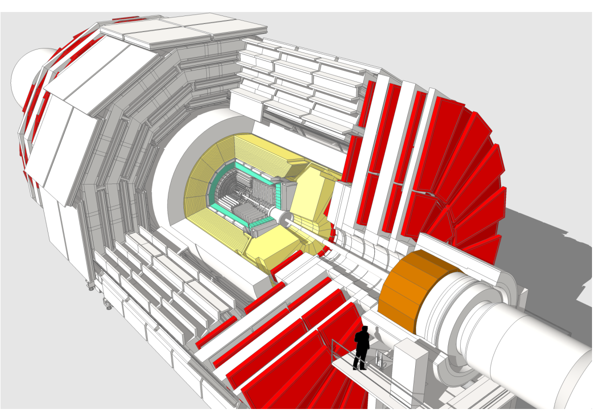
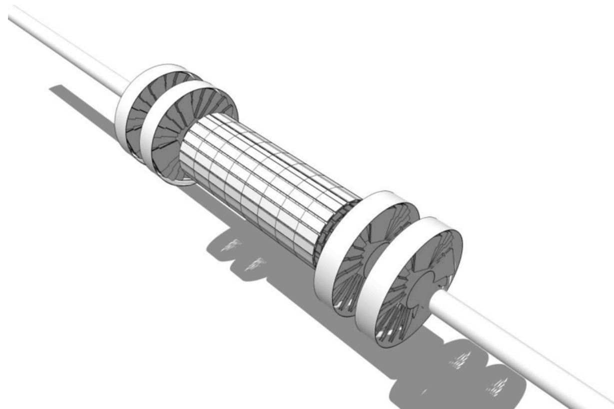
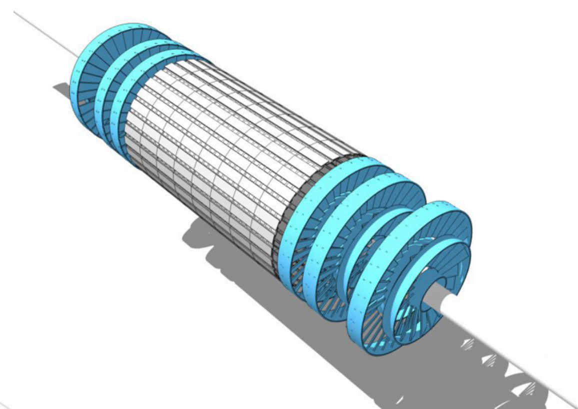






Outline

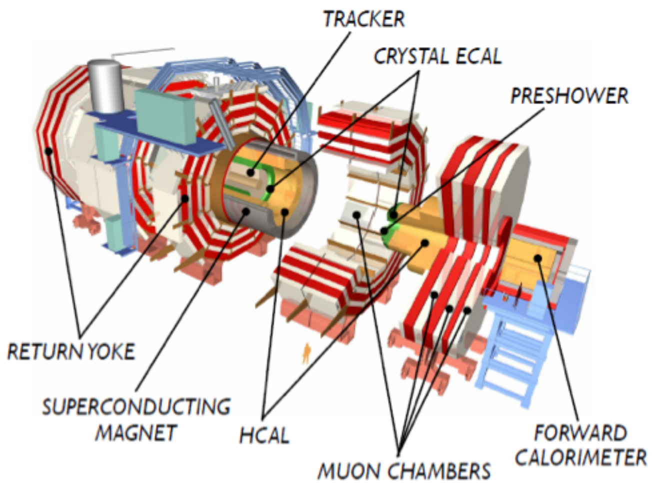
- Current Pixel System
- Motivations for Upgrade & Constraints
- Elements of Phase 1 Upgrade
- Expected Performance
- Status of Upgrade
- Pilot System
- Summary

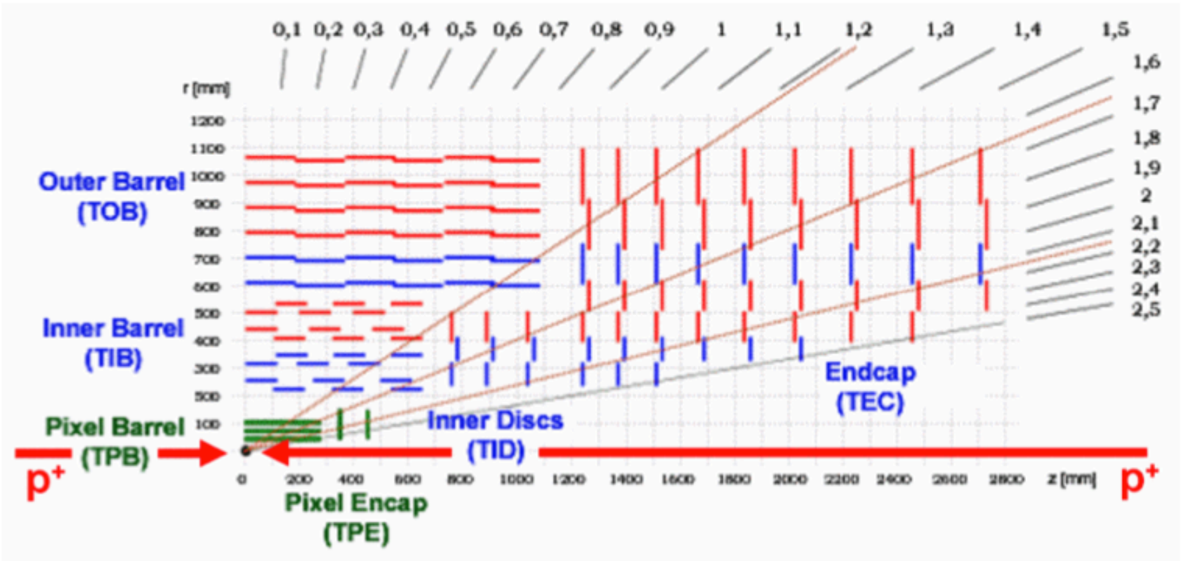
The CMS Tracker

- All-silicon tracker : largest silicon detector ever built. Immersed in 3.8 T magnetic field
  - Strips

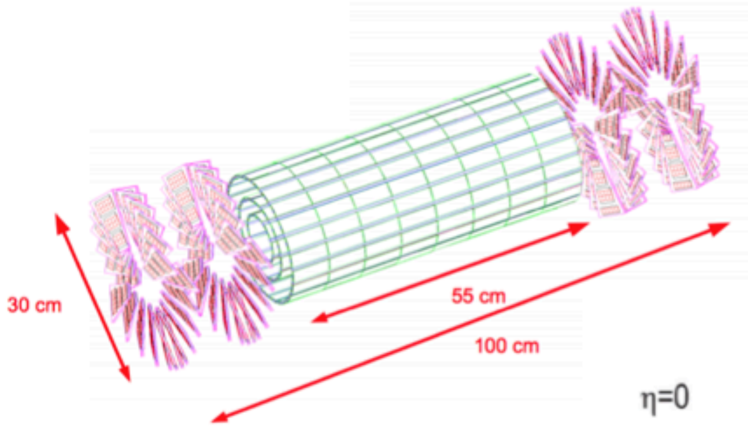
    9.3 M channels, Area : 200 m^2
  - Pixels

    66 M channels, Area: 1 m^2

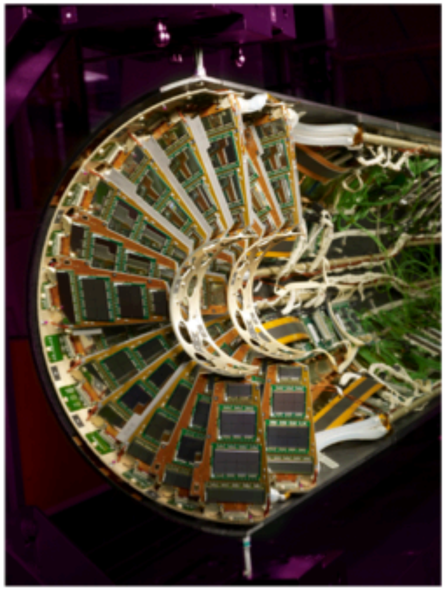




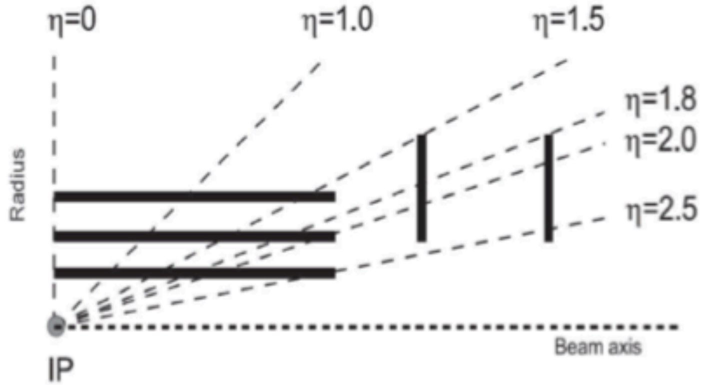
Present CMS Pixel Tracker

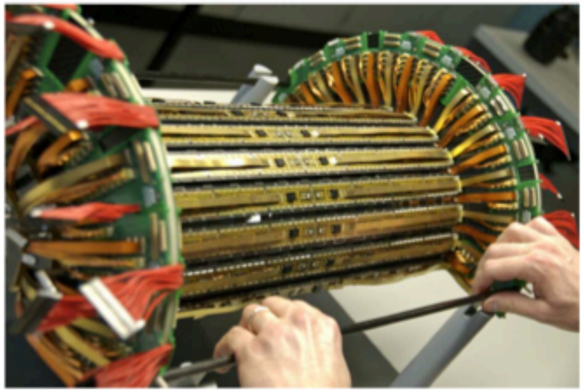


- FPIX (forward)
  - 2 disks / endcap
    - z = 34.5, 46.5 cm
    - 6 cm < r < 15 cm
  - 18M pixels, 0.28 m^2



- BPIX (barrel)
  - 3 layers
    - r = 4.3, 7.2, 10.8 cm
  - 48M pixels, 0.78 m^2

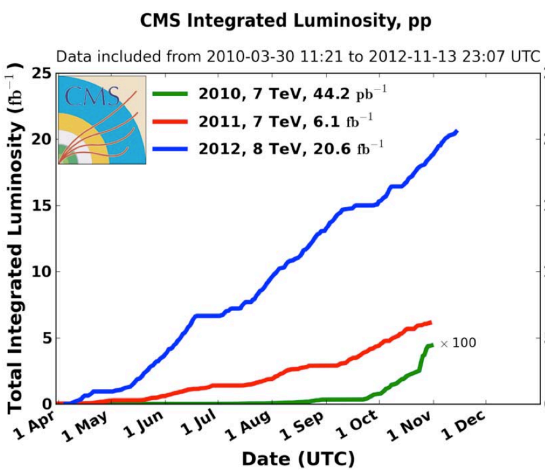


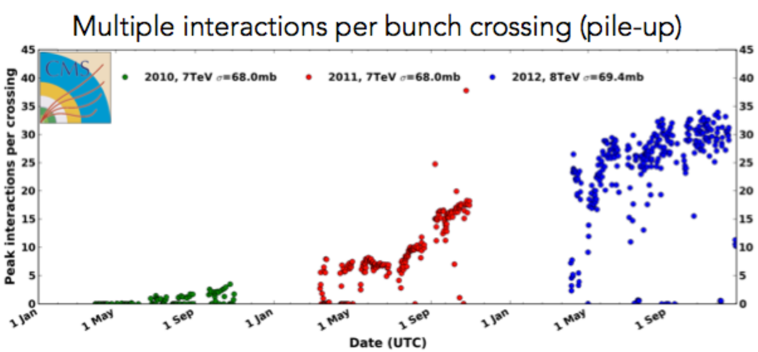


- 3-hit (2-hit) coverage for tracks $|\eta|$ ~2.1 (<2.5)
- Plays crucial role in vertexing (primary and secondary vertices) and tracking

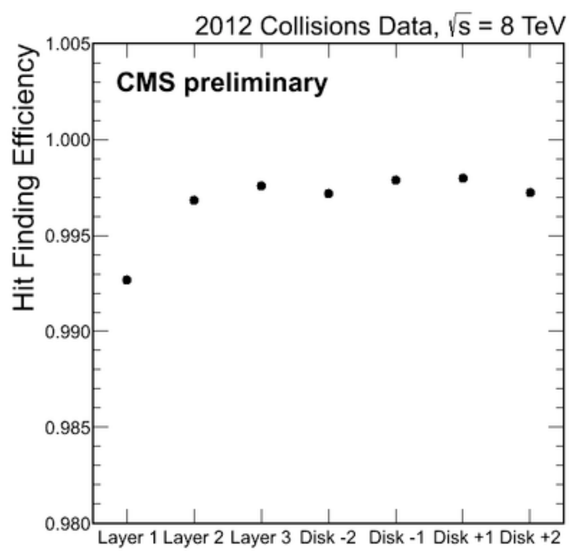
LHC Run 1: Performance

- Excellent performance of LHC with peak luminosity 7.67×10^{33} $cm^{-2}s^{-1}$
- Almost at design luminosity with bunch spacing 50 ns
- Overlapping interactions per bunch crossing up to 34 at begin of store



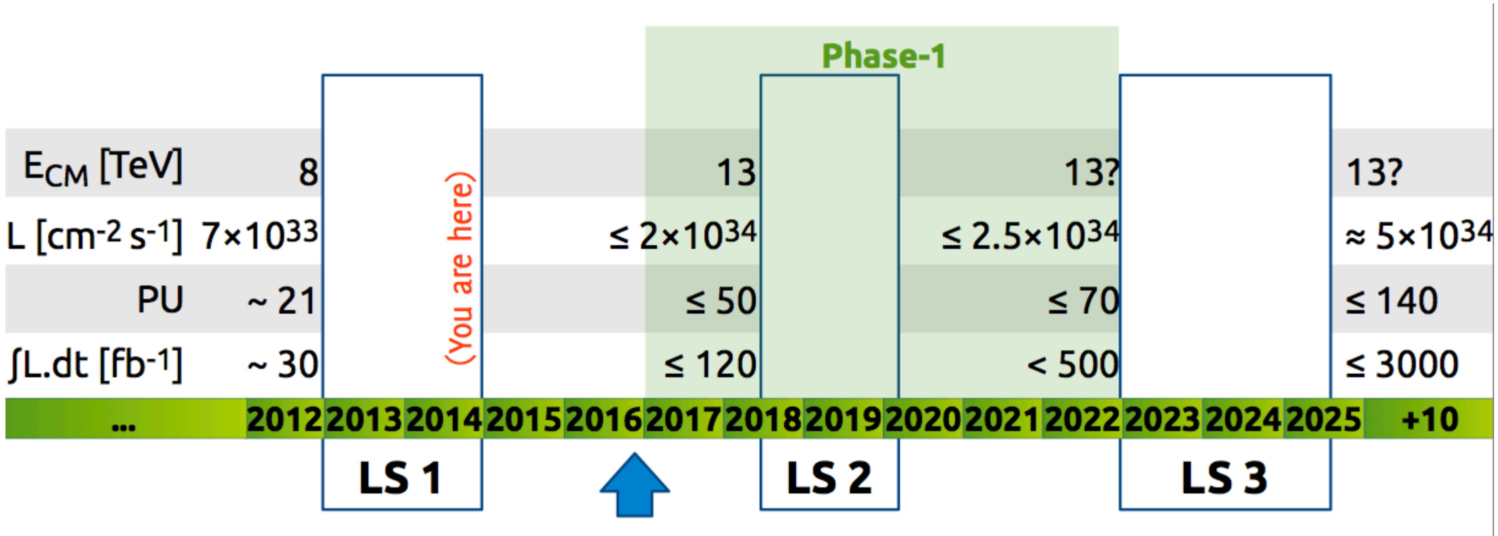


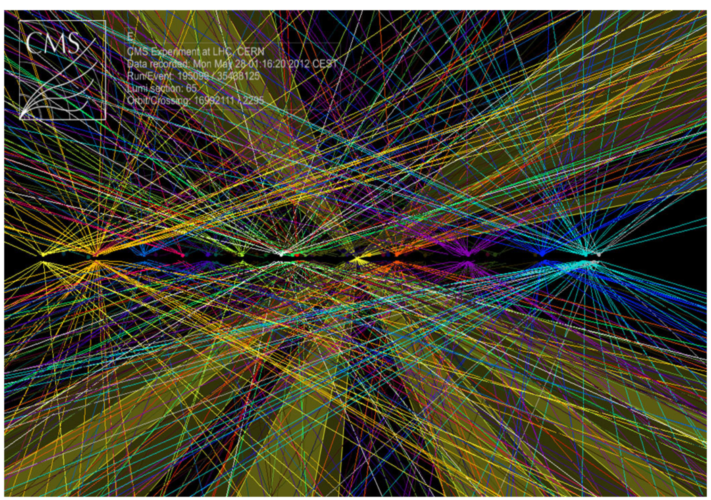
- Excellent data taking efficiency
- Stable performance of Pixel detector
  - Fully operational 96%
  - Pixel hit efficiency >99%



Covered in the talks by Frank Meier & Janos Karancsi

Challenges for LHC Run 2



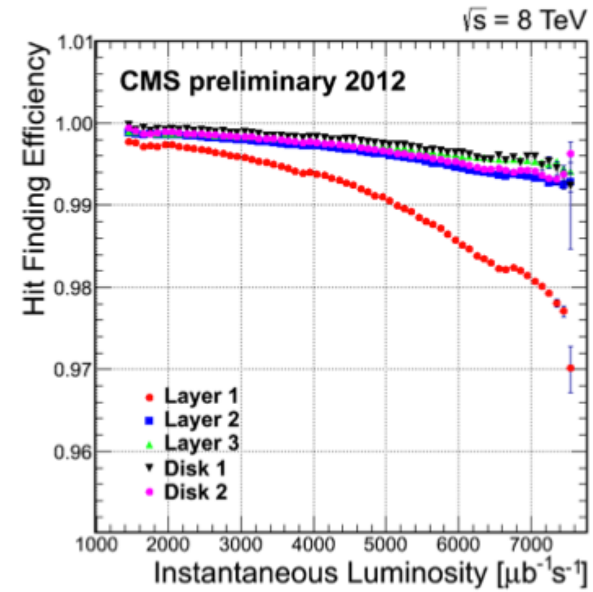


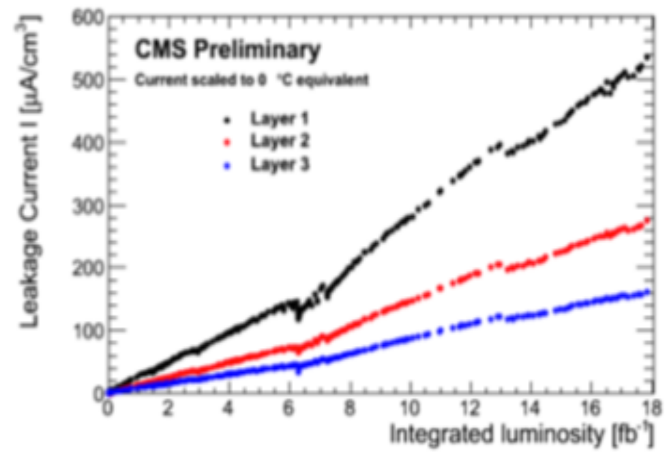
- **Criteria for upgrade**
  - Operate with a baseline pileup of ~50 events/crossing, tolerate max of 100
  - Maintain low trigger thresholds with increased event rate
  - Survive doses corresponding to luminosity of ~500 fb^{-1}

Why Upgrade the Pixel Detector?

- Pixel tracker designed for maximum $L_{inst}=1x10^{34}cm^{-2}s^{-1}$

- $L_{inst}=2x10^{34}cm^{-2}s^{-1}$ likely before 2018
  - Limits of readout chip buffers & speed, high data loss (16% @25 ns / 50% @50 ns) for Layer 1
  - Increasing effects of radiation damage: degradation of spatial resolution Sensors designed to run at design lumi for 2 years with expected fluences of up to $0.6x10^{14}\ n_{eq}/cm^2$ for Layer 1
  - Reduced physics performance: difficult pattern recognition





Phase 1 Pixel Upgrade Strategy

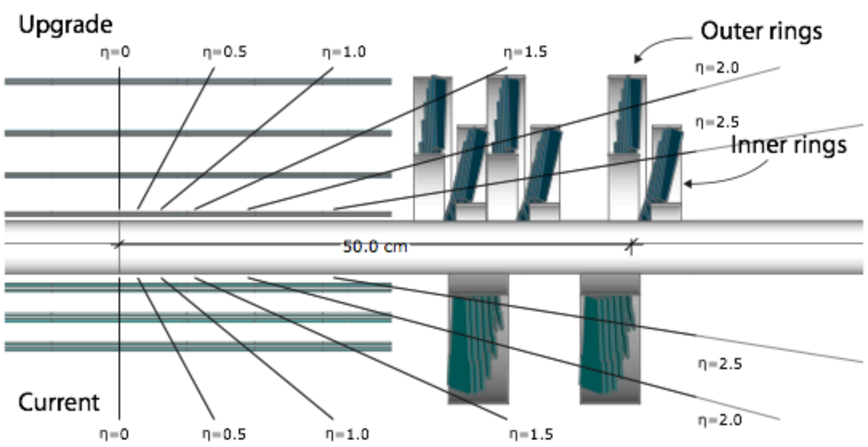
Goal: Sustain the current pixel performance (efficiency / low fake-rate, resolution) at 50 interactions per bunch-crossing or higher

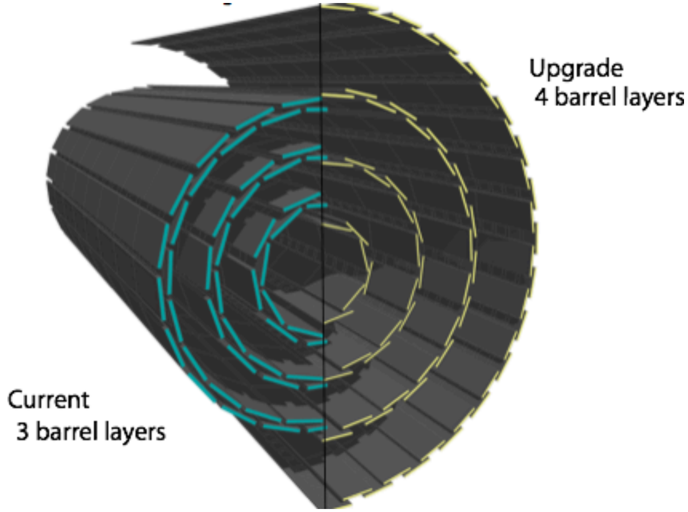
- **Elements of upgrade**
  - More layers (3➔4 barrel layers, 2x2➔2x3 forward disks) : more 3D space points for robust pattern recognition
  - Improved mechanics, cooling and powering : reduction of material in tracking volume => less multiple scattering, fewer photon conversions
  - New readout electronics to handle higher rates
  - Minimize degradation due to radiation damage : lower temperature, lower pixel threshold

- **Constraints of upgrade**
  - Schedule : Install during 2016/2017 extended year-end stop
  - Keep services (cables, pipes, fibers …)
  - Be compatible with the new smaller diameter beam pipe

From 3- to 4- Hit Tracking

- Optimized detector layout for 4-hit coverage over full η range (±2.5) with a radius of the innermost layer as close to beam pipe as possible
  - additional 4th BPIX layer: 48M pixels ➔ 79M pixels
  - additional 3rd FPIX disks: 18M pixels ➔ 45M pixels
- Improves efficiency and resolution for pixel-only tracks important for:
  - High level Triggering
  - Seeds for full tracking=> higher track efficiency and lower fake track rate
  - Vertexing: both primary (-> pile up) and secondary (-> b-tagging)
- Improves impact parameter resolution (-> b-tagging)





Barrel Pixel (BPIX) Layout

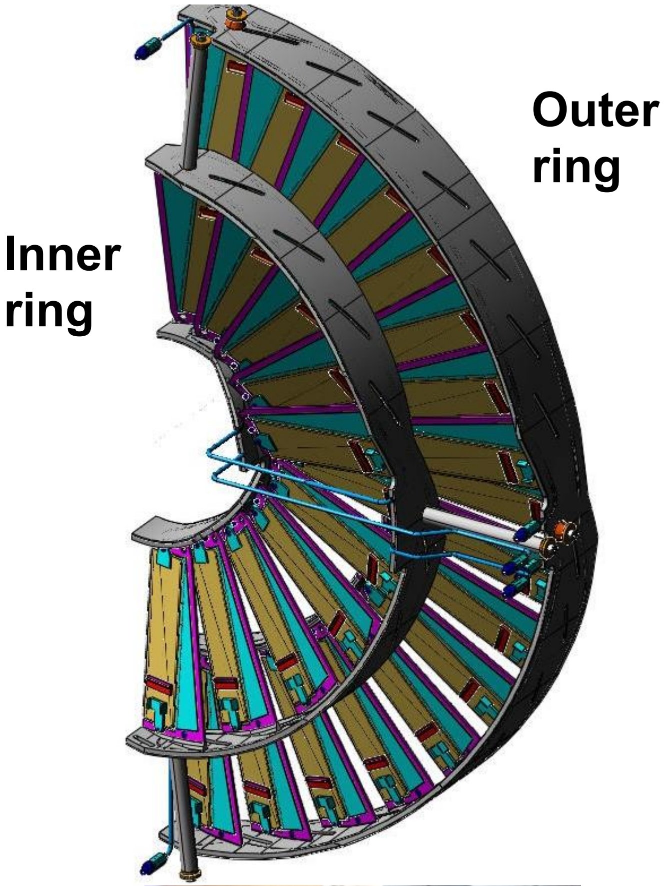
- Arranged in 4 layers in 2 half-barrels : 1184 modules of the same type

layer	radius	faces	modules
1	29 mm	12	96
2	68 mm	28	224
3	109 mm	44	352
4	160 mm	64	512

- Innermost layer:
  - Radius reduced from 44 mm to 29 mm → new beam pipe with outer diameter of 45 mm
  - Replaceable without disconnecting other layers (foreseen after 250 fb^{-1})

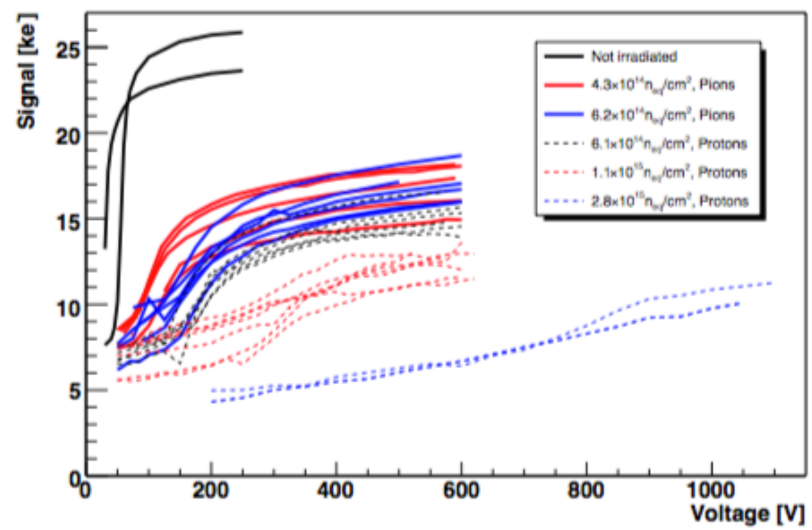
Forward Pixel (FPIX) Layout

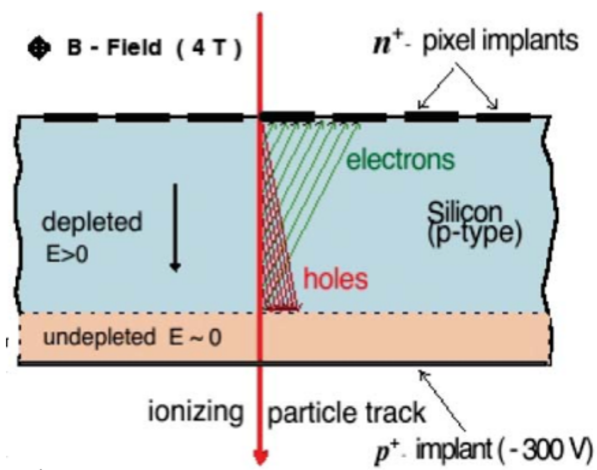
- 3+3 disks with 672 modules
- Independent half disks with inner and outer rings for easier replacement
  - Outer: 34 modules, 17 blades
  - Inner: 22 modules, 11 blades
- Same module design as BPIX with 2x8 readout chips
- All blades rotated by 20^0 around radial axis to enhance charge sharing and improve r-Φ resolution
- Blades on inner ring have additional 12^0 tilt for better z resolution



Pixel Sensors

- **Keep present design:**
  - 285 µm thick Si with pixel size of 100x150 μm^2, each pixel bump-bonded to its readout
  - "n^+-in-n" radiation tolerant design, under-depleted operation possible
  - p-spray (BPIX) or p-stop (FPIX) for n-side isolation
- Signal charge is deflected by magnetic field and shared among pixels => enhances position resolution

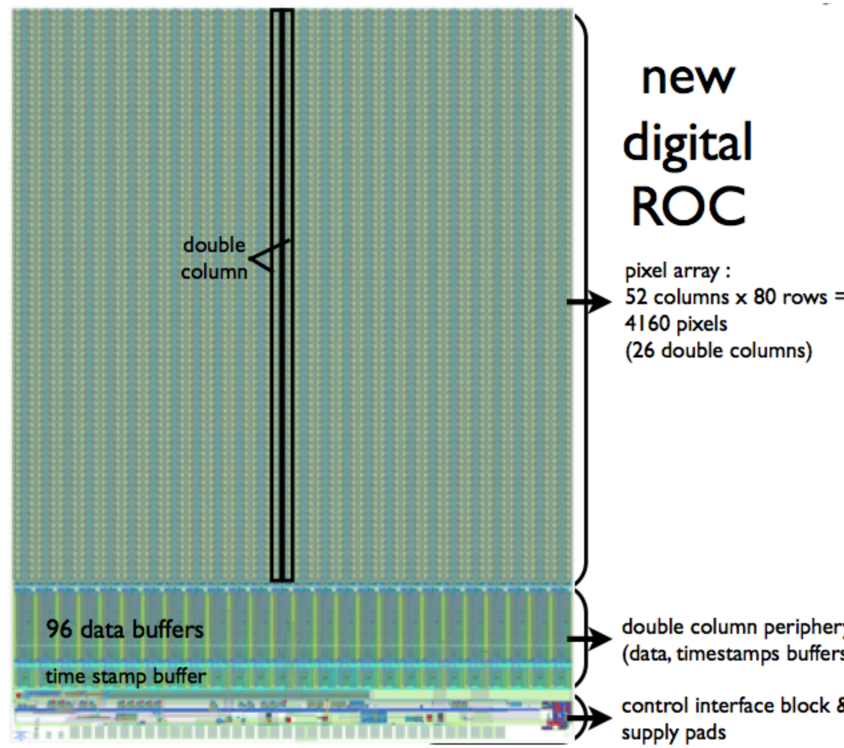




- Fluence of 1.5 n_{eq}/cm^2 expected during lifetime of Innermost layer (replacement after 250 fb^{-1})
- For samples irradiated up to 1.1 n_{eq}/cm^2 capability with biases of 450-600V provide some margin
- Also gain from improvements on lower threshold

New Pixel Readout Chip (ROC)

- **ROC features**
  - 250 nm, IBM process
  - Area: 7.9 x 9.8 mm^2, 6 metal layers
  - Pixel array: 52 columns x 80 rows
  - Column drain readout architecture
- **Reduced data losses**
  - increased time stamp / data buffers 12/32 → 24/80 to prevent overflow with high occupancy
  - Increased readout link speed (40 MHz analog→160MHz digital) for pixel address and pulse heights
- **Reduced pixel threshold** of 1800e from present 3500e



See talk by Dmitry Hits for more details

New Cooling & Powering System

- Present pixels use mono-phase C_6F_{14} cooling scheme → major fraction of material budget
- Upgrade to two-phase CO_2 cooling
  - High heat transfer coefficient; more heat load per channel
  - Requires less flow and smaller diameter pipes despite high pressure operation (up to 70 bar) → major fraction of material savings in pipes & coolant

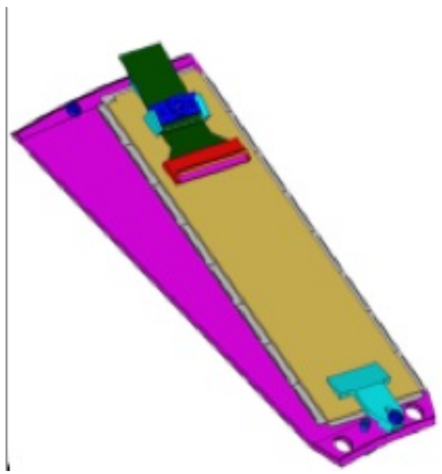
Weight Layer1 51g + 11g CO_2
→ 40% of old first layer

DC-DC Converters

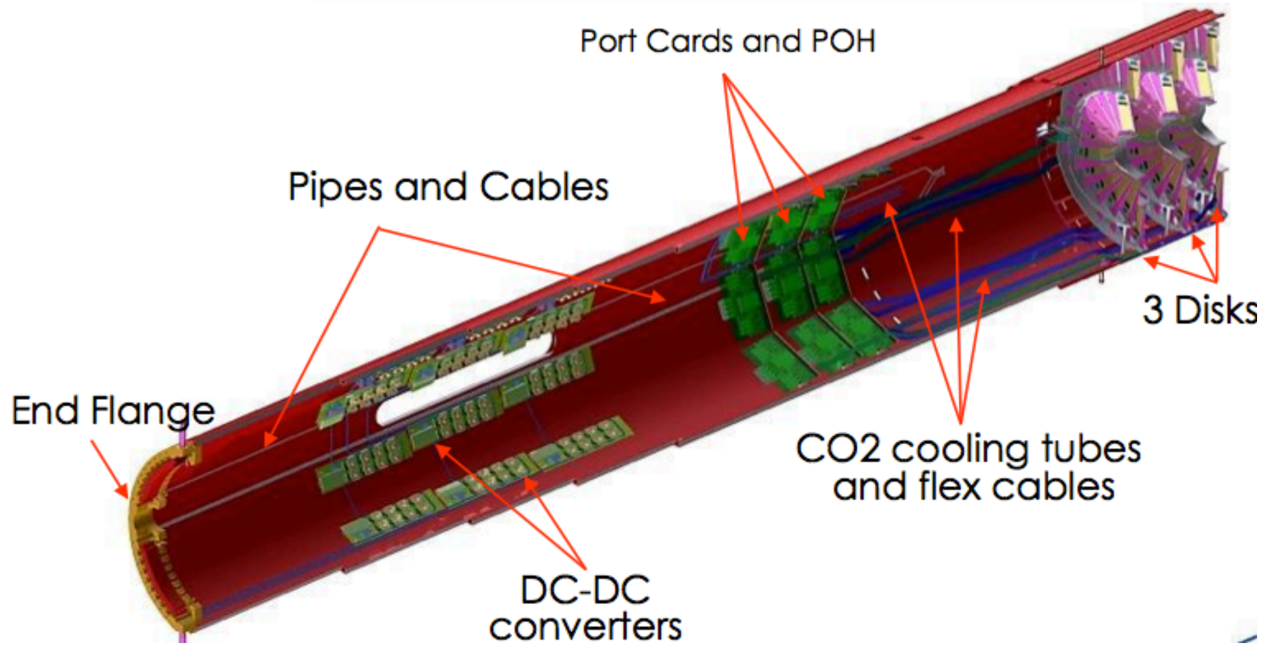
- Substantial increase in no of channels (demands more power) but use present LV cables.
- Up scaling existing power system leads to high cable losses.
- Solution: Modified CAEN PS modules deliver higher voltage at lower current. DC-DC converters generate low voltage with high current in the service cylinder
  - Conversion ratio of 3-4, losses on supply cable less by factor of 10

FPIX Support Structure

- Module & disk design uses light material (replaces Al/Be)
  - Modules mounted on low mass thermal pyrolytic graphite (TPG) blades. Blades supported and cooled by low mass graphite/carbon fiber rings. Graphite rings are cooled by two-phase CO_2 in embedded stainless steel tubes
  - Disks supported by low mass single shell carbon fiber cylinders

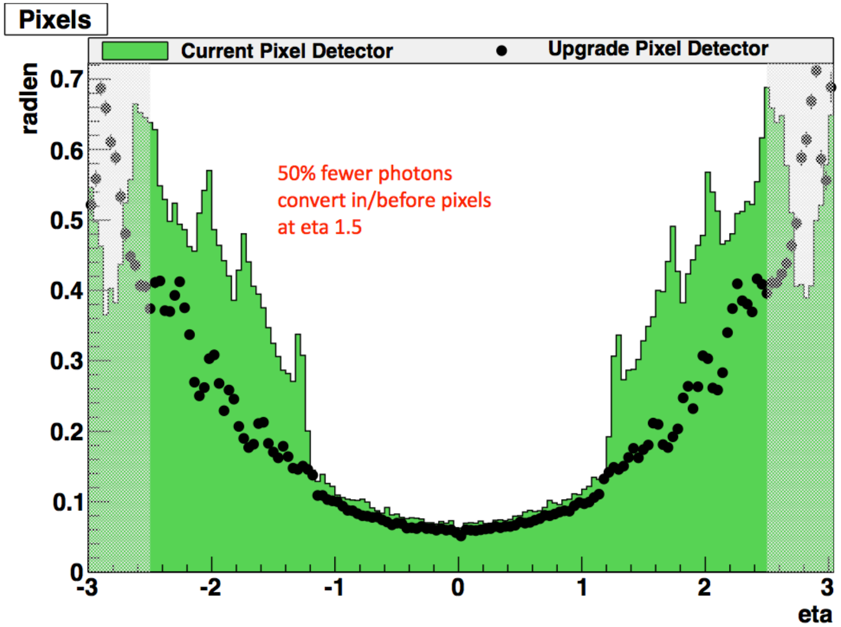


Current Half Cylinder (1/ 4)



Impact on Material Budget

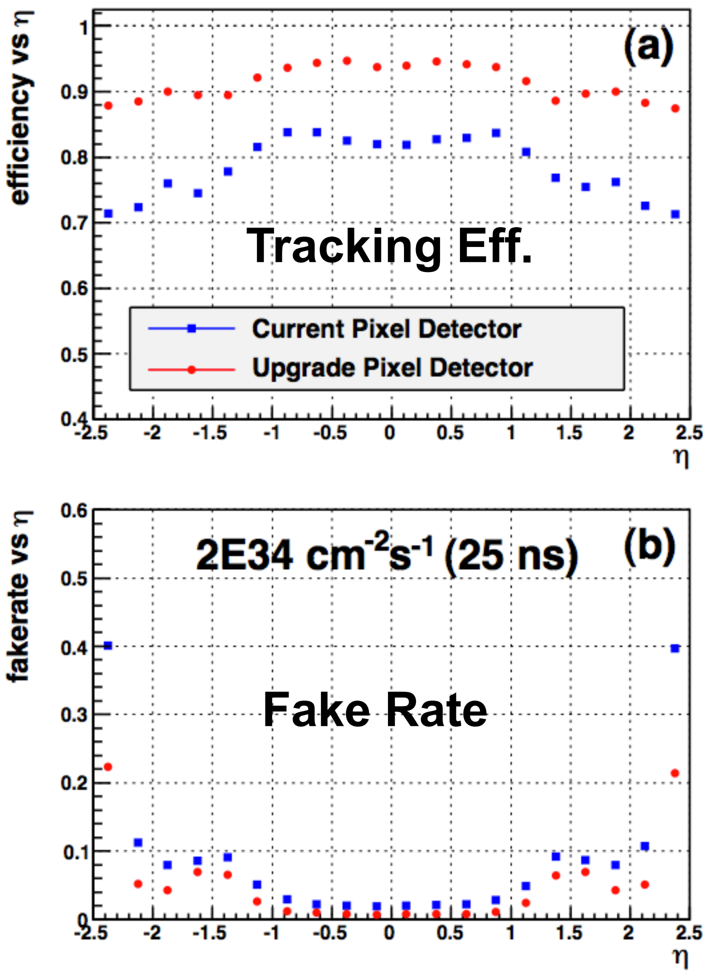
- Despite additional layer/discs, substantial reduction in material budget in the tracking volume
  - New ultra-light mechanical support
  - C_6F_{14} -> two-phase CO_2 cooling (low mass & allow smaller and lightweight pipes)
  - Moving electronic boards and connections out of active tracking region



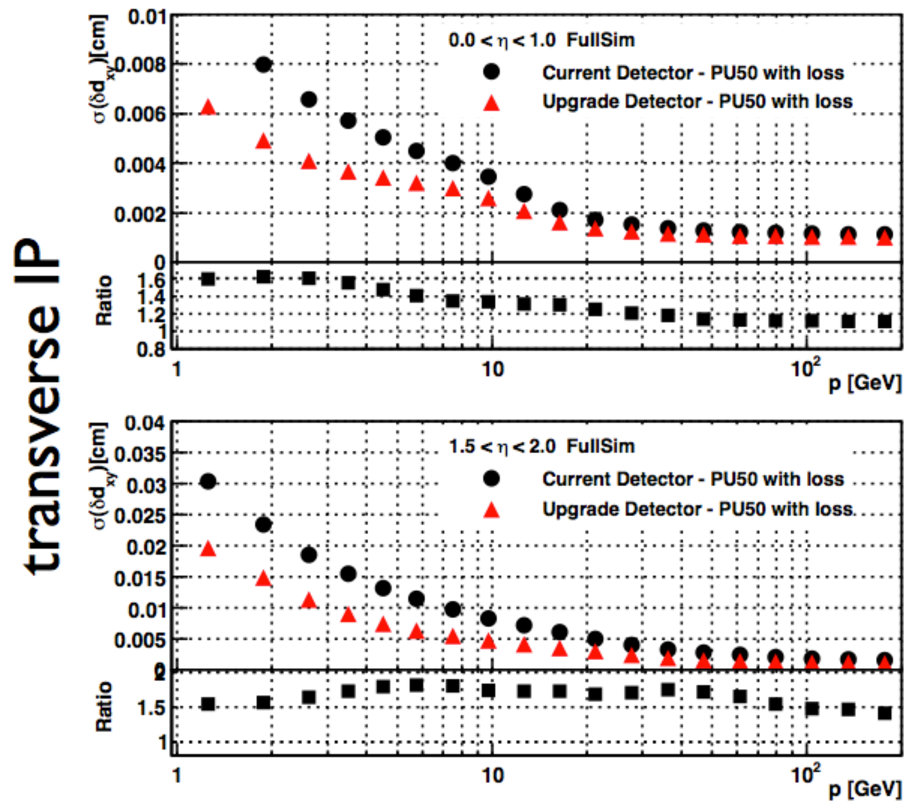
- Material reduction will reduce the photon conversions, leading to improved electron reconstruction, and will reduce the rate of secondary tracks from nuclear interactions

Impact on Tracking

- Use simulated top pair events with 50 pileup vertices

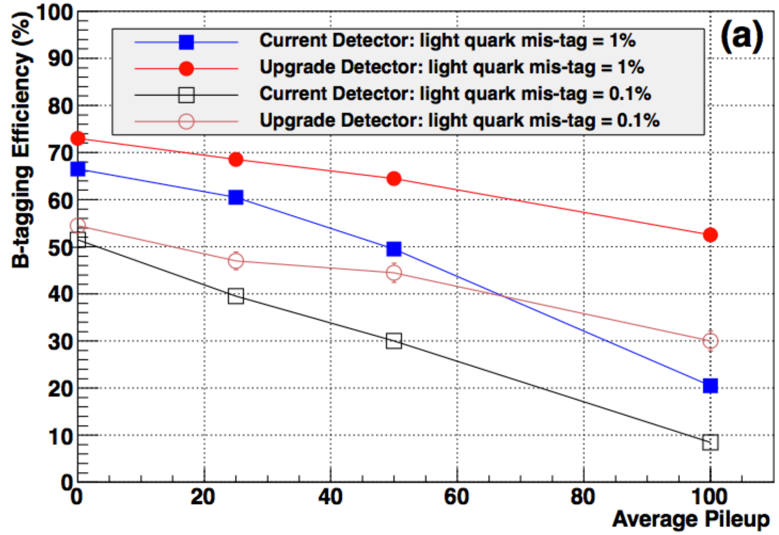


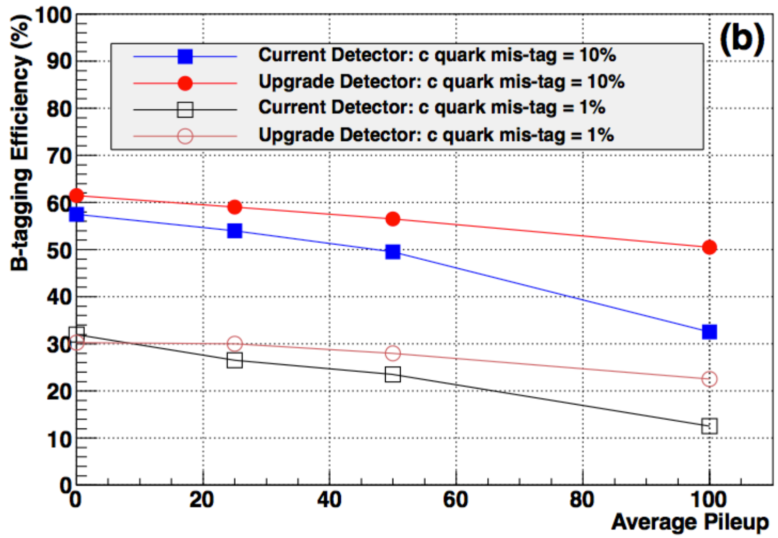
- Improvements in transverse and longitudinal impact parameter resolutions : more pronounced at low p_T



B-Tagging Improvements

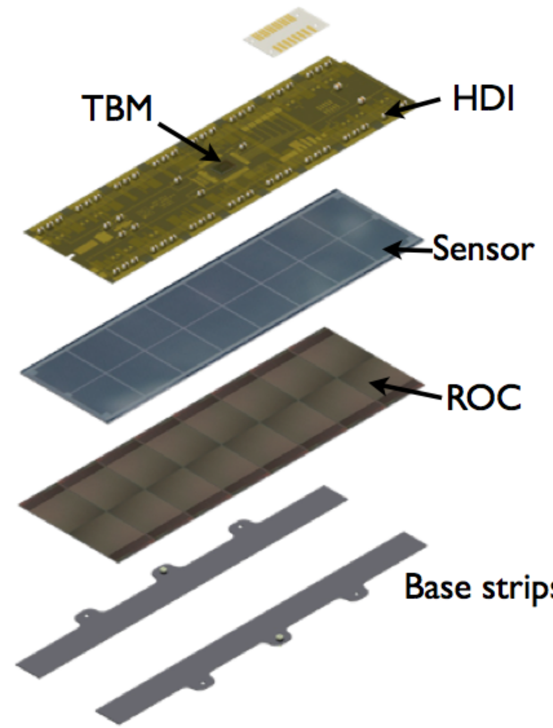
- b-tagging relies on track impact parameter & primary vertex resolutions → sensitive to improvements in the upgraded detector
- Study performed on simulated tt sample with Combined Secondary Vertex algorithm
- Significant enhancement in b-jet tagging efficiency at fixed fake rates from mis-identification of charm and light jets
    - result of 4th pixel layer and smaller inner layer radius



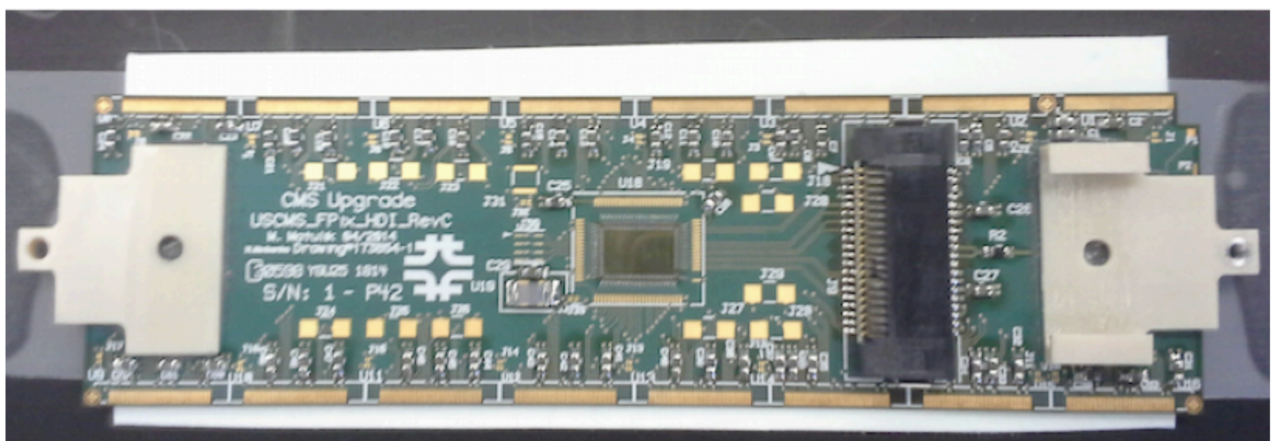


Pixel Modules

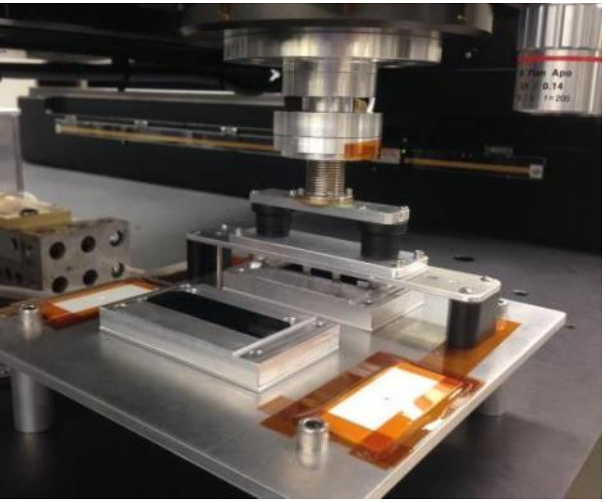
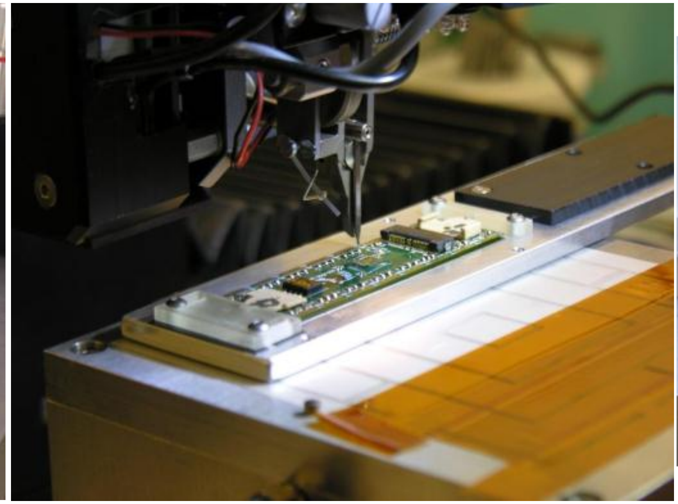
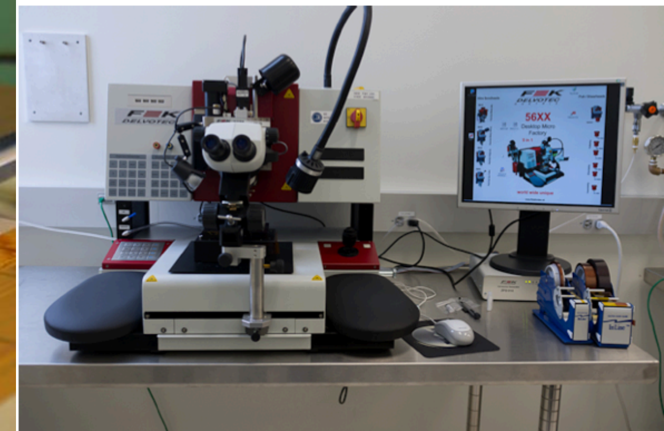
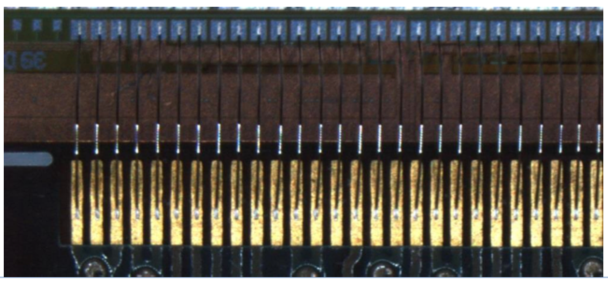
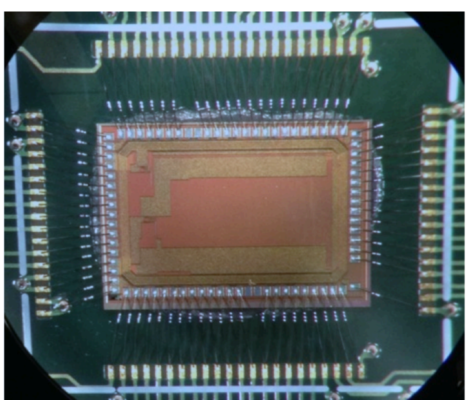
- Upgraded detector has one type of sensor module w/ active area of 16.2 x 64.8 mm^2
- Sensor is bump-bonded to 2x8 ROCs and ROCs are wire-bonded to a high density interconnect (HDI) glued to the sensor
- The Token Bit Manager (TBM) controls the readout of the ROCs and distributes clock, trigger and resets



Fully populated HDI (FPIX)



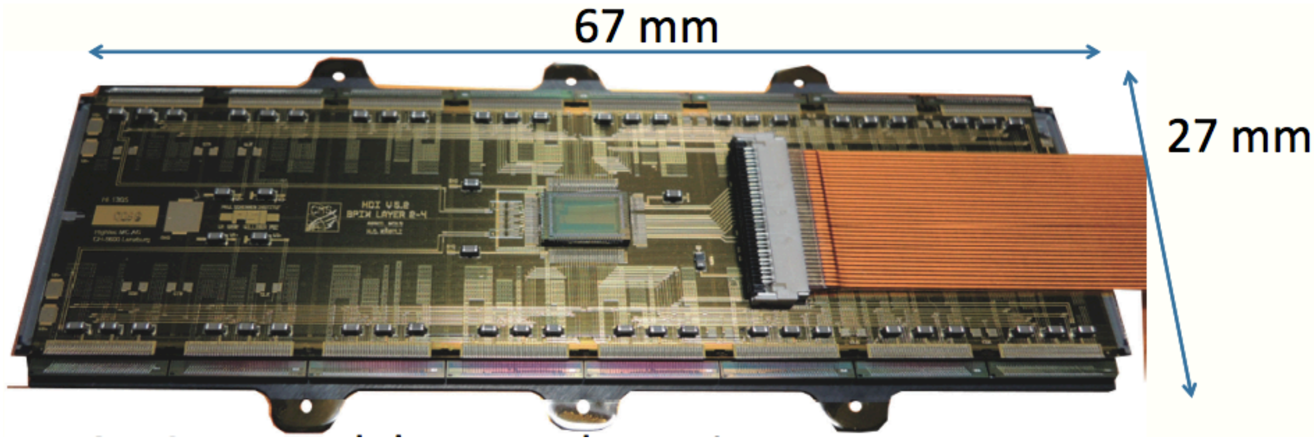
Module Production

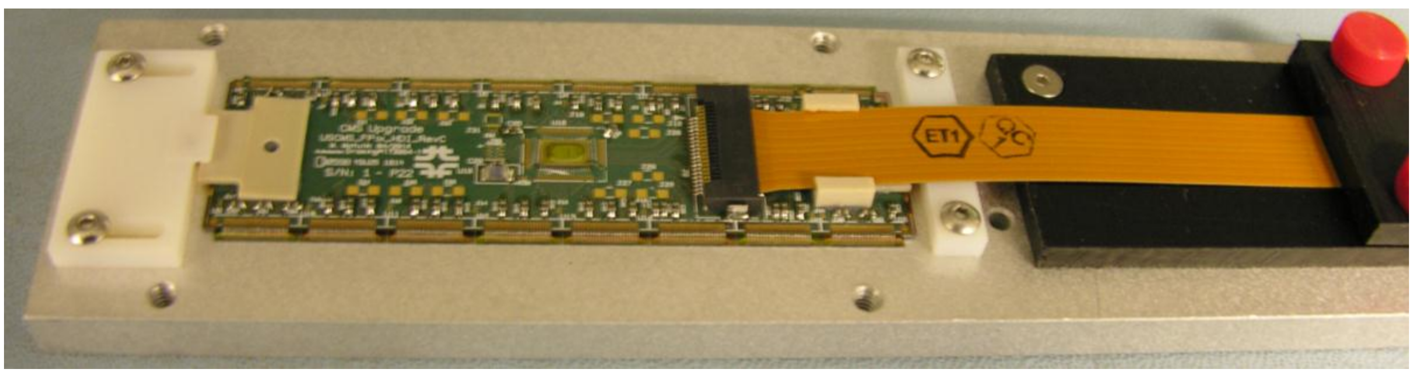
- Assembled several modules with prototypes and pre-production components.
  - Fully populated HDI (surface mount components + TBM wire-bonded)
  - Bare module (sensor bump-bonded to ROCs)
  - Glue HDI to bare module
  - Wire-bonding of ROCs to HDI
  - Visual inspection and detailed qualification tests for components and at each stage of assembly

Pixel Modules

BPIX Module



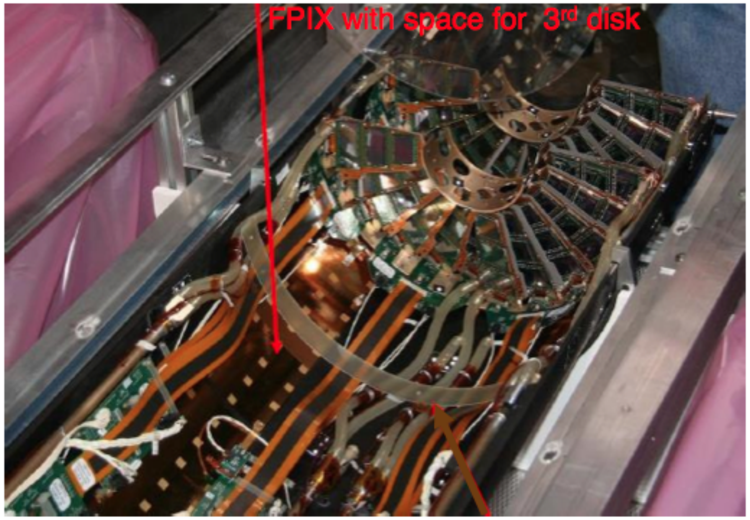
FPIX Module



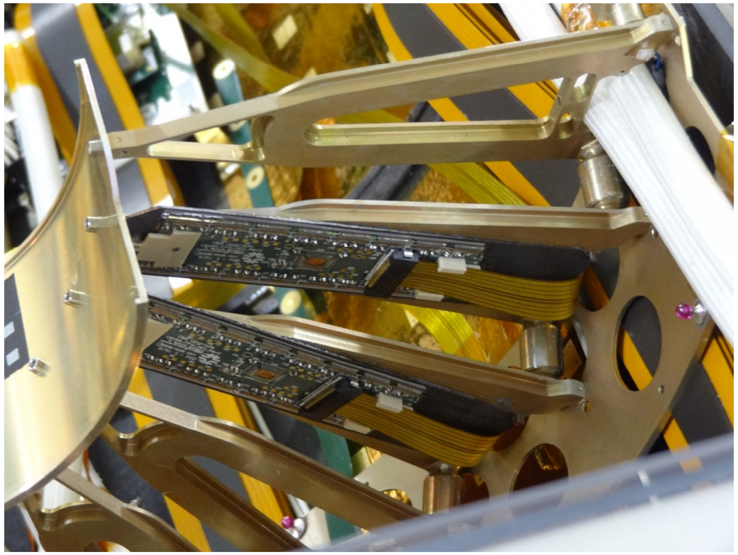
See the poster by Mercedes Moya for details on “Module Production and Qualification Tests”

Pilot System

- 8 modules with new digital readout chain installed into present FPix during LS1 (2014) and will be operated during 2014-2016
  - Use pre-production components
  - Use existing power, cooling and optical fiber infrastructure from present system
- Operational experience with LHC realistic conditions will be valuable for the full detector commissioning and operation
  - Firmware / Software development tool



Half disk with pilot modules

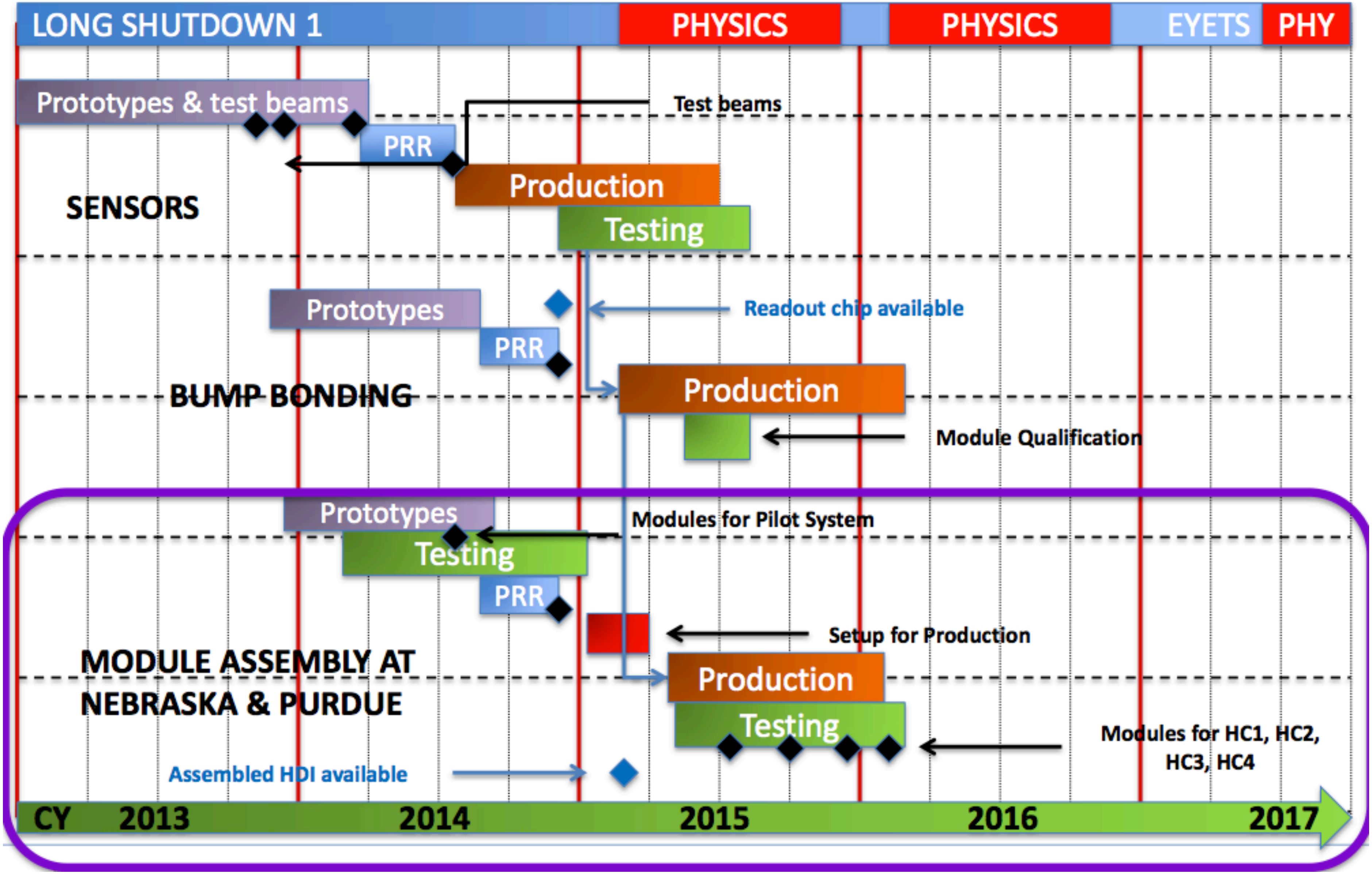


Summary

- Upgrade of the CMS pixel detector motivated by excellent performance of LHC as well as accumulated radiation damage
- Phase 1 upgrade with additional detector layer, reduced material budget and improved readout will maintain or even improve performance of the current detector at 50 pile-up or higher
- Detailed simulations show improved detector performance in the high data rate environment
- Upgraded pixels will be installed into CMS during 2016/2017 extended year-end shutdown with minimum impact on other detector components
- Few modules (pilot system) installed into CMS forward pixel to gain operational experience and commission the DAQ

CMS Technical Design Report for the Pixel Detector Upgrade
http://cds.cern.ch/record/1481838?ln=de

Schedule



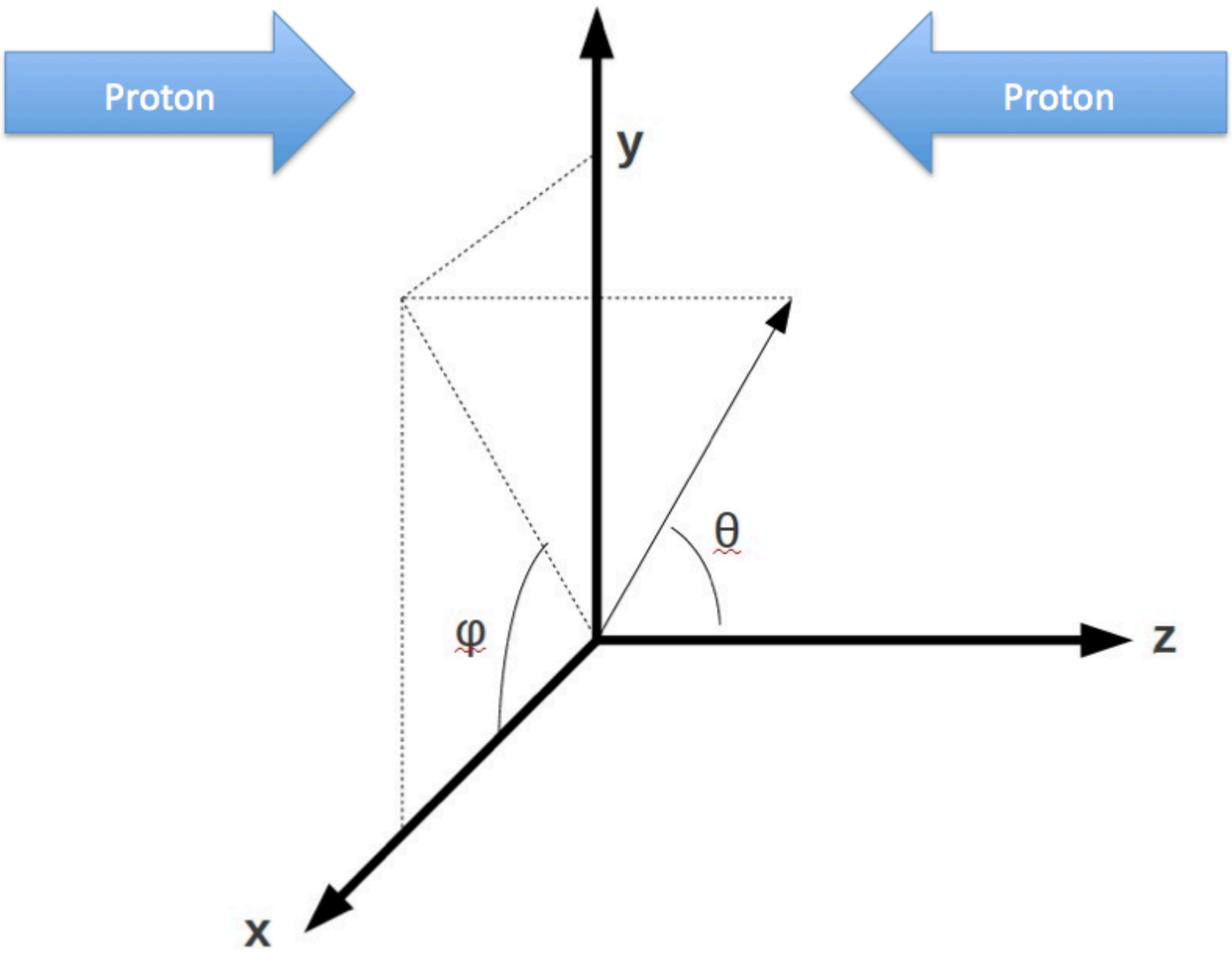
LONG SHUTDOWN 1
PHYSICS
PHYSICS
EYETS
PHY
Prototypes & test beams
Test beams
PRR
Production
Testing
SENSORS
Prototypes
Readout chip available
PRR
Production
BUMP BONDING
Module Qualification
Prototypes
Modules for Pilot System
Testing
PRR
Setup for Production
MODULE ASSEMBLY AT
NEBRASKA & PURDUE
Production
Testing
Modules for HC1, HC2,
HC3, HC4
Assembled HDI available
CY 2013
2014
2015
2016
2017

Upgrade : Change in parameters

University at Buffalo
The State University of New York

Parameter of Pixel System	Present	Upgrade
# layers (tracking points)	3	4
beam pipe radius (outer)	29.8 mm	22.5 mm (LS1)
innermost layer radius	44 mm	29.5 mm
outermost layer radius	102 mm	160 mm
pixel size (r-phi x z)	100μ x 150μ	100μ x 150μ
In-time pixel threshold	3400 e	1800 e
pixel resolution (r-phi x z)	13μ x 25μ	13μ x 25μ (or better)
cooling	C_6F_{14} (monophase)	CO_2 (biphase)
material budget X/X_0 (η=0)	6%	5.5%
material budget X/X_0 (η=1.6)	40%	20%
pixel data readout speed	40MHz (analog coded)	400Mb/sec (digital)
1st layer module link rate (100%)	13 M pixel/sec	52 M pixel/sec
ROC pixel rate capability	~120 MHz/cm²	~580 MHz/cm²
control & ROC programming	TTC & 40MHz I²C	TTC & 40MHz I²C

CMS Coordinate System



Tracker Radiation Dose

1 Gy = 100 Rad

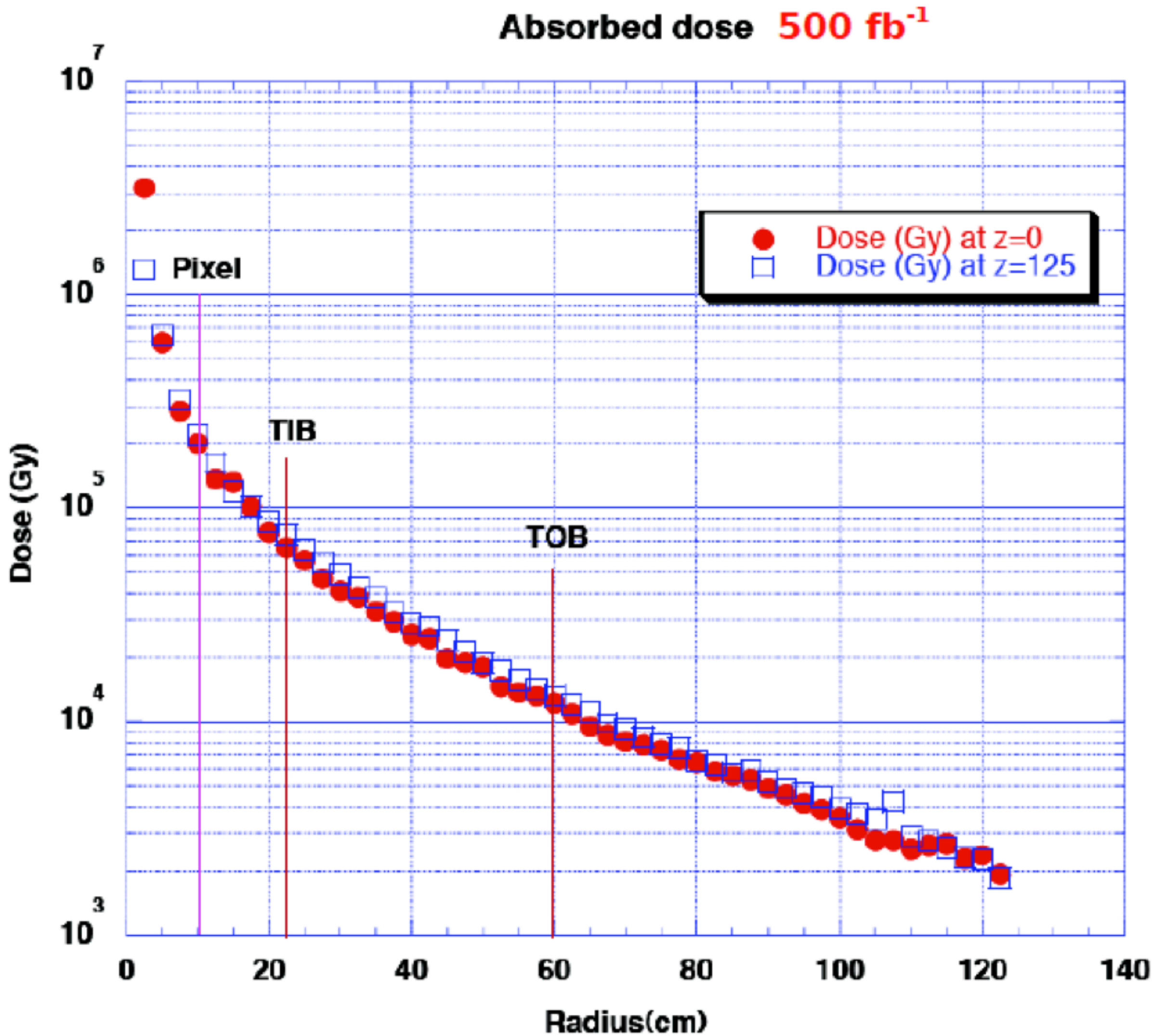
500 fb^{-1}

Layer 1: 200 MRad

Layer 2: 50 MRad

Layer 3: 20 MRad

Layer 4: 13 MRad



Fluence:

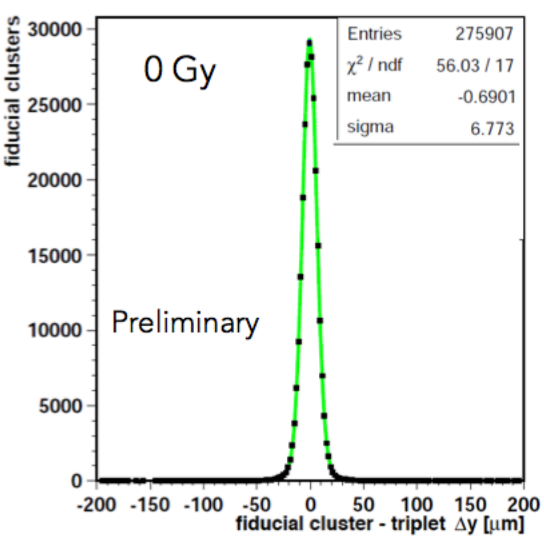
1 MRad ≃ 3 10^{13}/cm^2 pions

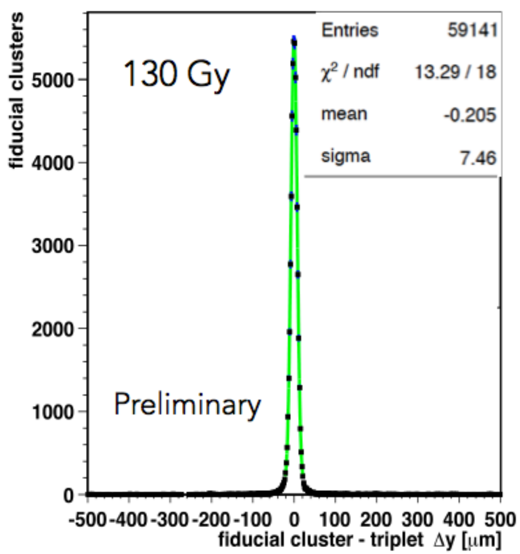
Pixel upgrade TDR 2012

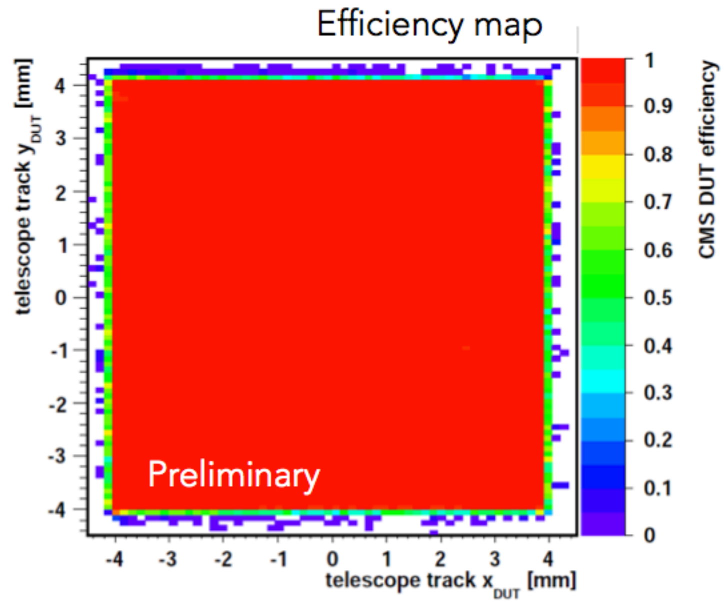
Irradiation Studies

Irradiated at CERN PS with 24GeV protons
$\phi = 3.77 \times 10^{14}$ p/cm^{-2} → 130 kGy
(Full layer 4 lifetime dose)

Threshold: ~1.5 ke
Full depletion at V_{bias} = -200 V







Remains 99.8% efficient in fiducial volume

After Irradiation: Spatial resolution ~6.2 μm (before ~5.1μm)

Module Testing

- Module functionality tests to discover any problem with bump-bonding, pixel readout, module assembly etc.
  - Sensor IV tests on bare modules
  - Tests on assembled modules
    - Pre-tests to set ROCs current, threshold and delays
    - ROC functionality tests to check pixel readout, address decoding
    - Bump-bond tests
    - Performance/calibration of all pixels including pedestal and noise tests, pulse height test etc.
  - Thermal cycling of unpowered modules: >10 cycles to validate mechanical stress.
  - Repeat tests after thermal cycling
  - More detailed tests using x-rays to validate electronic bump-bonding tests