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The CMS Pixel Readout Chip for the Phase 1 Upgrade

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The present CMS pixel Read Out Chip (ROC) has been designed for operation at 25 ns and to be efficient up to the nominal instantaneous luminosity of 10^{34} cm^{-2}s^{-1}. Based on the excellent LHC performance to date, and the upgrade plans for the accelerators, it is anticipated that the instantaneous luminosity could reach 2×10^{34} cm^{-2}s^{-1} before Long Shutdown (LS) 2 in 2018, and well above this by LS3 in 2022. That's why a new ROC has been designed and a completely new pixel detector will be built with a scope of its installation in CSM during an extended winter shutdown in 2016/17. The ROC for the upgraded pixel detector is an evolution of the present architecture. It will be manufactured in the same 250 nm CMOS process. The core of the architecture is maintained, with enhancement in the performance in three main areas: readout protocol, reduced data loss and enhanced analog performance. The main features of the new CMS pixel ROC are presented together with measured performance of the chip.

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