Novel Active Signal Compression in Low-noise Analog Readout at Future XFEL Facilities

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On behalf of the

PixFEL Collaboration[1,2,3]

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Motivation

- The electronic instrumentation developed for FEL experiments has to satisfy severe requirements in terms of space and amplitude resolution, frame rate, input dynamic range and frame storage capability
- Covering the wide (1 to 10000 photons @ 1 keV to 10 keV) input dynamic range while preserving single photon resolution at small signals is one of the most challenging tasks
- In order to fit this dynamic range into a reasonable output signal range a strongly non-linear characteristic is required
- Signal compression can be achieved
  - at sensor level (as in the case of the DSSC)
  - at front-end level (like in the AGIPD and LPD detector)
- A novel solution, based on the non-linear features of a MOS capacitor, is proposed
- Technology TSMC 65 nm, pixel pitch of 100 μm
- The work has been carried out in the frame of the PixFEL project[1] approved by the Istituto Nazionale di Fisica Nucleare (INFN) and started in 2014

[1] G. Rizzo, "The PixFEL project: development of advanced X-ray pixel detectors for application at future X-FEL facilities"

Outline

Dynamic compression with MOS capacitor

- Inversion-mode MOS capacitor
- Gain setting
- Improved gain accuracy

Readout channel for FEL application

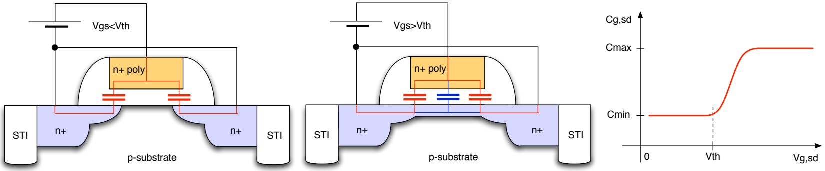
- Charge sensitive amplifier with dynamic signal compression
- Transconductor for V-to-I conversion
- Time-variant filter
- Analog-toDigital Converter

Readout channel performance

- Channel dynamic performance
- System noise analysis
- Considerations for single photon detection

Inversion-mode MOS capacitor

Drain and source shorted to form one capacitor terminal, the gate forms the other



- $0 < V_{G,SD} << V_{Th}$ → $C_{G,SD}$ is set at its minimum and it is mainly due to the overlap gate-to-source $C_{gs,ov}$ and gate-to-drain $C_{gd,ov}$ capacitances:

$$C_{min} \approx C_{gs,ov} + C_{gd,ov} = 2W\Delta L C_{ox}$$

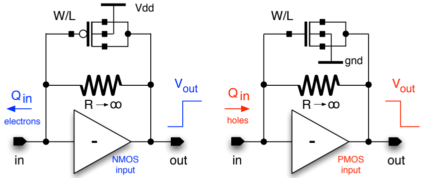
  W = channel width, ΔL = extension of the overlap region, C_{ox} = gate oxide capacitance per unit area

- $V_{G,SD} >> V_{Th}$ → $C_{G,SD}$ shows a maximum value which is mainly given by the gate-to-channel C_{gc} capacitance

$$C_{max} \approx C_{gc} = WLC_{ox}.$$

Basic idea: exploit the non-linear features of MOS capacitors to dynamically change the gain of Charge Sensitive Amplifier with the input signal amplitude

Dynamic compression with MOS capacitor



- Low energy photons

$$\Delta V_{out} << V_{th} \Rightarrow C_f = C_{min}$$

- High energy photons

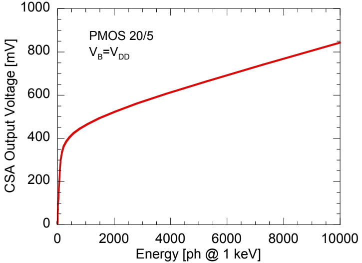
$$\Delta V_{out} >> V_{th} \Rightarrow C_f = C_{max}$$

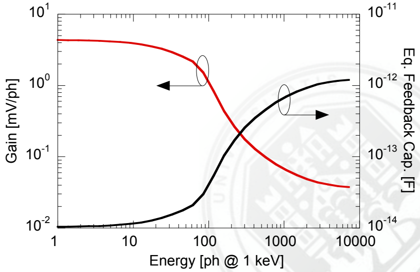
Charge Sensitive Amplifier Gain

$$G = \frac{dV_{out}}{dph}$$

Equivalent feedback capacitance

$$C_{ef} = 280q \left[\frac{dV_{out}}{dph} \right]^{-1}$$





Gain setting

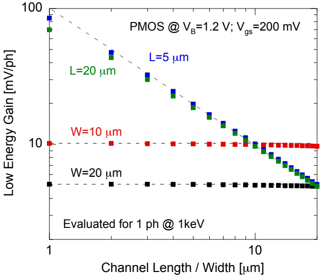
Low Energy Gain (G_{le}) ($E < 10$ ph at 1 keV)

If $V_{out} << V_{th} \Rightarrow C_{gs} = C_{min}$

$$C_{min} \approx C_{gsovl} + C_{gdovl} = 2W\Delta L C_{OX}$$

$$G_{le} = 280q \frac{1}{2\Delta L C_{OX}} \frac{1}{W}$$

$\Rightarrow G_{le}$ adjusted with the MOS channel width W



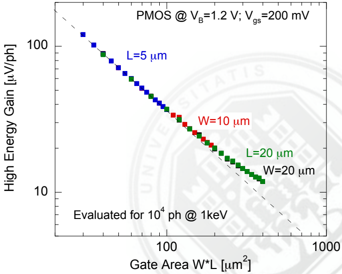
High Energy Gain (G_{he}) ($E > 10^3$ ph at 1 keV)

If $V_{out} > V_{th} \Rightarrow C_{gs} = C_{max}$

$$C_{max} \approx C_{gs} + C_{gd} = WLC_{OX}$$

$$G_{he} = 280q \frac{1}{C_{OX}} \frac{1}{WL}$$

$\Rightarrow G_{he}$ adjusted with the MOS channel length L

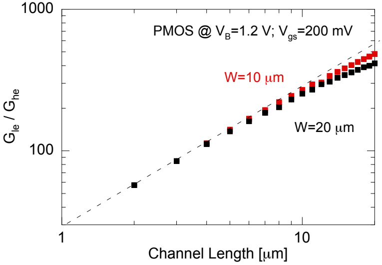


Low to High Energy Gain ratio (G_{le}/G_{he}) setting

Signal compression factor (the ratio of the slopes at small and large signals) is

$$k = \frac{G_{le}}{G_{he}} = \frac{C_{max}}{C_{min}} \approx \frac{L}{2\Delta L}$$

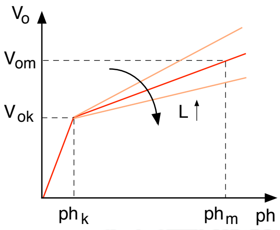
$\Rightarrow$ k depends only on the channel length L



Signal compression factor fixed by

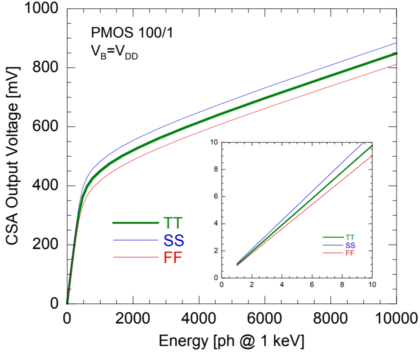
$$k = \frac{ph_m - ph_k}{V_{om} - V_{ok}} G_{le} \approx \frac{ph_m}{V_{om} - V_{ok}} G_{le}$$

- V_{om} maximum range at CSA output
- V_{ok} voltage at which the kink occurs ($\approx V_{th}$)
- ph_m maximum number of photons
- ph_k number of photons at the kink ($ph_k << ph_m$)



Low and High Energy Gain accuracy

Gain accuracy might be affected by process parameters variation



	G_{le} [mV/ph]	G_{he} [μV/ph]
TT	0.99	37.6
SS	1.06	37.8
FF	0.90	37.2

- Low Energy Gain inaccuracy

  ± 10 %

  mainly due to ΔL and t_{ox} mismatch

- High Energy Gain inaccuracy

  ± 1 %

  mainly due to t_{ox} mismatch

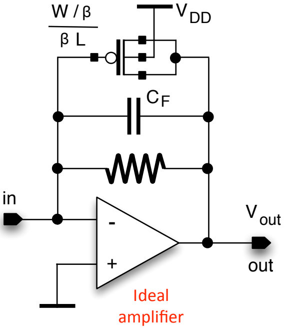
- Output voltage range variation

  ± 4 %

  mainly due to V_{Th} mismatch

Improved Low Energy Gain accuracy

Additional capacitance C_F in parallel to the feedback MOS



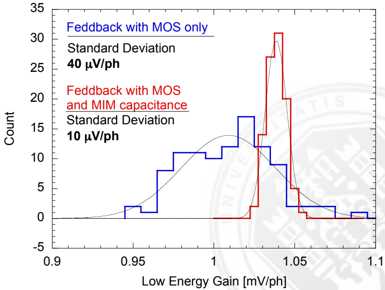
$$C_F = \left(1 - \frac{1}{\beta}\right) C_{min}$$

$$W \rightarrow \frac{W}{\beta} \quad \text{and} \quad L \rightarrow \beta \cdot L$$

with $\beta > 1$(the higher the value of β, the lower the inaccuracy)

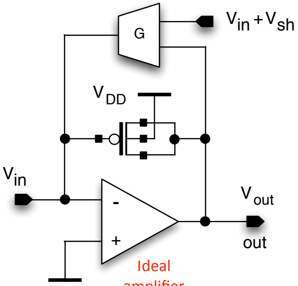
Improved feedback for $\beta = 5$

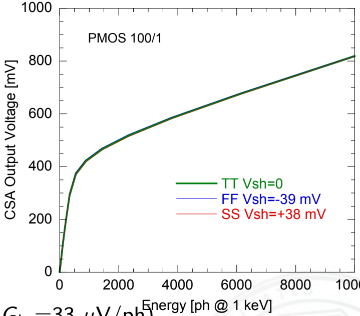
- $C_F = 34$ fF MIM cap
- $W = 20$ μm and $L = 5$ μm



Improved output voltage range accuracy

The shift in the high energy range can be (virtually) cancelled by trimming the gate-to-source voltage V_{GS} of the feedback MOS



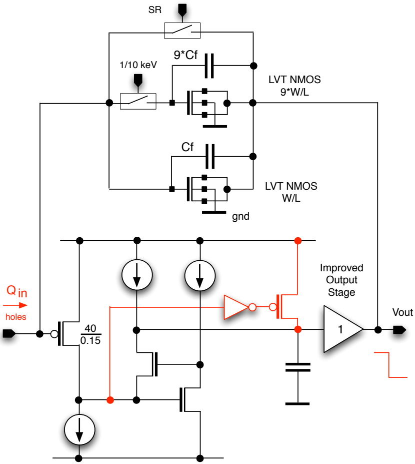


Error (in photons) evaluated at 10^4 ph at 1 keV (G_{he}=33 μV/ph)

V_{sh} [mV]	+38	0	-39
SS	+9	+1060	
FF		-1060	-3

Note: inaccuracy introduced by the transconductor itself and by the DAC providing V_{sh} not considered

Complete CSA for FEL applications



Forward gain stage

- active folded cascode (with local feedback) loaded by an active load
- Input device PMOS W/L=40/0.15

Feedback MOS

- NMOS W/L=10/4
- NMOS W/L=9·10/4

Improved output stage

- drive the large feedback capacitance

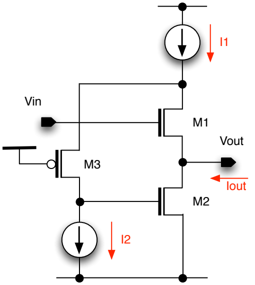
Reset network

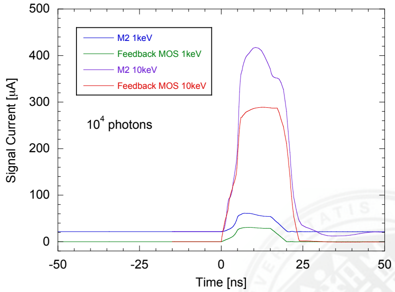
- to speed up the slew-rate limited reset phase

Amplifier main features	
Open Loop DC Gain	60 dB
Open Loop GBP	140 MHz
Phase Margin (Cef=10pF)	52 deg
Power Consumption	100 μW

Improved output stage

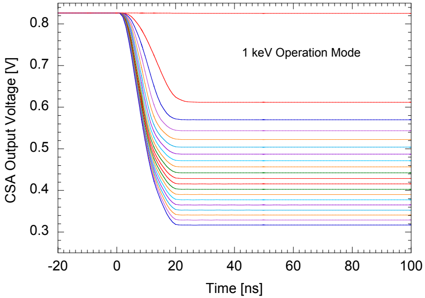
- The output stage must sink a current of 400 μA in the worst case (10^4 ph @ 10 keV)
- Standard PMOS source-follower is not adequate since its gate-to-source voltage would severely limit the negative output voltage swing
- $\Rightarrow$ improved output stage based on the *White follower* scheme has been adopted

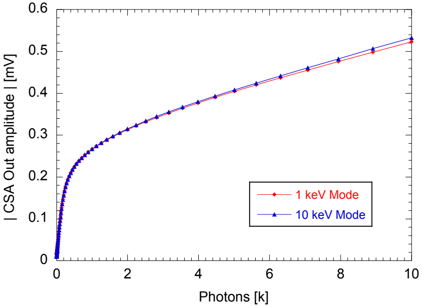




- M1 acts as source-follower
- M_2 acts as a controlled current sink providing a path for feedback capacitance current
- The current provided by M2 is controlled by the feedback loop M1, M2 and M3

CSA response and dynamic range

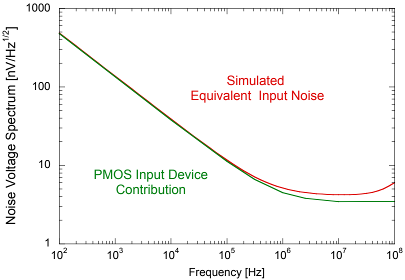




- Rise time: $t_r \approx 20$ ns for a detector signal collected in 15 ns
- Low energy gain: $G_{le} \approx 1.0$ mV/ph
- High energy gain: $G_{he} \approx 25\ \mu$V/ph
- Compression factor: $k \approx 40$
- Dynamic range: the CSA covers the full dynamic range of 10^4 photons

CSA noise performance

Equivalent Input Noise



Dominated by the PMOS input device noise

- White noise components

$$S_W = 4.16 \frac{nV}{\sqrt{Hz}}$$

- $1/f$ noise coefficient

$$A_f = 3.7 \cdot 10^{-11} V^2$$

Equivalent Noise Charge evaluation

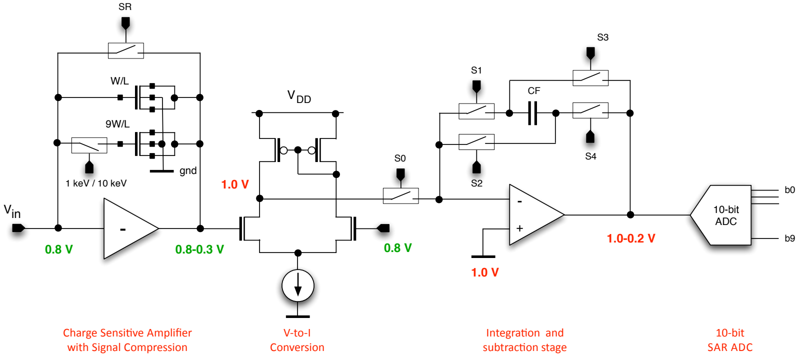
$$ENC^2 = C_T^2 \left(\frac{A_1}{\tau} S_w + 2\pi A_2 A_f \right)$$

$$ENC = 50e - rms$$

$\Rightarrow$ SNR=5.6 for 1 ph @ 1 keV

- $C_T = C_D + C_{in} + C_f + C_{stray}$
- A_1=1, A_2=0.69 shaping coefficients for a trapezoidal weighting function
- τ =50 ns Integration time

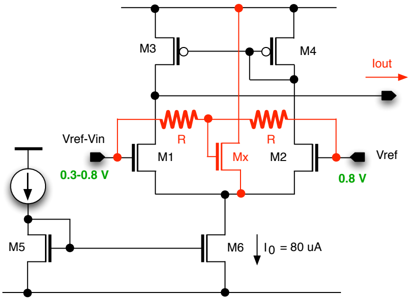
Complete readout channel

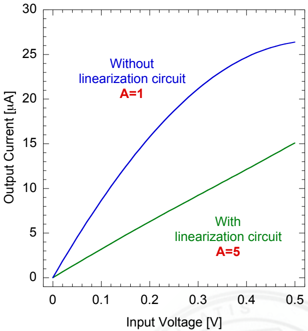


- Charge-sensitive preamplifier with dynamic signal compression
- Transconductor for voltage-to-current conversion
- Time-variant filter with gain and integration time selection options
- Analog-to-Digital conversion performed by a 10 bit SAR ADC

Transconductor for V-to-I conversion

Wide input range (0.5 V) ⇒ additional circuit (in red) to linearize the characteristic





$$G_m = \frac{\sqrt{1\beta_{1,2} I_0}}{A} V_{in}\sqrt{1-\frac{\beta_{1,2}^2 V_{in}^2}{2I_0}} \quad \text{with} \quad A=\sqrt{1+\frac{\beta_X}{2\beta_{1,2}}}$$

where $\beta_{1,2}=\frac{1}{2}\mu_0 C_{ox}\frac{W_{1,2}}{L_{1,2}}$ and $\beta_x=\frac{1}{2}\mu_0 C_{ox}\frac{W_x}{L_x}$

V-to-I main features	
Gain	30 μA/V
Power	120 μW

Gated integrator: Flip Capacitor Filter

Events with a known repetition rate ⇒ time variant shaping

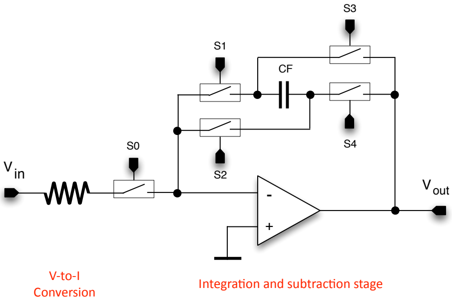
- Reduced time to return to base, provides the sample to ADC at its output

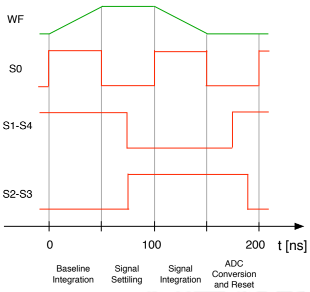
Trapezoidal weighting function

- Gated integrator and Correlated Double Sampling (CDS)

Flip Capacitor Filter[2]

- Trapezoidal weighting function achieved by flipping the feedback capacitor C_F

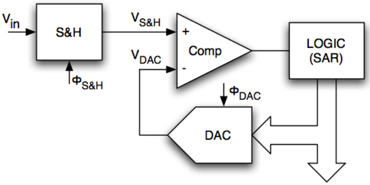




2 L. Bombelli, C. Fiorini, S. Facchinetti, M. Porro, G. De Vita, *NIM*, vol. 624, pp. 360-366, 2010.

10-bit Successive Approximation Register ADC

- guarantees single photon resolution at small signal
- small quantization noise in Poisson-limited regime
- 5 MHz sample rate (for operation at the Eu-XFEL) SAR ADC
- Clock frequency = 5 MHz × 11 = 55 MHz



DAC Architecture

2 standard splitted Capacitive DAC in a pipeline structure to avoid high current peaks

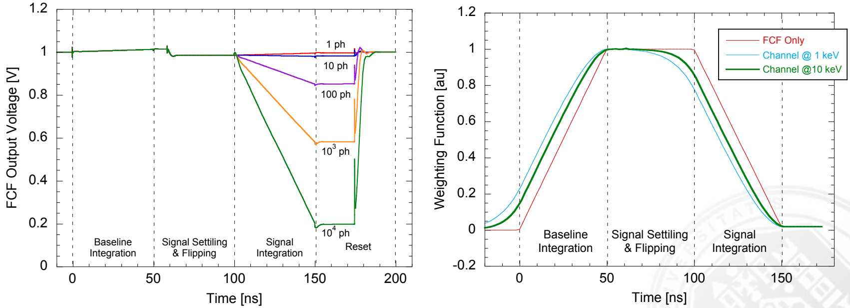
- an entire conversion period dedicated to precharge one DAC input capacitance (≈2.5 pF)
- while the other DAC performs the conversion

Present simulation results

- C_{min}= 35 fF to ensure 3σ matching within 0.5 LSB
- Area ≈ 5000 μm^2
- Static Power Consumption ≈ 70 μW
- Average power consumption in a conversion period ≈ 85 μW
- SNR = 57.75 dB
- ENOB = 9.3

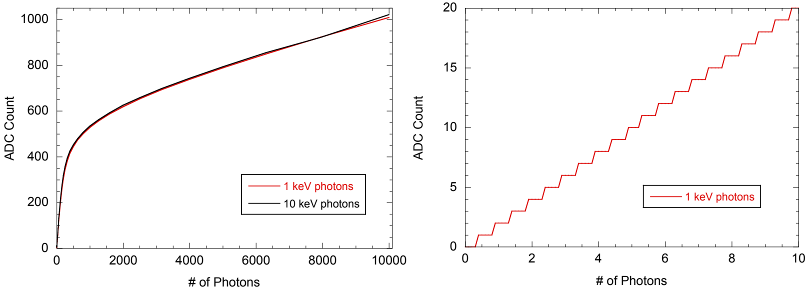
Filter transient response

- Channel simulated by referring to the time constraints of the Eu-XFEL laser $\Rightarrow$ macro bunches of light pulses separated from each other by 200 ns
- The period has been subdivided into four equal intervals $\Rightarrow$ integration time $\tau = 50$ ns



Weighting function: the deviation from the ideal trapezoidal shape is due to the switches timing and to the finite rising time of the CSA

Channel dynamic performance



- ADC dynamic range well covered
- Bilinear characteristic
- 2 ADC bins attributed to 1 photon in the linear region
- First 10 photons well detected

System noise analysis

Electronics Noise

- due to the analog front-end
- increases with the increase of the signal
- ENC 60 e- rms @ τ=50 ns
  $\Rightarrow$ SNR of 4.6 for single photon

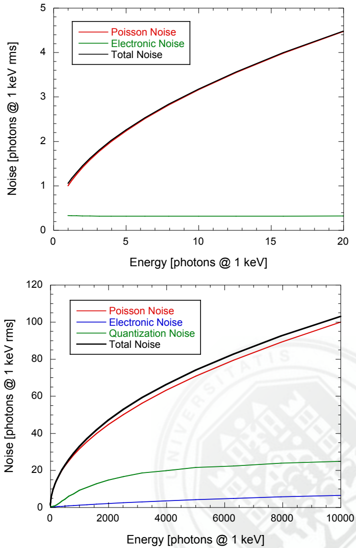
Quantization noise

- introduced by the ADC
- Very low number of incoming photons
  linear region $\Rightarrow$ no quantization noise
- High number of collected photons
  $\approx$ number of photons attributed to the same bin divided by $\sqrt{12}$

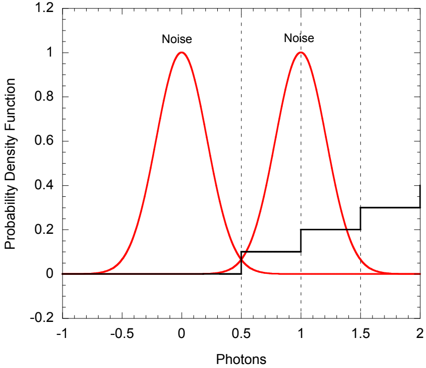
Noise of the Poisson distributed photon generation process

Conclusion

The total noise of the system is dominated by the Poisson photon generation noise



Single photon detection



Assume

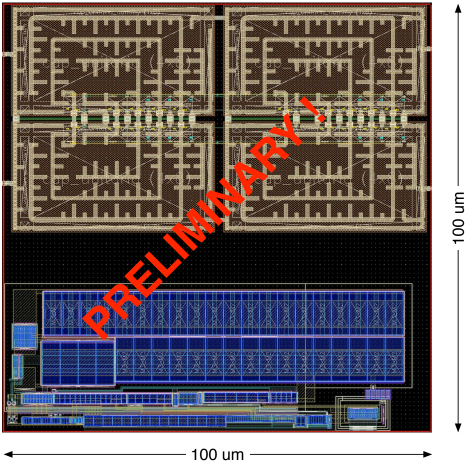
- Gaussian distribution for the electronic noise with

$$ENC = 60e - rms$$

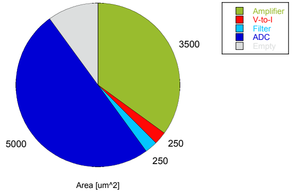
- ADC threshold of the 2^{nd} bin placed @ 1^{st} photon

- The probability that a zero signal is misinterpreted as a one photon signal is 1%
- The probability that 1 photon signal is correctly attributed to the first 2 bins is 98%

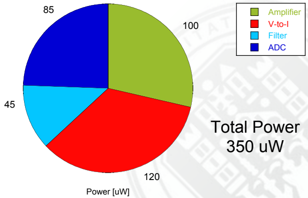
Pixel overview



Area occupancy



Power Consumption



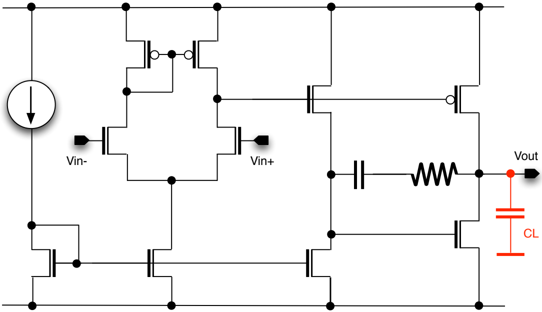
Conclusions

- A novel active signal compression based on the non-linear features of a MOS capacitor has been investigated
- The front-end has been included in a readout channel for operation at FEL facilities
- Circuit simulations have shown that the proposed read-out channel
  - achieves a dynamic range of 10^4 photons at 1 or 10 keV
  - preserve at the same time single 1 keV photon resolution with 98% accuracy
  - can be operated at a rate of 5MHz
- A test chip including single test structures and an 8×8 matrix will be submitted at the end of September 2014

Backup Slides

Filter amplifier

- Two stages AB class Operational Transconductance Amplifier (OTA)
- AB class amplifier to drive the large (2.5 pF) ADC capacitance since it is able to deliver currents larger than the quiescent value



Amplifier main features	
DC Gain	53 dB
GBP	402 MHz
Phase Margin	62 deg
Power	45 μW