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Novel Active Signal Compression in Low-noise Analog Readout at Future XFEL Facilities

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This work presents the design of a low-noise front-end implementing a novel active signal compression technique. This feature can be exploited in the design of analog readout channels for application to the next generation free electron laser (FEL) experiments. The readout architecture includes the low-noise charge sensitive amplifier (CSA) with dynamic signal compression, a time variant shaper used to process the signal at the preamplifier output and a 10 bit successive approximation register (SAR) analog-to-digital converter (ADC). The channel will be operated in such a way to cope with the high frame rate (exceeding 1 MHz) foreseen for future XFEL machines. The choice of a 65 nm CMOS technology has been made in order to include all the building blocks in the target pixel pitch of 100 um. This work has been carried out in the frame of the PixFEL project funded by Istituto Nazionale di Fisica Nucleare (INFN), Italy. The members of the PixFEL Collaboration are affiliated with Università di Bergamo, Università di Pavia, Università di Pisa, Università di Trento and INFN, Italy.

Summary

X-ray free electron laser (FEL) experiments require electronic instrumentation able to cope with severe requirements in terms of space and amplitude resolution, frame rate, input dynamic range and frame storage capability. Covering the extremely wide input dynamic range from 1 to 10^4 photons at fixed energy (which may change between about 1 keV and 10 keV according to the specific experiment) while preserving single photon resolution at small signals (up to about 10^2 photons) is one of the most challenging tasks in developing readout channels for FEL applications. This wide dynamic range can be fitted into a reasonable signal swing at the channel output, only if a compression is achieved at sensor level, as in the case of the DSSC device [1], or front-end level, like in the LPD detector [2].

In this work, an innovative solution, based on the non-linear features of a MOS capacitor [3] used as the feedback network of a charge amplifier, is proposed. The gate of the device forms one capacitor terminal connected to the amplifier input which is held at a fixed voltage (Vin), whereas the drain and source terminals are shorted together to form the other capacitor terminal connected to the amplifier output (Vout). The device polarity is chosen in relation with the detector characteristics: a PMOS for a detector collecting electrons and an NMOS for one collecting holes. With this choice, if the voltage of the gate connection is properly fixed (close to gnd for PMOS and close to VDD for NMOS) the device is operated in inversion, yielding a strongly non-linear C-V characteristic and thus providing a compression at the output of the amplifier. Since low energy photons generate an output voltage step with amplitude |ΔVout| much lower than the device threshold Vth, the equivalent feedback capacitance Cf provided by the MOS device is set at its minimum and is mainly due to the overlap gate-to-source Cgs,ov and gate-to-drain Cgd,ov capacitances. Therefore, Cf,min ≈ 2W ΔLCox, where W is the device channel width, ΔL is the extension of the overlap region and Cox is the gate oxide capacitance per unit area. Therefore, in the low energy range (<10^2 photons) the gain of the preamplifier is almost independent of the MOS channel length L and can be adjusted by carefully choosing the channel width W. For high energy photons, the output voltage is expected to exceed the threshold thus showing a maximum Cf which is mainly given by the gate-to-channel Cgc capacitance Cf,max ≈ W LCox. Therefore, in the high energy range (>10^3 photons) the gain depends on the MOS gate area WL and can be set with a suitable design of the MOS channel length L (once W has been properly chosen for the low energy gain setting). With respect to other compression solutions under investigation for FEL experiments, the one proposed here has the advantage of being based on a standard CMOS technology (not on a customized process, as in the case of the DSSC device) and on a single channel with dynamically changing gain (not on the parallel configuration of channels with different gain, like in the case of the LPD and the Percival detectors).

The full readout processor developed in the frame of the PixFEL project includes, beside the charge amplifier with signal compression, the shaping stage, the Sample&Hold capacitor and a 10-bit SAR ADC. Since the readout channel will be bump-bondend to a hole collecting pixel sensor, an NMOS has been used as the non-linear feedback capacitor. Starting from the compression idea proposed above, a more complex feedback network has been worked out as will be shown at the time of the conference. The device dimensions have been chosen to have a low energy gain of about 0.4 mV/ph and an output dynamic range of the amplifier of 500 mV. The forward stage of the amplifier is realized with a classical folded cascode architecture with a PMOS input device to cope with the bias requirements of the feedback MOS. Moreover, an improved output stage has been used to provide the high current values required during the integration and reset phases. The second stage of the analog chain is a linear transconductor introduced to convert the voltage at the output of the charge amplifier into a current, which is then fed to the input of the subsequent shaping stage. Since FEL facilities generate events with a known repetition rate, a time-variant shaping stage has been adopted in this work. The proposed architecture is based on the Flip Capacitor Filter (FCF) idea [4], which applies a Correlated Double Sampling (CDS) technique to obtain, with a single integrator stage and a flipped feedback capacitor, a trapezoidal weighting function. The channel has been simulated by referring to the time constraints of the European XFEL laser, whose beam structure consists of macro bunches of light pulses separated from each other by 200 ns. As a first attempt, in the shaper operation the period can been subdivided into four equal intervals of 50 ns each. In agreement with the CDS sequence, the readout cycle starts with the baseline integration. Then the charges generated by the laser pulse are collected by the detector and the FCF feedback capacitor gets flipped. A second integration is performed in the subsequent period measuring both the signal and the baseline (the baseline being subtracted due to the feedback capacitor flipping) to give the final output voltage. At the end of the cycle the feedback capacitances of the charge amplifier and filter are reset. With the simulated 50 ns integration time, an Equivalent Noise Charge (ENC) of 51 electrons rms has been obtained, thus providing a signal-to-noise ratio of 5.5 for a single photon with an energy of 1 keV. At the time of the conference a thorough analysis of the readout processor and the details of the simulation results will be presented.

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