Upgrade of the ALICE Inner Tracking System

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Outline

1. Introduction
2. The Upgraded ALICE ITS
   - Pixel Chip
   - Barrels and Staves
   - Flex Printed Circuit
   - Cooling
3. Summary and Outlook

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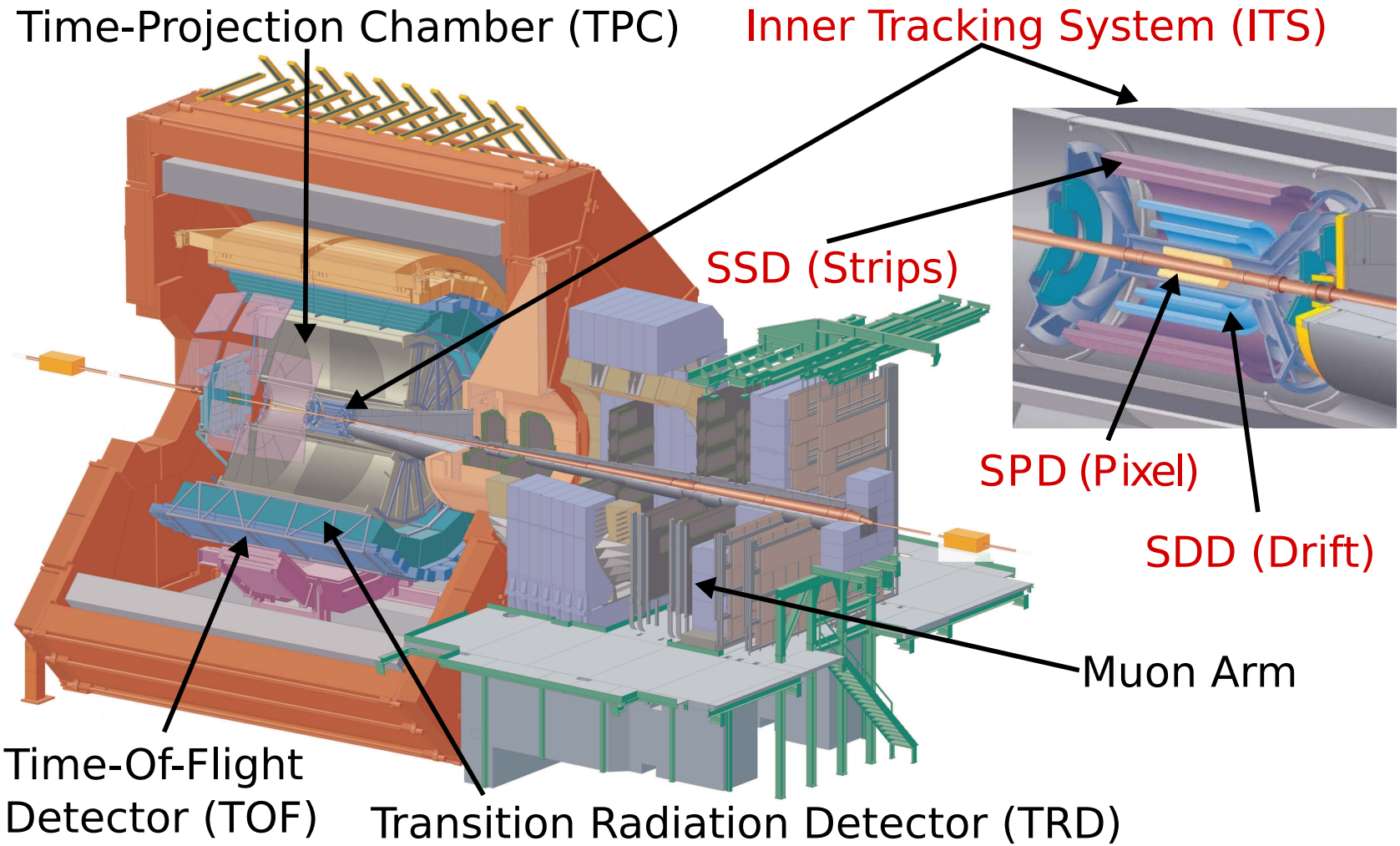
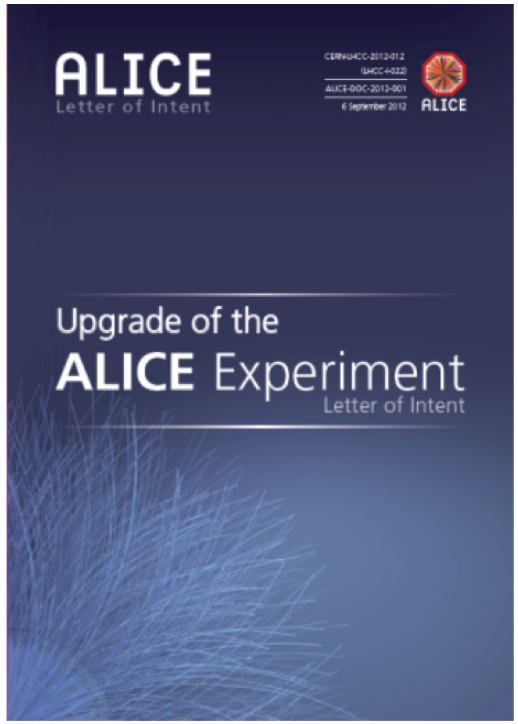
ALICE and the Current ITS



- ALICE is the heavy-ion focussed experiment at the LHC with the main goal to study strongly interacting matter

ALICE Upgrade Strategy

- Motivation: Focus on high-precision measurements of rare probes at low p_{T}
  - Cannot be selected by hardware trigger
  - Need to record large sample of events
- Goal: Pb-Pb recorded luminosity $\geq 10\,\mathrm{nb}^{-1}$ (Plus: pp and p-Pb data)
  - Gain of factor 100 in statistics for minimum bias
- Strategy: Read out all Pb-Pb interactions up to the maximum LHC collision rate of 50 kHz
- When: 2nd long LHC shutdown LS2 (2018/19)



ALICE

ALICE Upgrade Strategy (2)

- Upgrade of the Silicon Trackers
  - New high-resolution, low-material inner tracking system (ITS), covering mid-rapidity
  - New muon forward tracker (MFT) covering forward rapidity (silicon pixel telescope in front of the hadron absorber, in the acceptance of the muon spectrometer)
- Further Upgrade Items
  - New, smaller beam pipe
  - TPC: replacing of readout planes and electronics
  - Upgrade of forward trigger detectors (FIT) and ZDC
  - Upgrade of readout electronics of: TRD, TOF, PHOS and Muon Spectrometer
  - Upgrade of Online and Offline Systems

ITS Upgrade Design Objectives

- Improve impact parameter resolution by a factor 3(5) in $r\phi(z)$ at $p_{\mathrm{T}} = 500\,\mathrm{MeV/c}$
  - Move closer to IP; position of first layer: $39\,\mathrm{mm} \rightarrow 22\,\mathrm{mm}$
  - Further reduce the already low material budget, in particular in the inner layers: $\sim 1.14\%\,X_0 \rightarrow 0.3\%\,X_0$
  - Reduce pixel size: $50 \times 425\,\mu\mathrm{m}^2 \rightarrow \mathcal{O}(30 \times 30\,\mu\mathrm{m}^2)$
- Improve tracking efficiency and p_{T}-resolution at low p_{T}
  - Increase granularity
  - Increase number of layers from 6 to 7
- Fast readout (now limited to 1 kHz with full ITS)
  - Pb-Pb: 50 kHz, pp: 400 kHz
- Provide possibility to access for yearly maintenance
  - Fast insertion / removal

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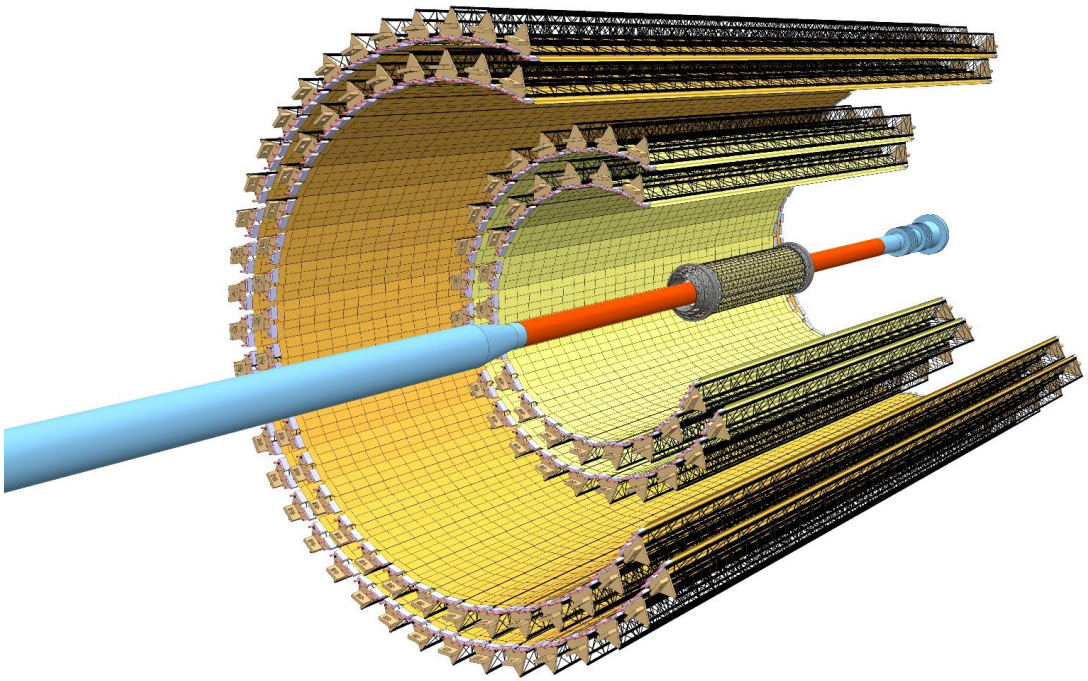
Layout of the Upgraded ITS

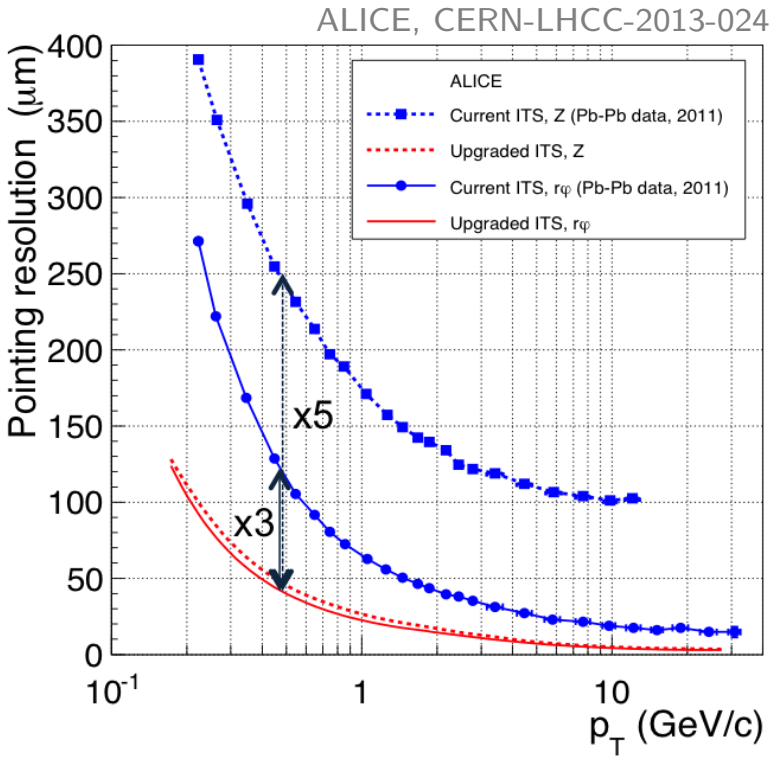


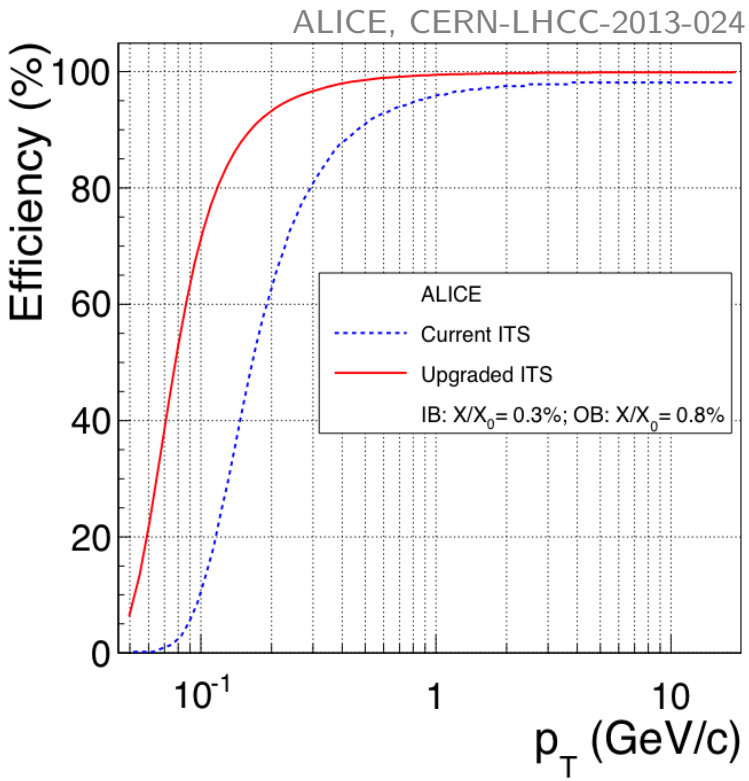
- 7 layers from r=22 mm to r=400 mm
- $\sim 10\,\mathrm{m}^2$ of silicon
- 12.5 GPixels

- Moderate radiation hardness required (at 30°C), expected radiation levels (innermost layer, safety factor of 10):
  - 700 krad (TID) and $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}cm^{-2}}$
- η coverage: $|\eta| \leq 1.22$, for tracks from 90% most luminous region

Expected Performance

- Expected improvement of impact parameter resolution (left) and tracking efficiency (right).





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Choice of Sensor Technology

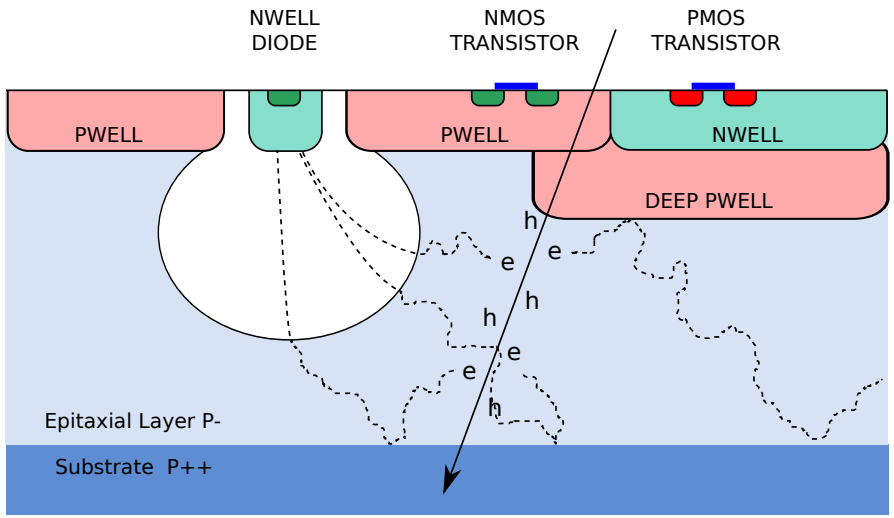
Requirements (TDR):

Parameter	Inner Barrel	Outer Barrel
max. silicon thickness (µm)	50	
spatial resolution (µm)	5	10
chip dimensions (mm^2)	15×30	
max. power density (mW)	300	100
max. integration time (µs)	30	
min. detection efficiency	99%	
max. fake hit rate ($evt^{-1}pixel^{-1}$)	10^{-5}	
TID radiation hardness (krad)	700	10
NIEL radiation hardness (1 MeV n_{eq}/cm^2)	10^{13}	3×10^{10}

- Very **thin sensors**
- Very **high granularity**
- **Large area** to cover
- **Modest radiation levels**

$\Rightarrow$ **Monolithic silicon pixel sensors**

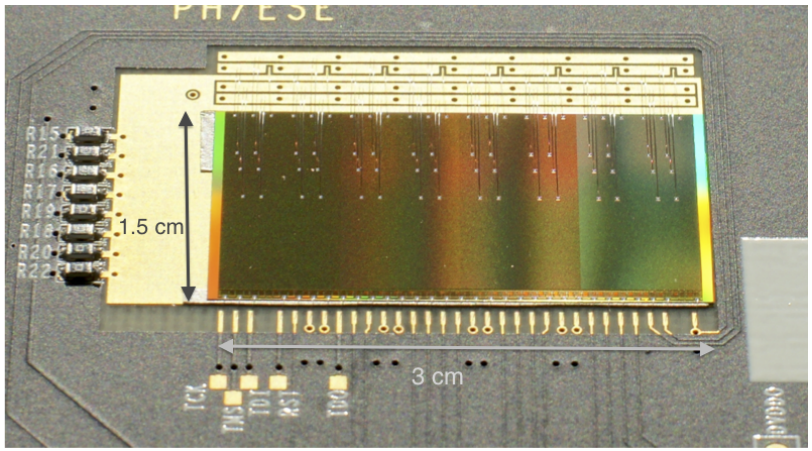
Pixel Chip Technology



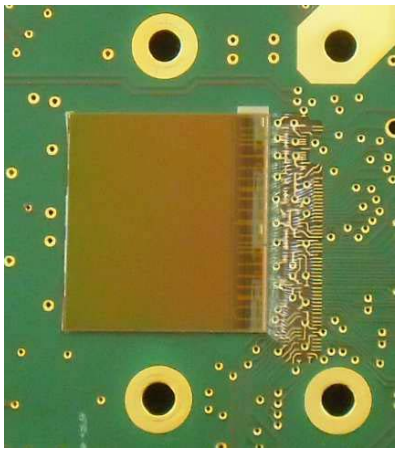
Monolithic active pixel sensors in TowerJazz 0.18 μm CMOS imaging process

- High-resistivity epitaxial layer on p-substrate
- Quadruple well process: deep pwell shields PMOS transistors, allowing for full CMOS circuitry within active area
- Application of (moderate) bias voltage to substrate can be used to increase depletion zone around NWELL collection diode

Pixel Chip Development



pALPIDEfs

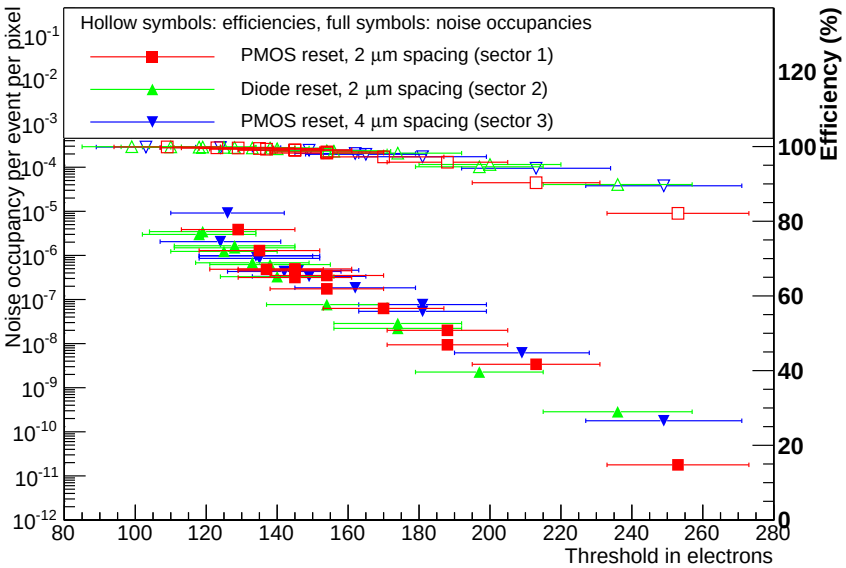

FSBB/MISTRAL

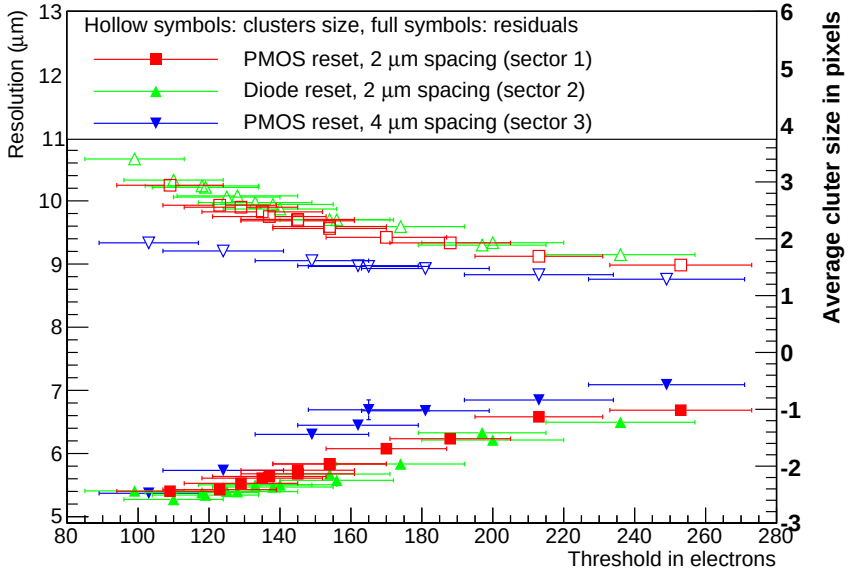
- Three main pixel chip architectures: ALPIDE and MISTRAL/ASTRAL, with the aim to select a common design beginning of 2015
- Several small scale prototypes have been developed to optimise sensor pixel and front-end
  - Test results show that performance and radiation hardness meet the requirements
- Received first full scale prototypes beginning of May; first lab tests and testbeam measurements show very promising results, including
  - Irradiated chips
  - Test of chips thinned to 50 μm

Performance Examples

ALPIDE Full-scale Prototype

- First ALPIDE full-scale prototype fully working
- Tests show this prototype already has satisfactory performance, pending the results of irradiated chips
  - ENC noise at 30°C between 5 and 10 e (using design value of inj. cap.), threshold RMS between 15 and 20 e
  - Efficiency close to 100% even without back bias
  - At the same time very low fake hit rates



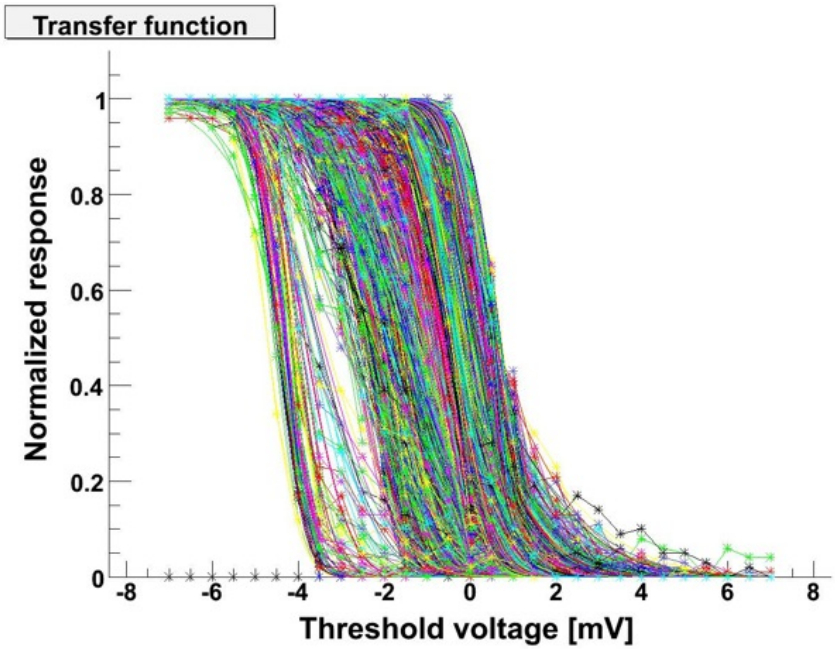


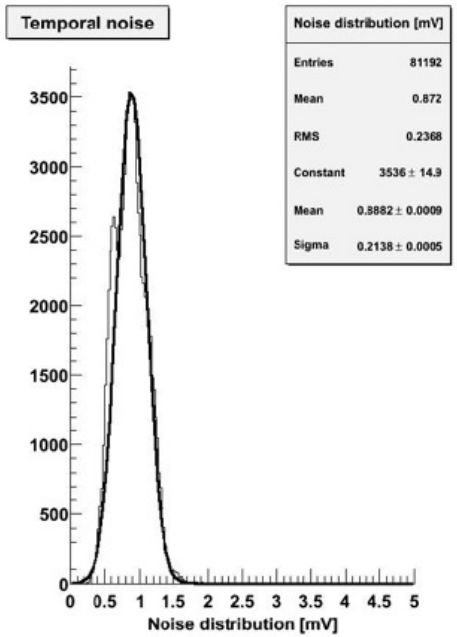
(for more details cf. Presentation of P. Yang)

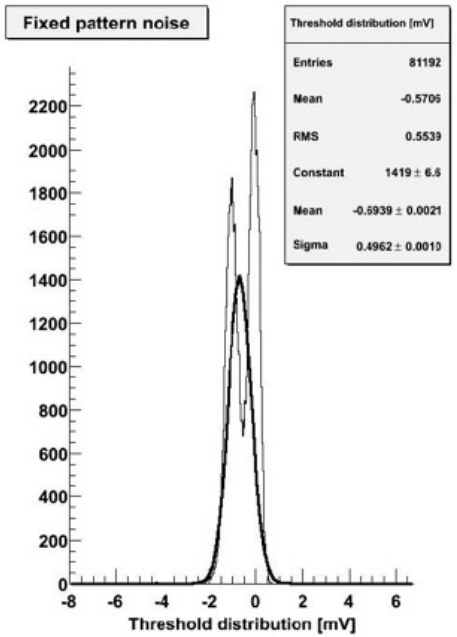
Performance Examples

ASTRAL/MISTRAL

- Full scale building block of MISTRAL received and fully working
- Lab characterisation has started and shows good results, ENC noise 15–20 e
- Test beam measurements to come...







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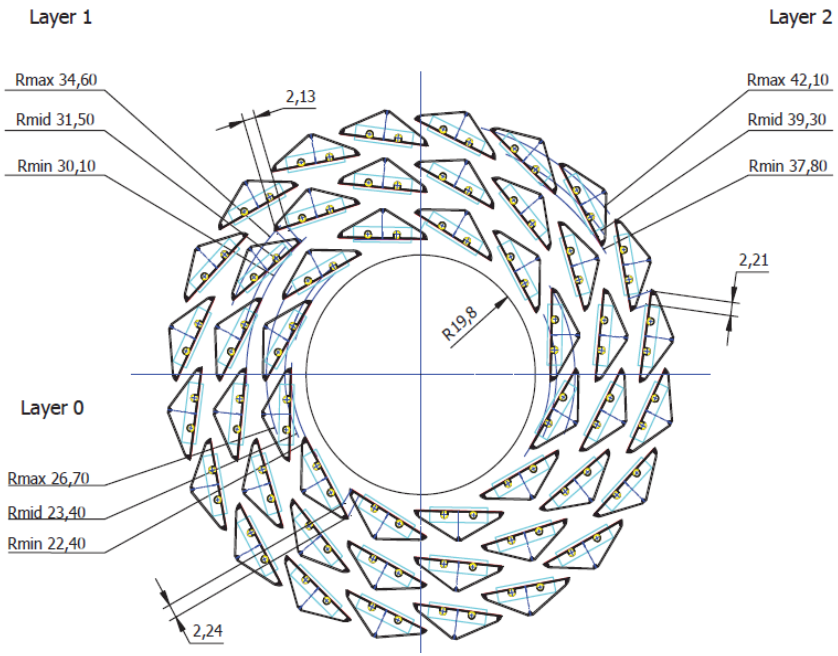
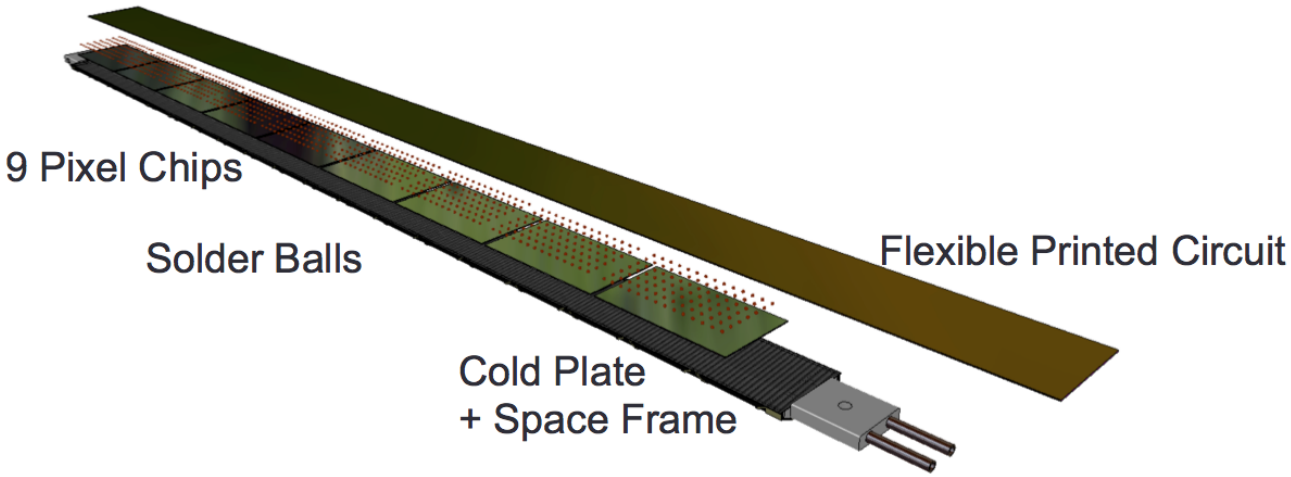
ALICE ITS Inner Barrel



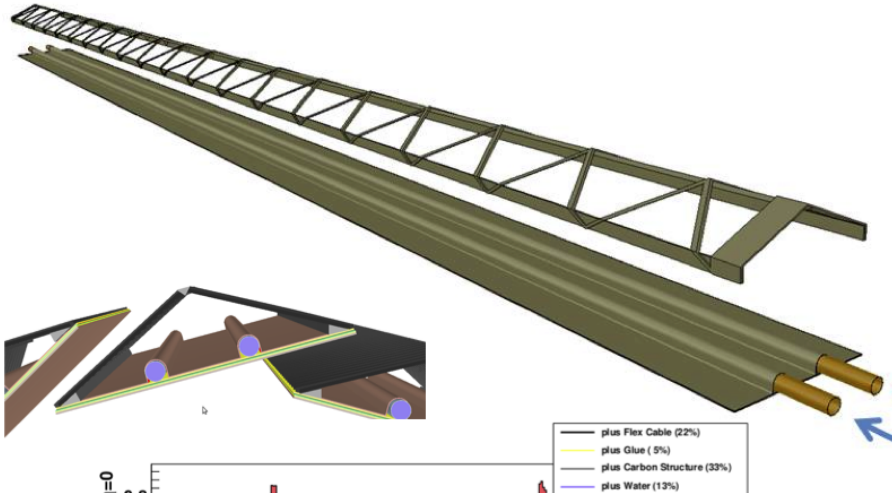
- Three layers, radii: 22, 31, 39 mm
- Length 270 mm
- Nr of staves: 12 + 16 + 20
- 9 chips per stave
- Material budget / layer: $\sim 0.3\% X_0$
- Av. data throughput up to 300 Mbit / s / chip

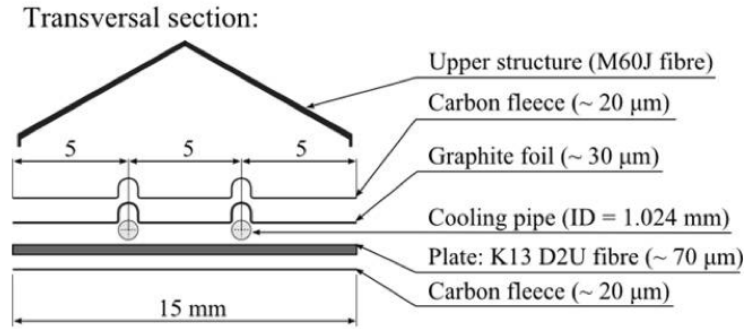


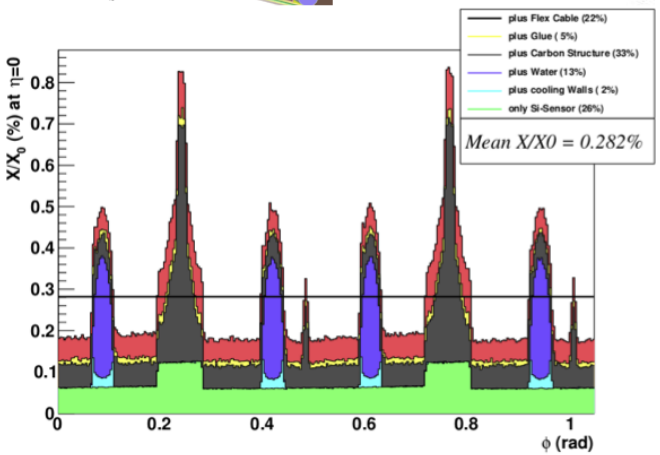
Inner Barrel Stave

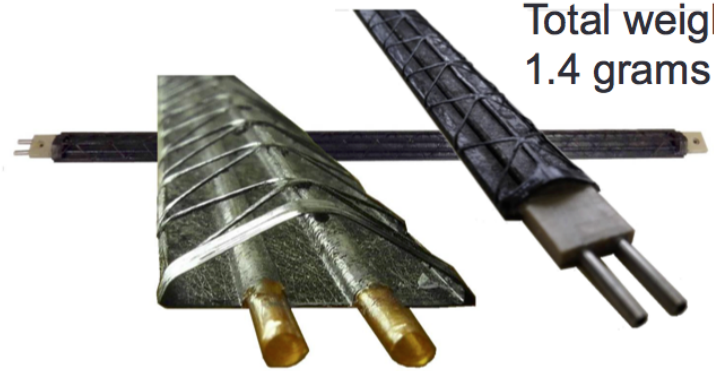
Design and Prototypes

- Lightweight carbon structure with polyimide cooling pipes (wall thickness 25 μm)
- Average material budget $< 0.3\%\,X_0$

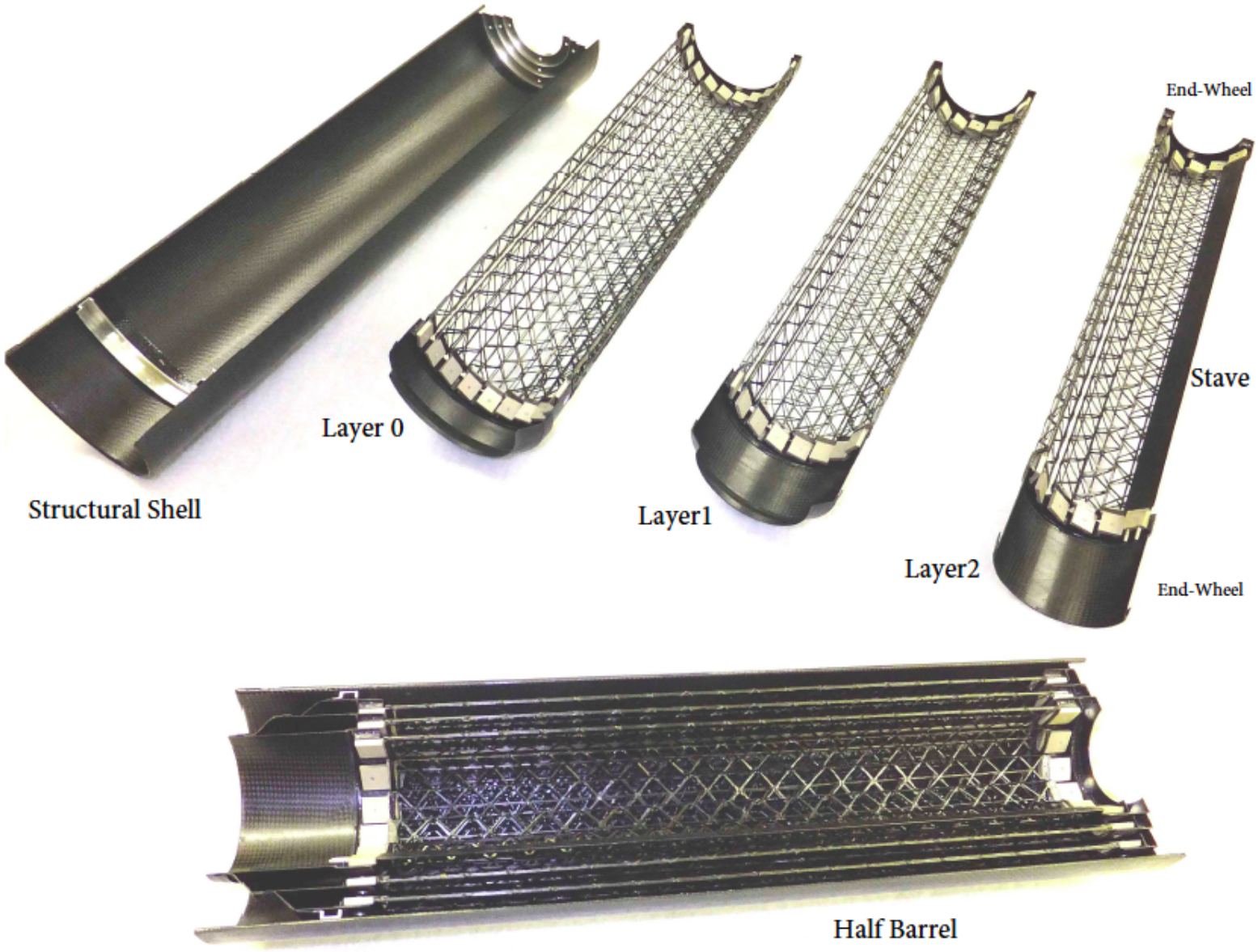






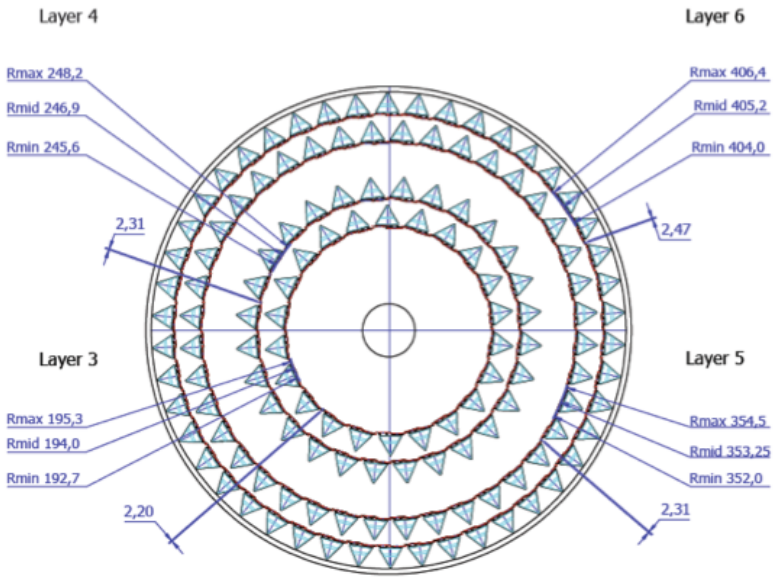


Inner Barrel Prototype



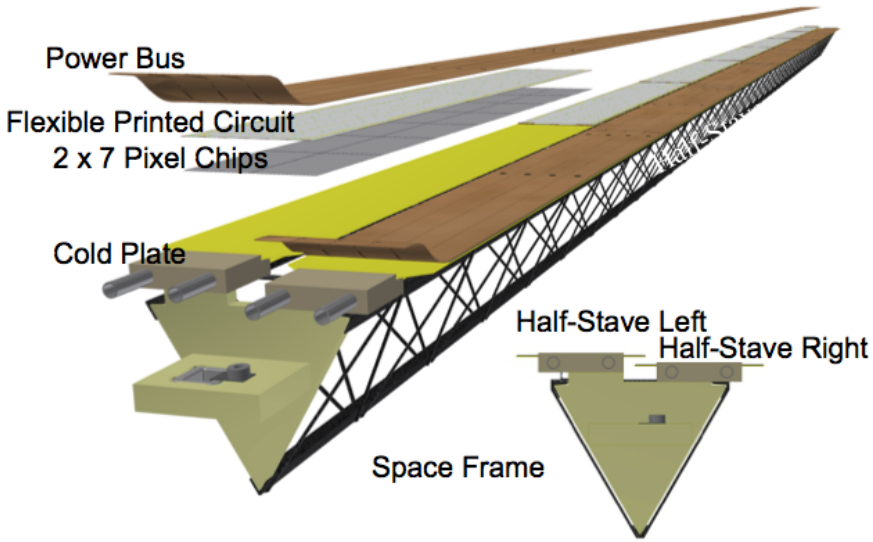
ALICE ITS Outer Barrel

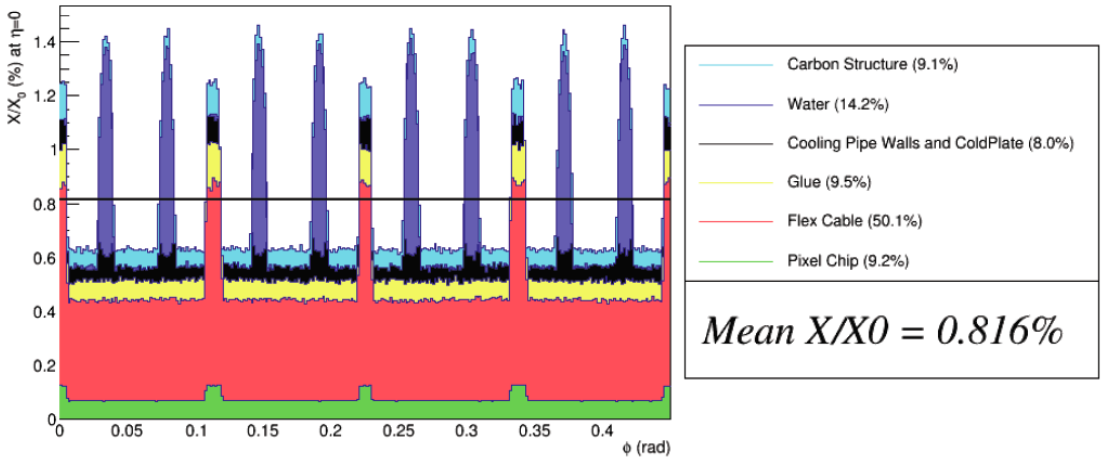
- 4 layers, radii: 194, 247, 353, 405 mm
- Length: 843 (ML), 1475 mm (OL)
- Nr of staves: 22, 28, 40, 46
- Nr of modules/stave: 4 (ML), 7 (OL)
- Nr of chips/module: 14
- Material budget / layer: $\sim 0.8\%\, X_0$
- Data throughput
  < 12 Mbit / sec / cm^2

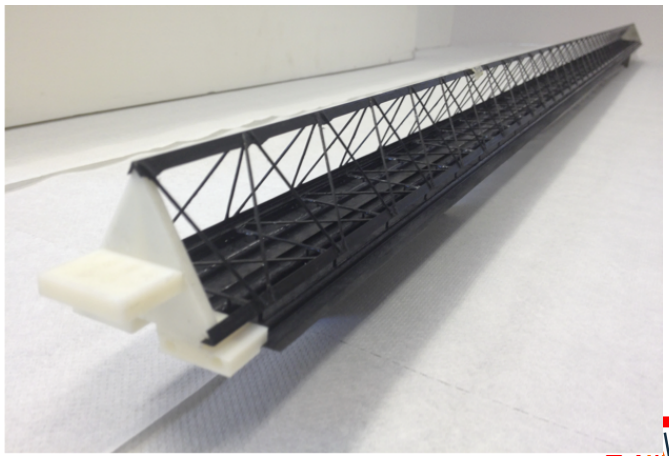


Outer Barrel Stave

- Outer barrel stave consists of two staggered half-staves
- Each half-stave further segmented into modules
- Average material budget per layer $\sim$ 0.8% X_0

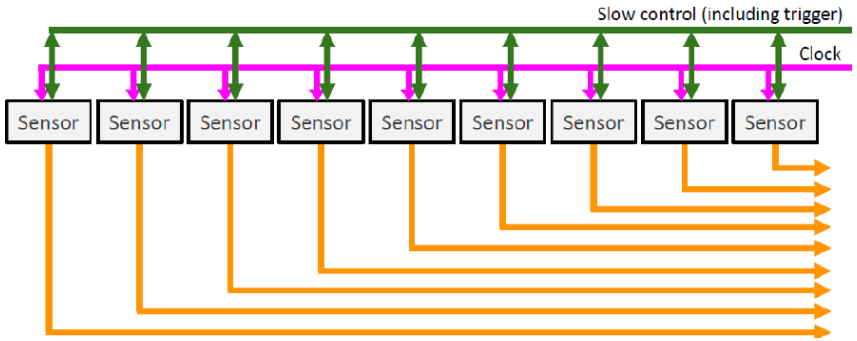




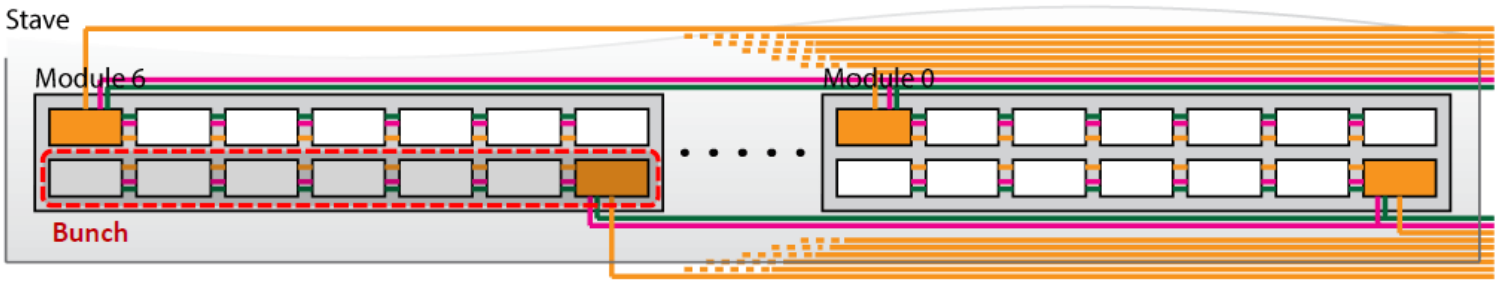


Stave Readout Topology

- From the innermost to the outermost layer
  - The expected hit densities decrease by a factor of 100.
  - The number of chips per (half-) stave increases from 9 to 98.
- Different readout topologies for inner and outer barrel
  - Inner Barrel: each chip drives point-to-point data line to off-detector electronics.



  - Outer Barrel: chips grouped into modules with two master chips; point-to-point link from masters to off-detector electronics.



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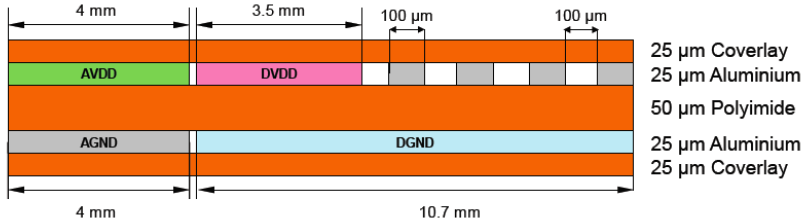
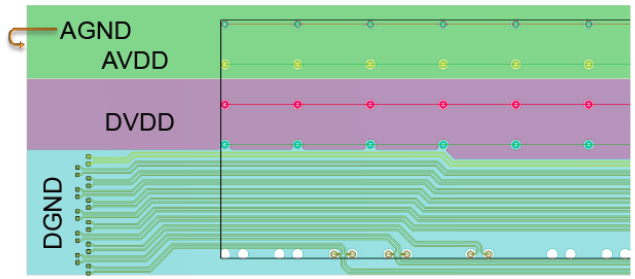
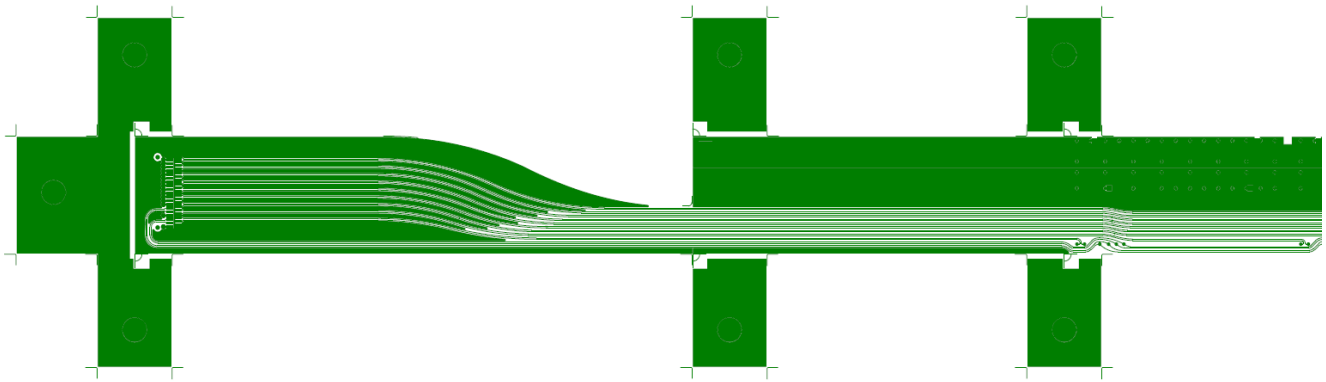
Flex Printed Circuit (FPC)

Here: Inner Barrel

- Flexible printed circuit of low-CTE polyimide and aluminium
- Power planes for digital and analogue voltage
- 11 differential pairs (clock, configuration, 9 data lines)

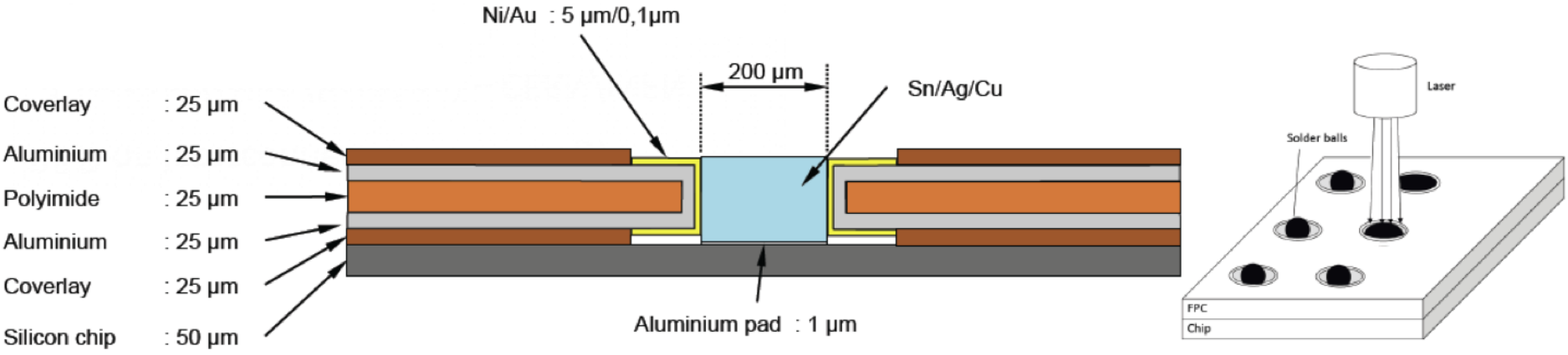


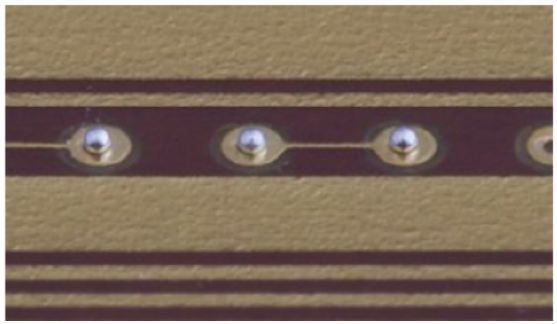


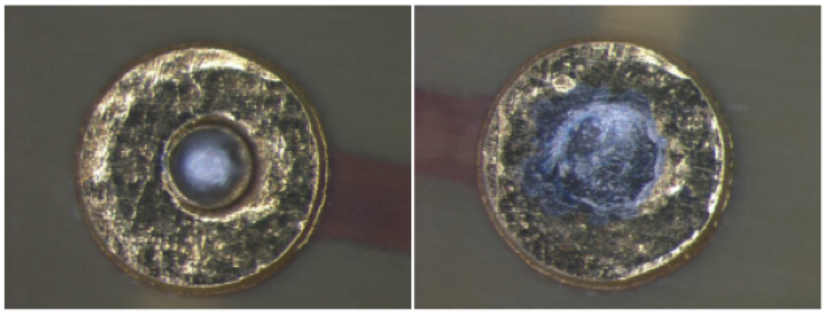


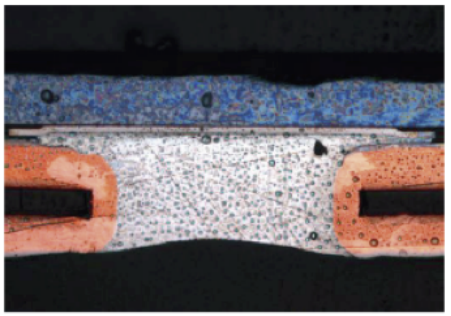
Outer Barrel: Decided to use Cu instead of Al ($\sim +0.1\% X_0$), physics impact low enough

Chip-to-FPC Connection









Chip and FPC will be connected by laser soldering

- Connection to dedicated pads distributed over the full chip area
- Successfully prototyped and now realiably working on daisy-chain chips
- Tests with real chips starting this week

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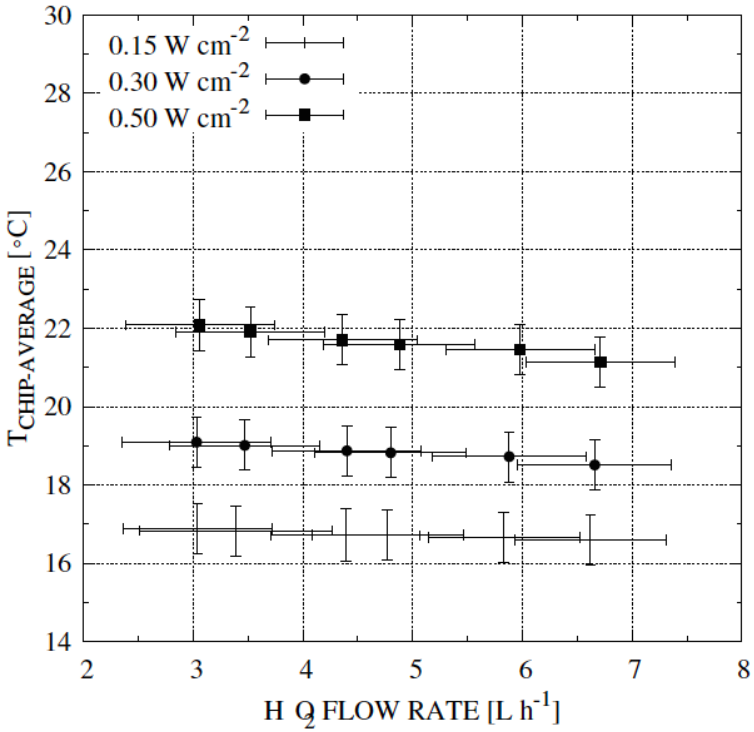
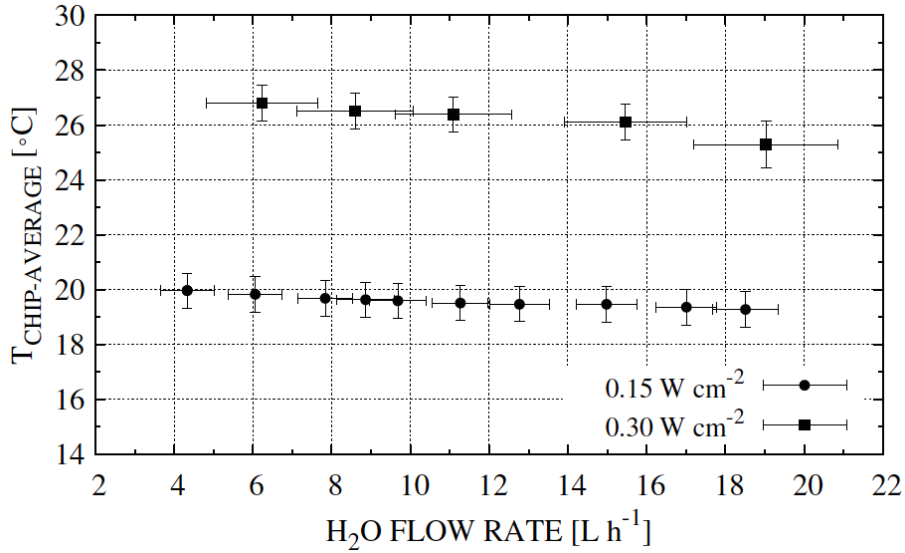
Cooling

- Goal: Chip temperature below 30°C
- Baseline: leakless (< 1 bar) water cooling
- Thermal characterisation of stave prototypes with heaters for different flow rates:
  - Chip (heater) temperature well below 30°C
  - Pressure drop < 0.3 bar





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Summary and Outlook

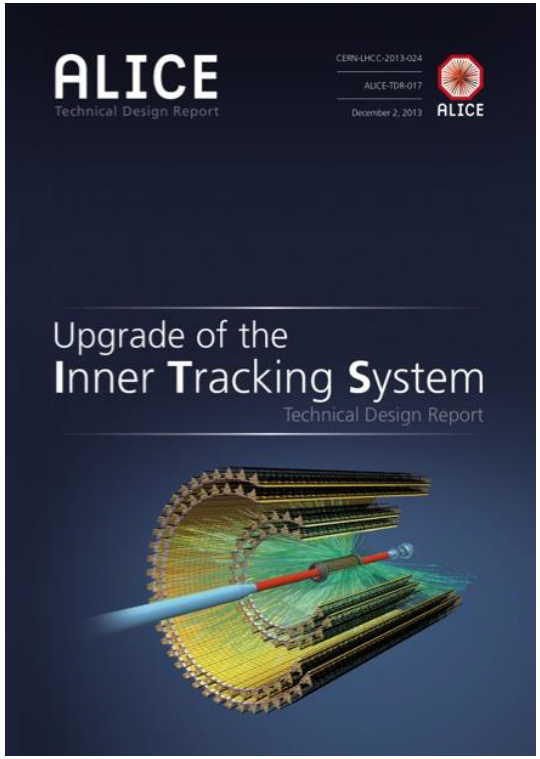
- ALICE will replace its entire Inner Tracking System by a pixel-only tracker during LS2 in order to
  - Significantly improve the impact parameter resolution at low p_T
  - Increase the readout rate up to 50 kHz for Pb-Pb collisions
- All R&D items of the project are close to finalised

The important steps in the coming year are characterised by the engineering of final prototypes and the preparation for the start of the construction in 2016:

- Converge from the working sensor prototypes to a final sensor design
- Build first inner barrel staves / outer barrel modules with real chips
- Finalise mass production and test procedures
- ...

Upgrade of the ALICE Inner Tracking System

Technical Design Report



TDR approved by the Research Board on March 12, 2014