Operational experience with the ALICE Pixel Detector

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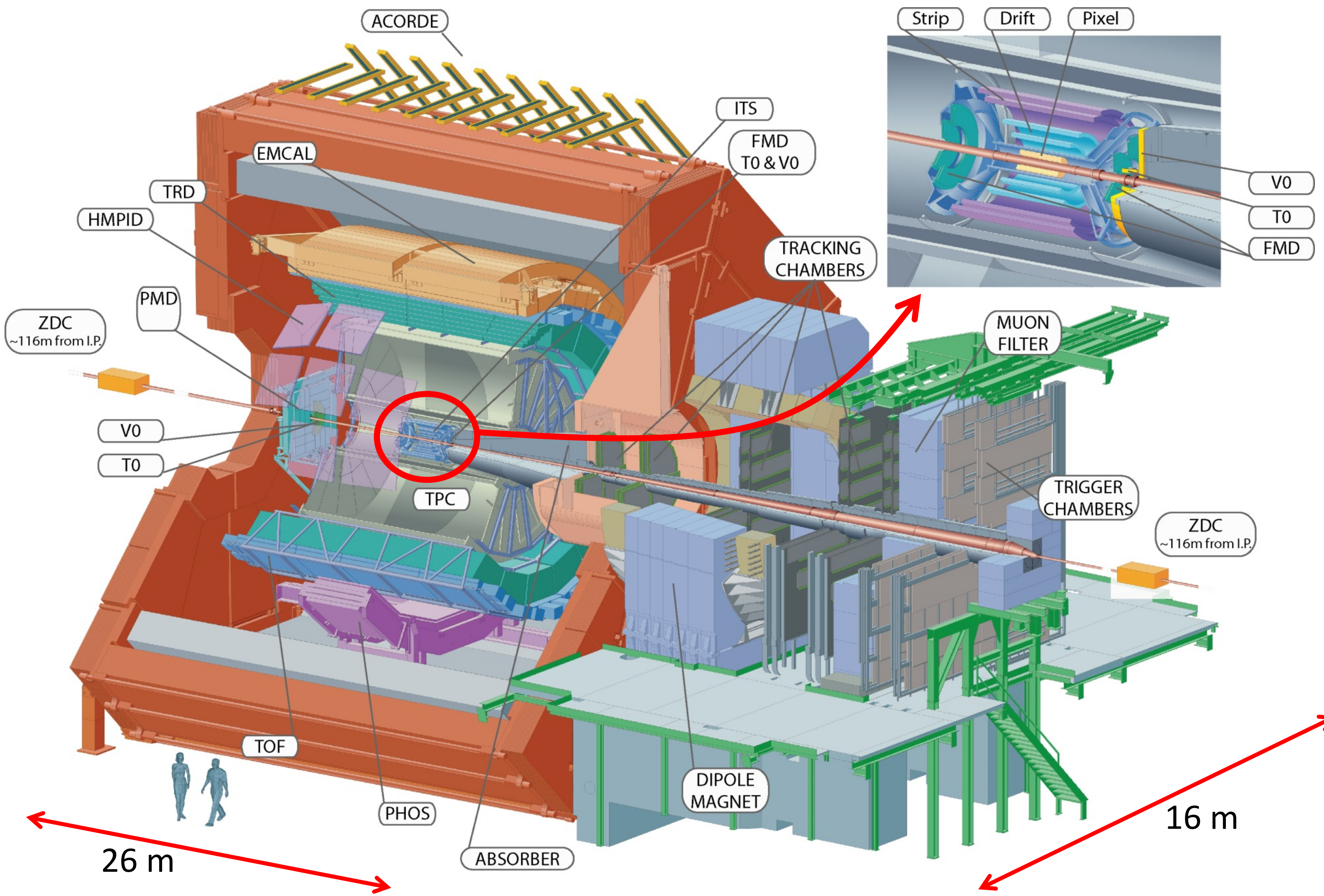
Outline

- ALICE Silicon Pixel Detector
- Operational experience
- Cooling conditions and optimization
- Detector calibration and optimization
  - Efficiency
  - Threshold
  - Trigger
- Long shutdown activities

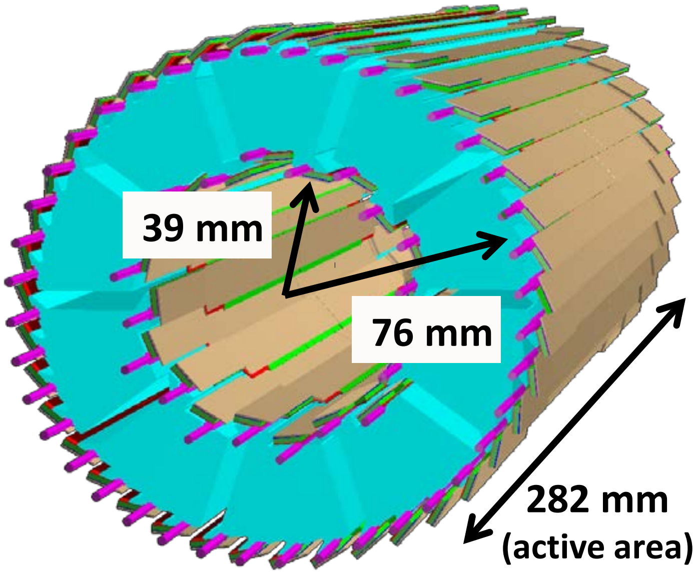
ALICE Inner Tracking System



ALICE pixel detector

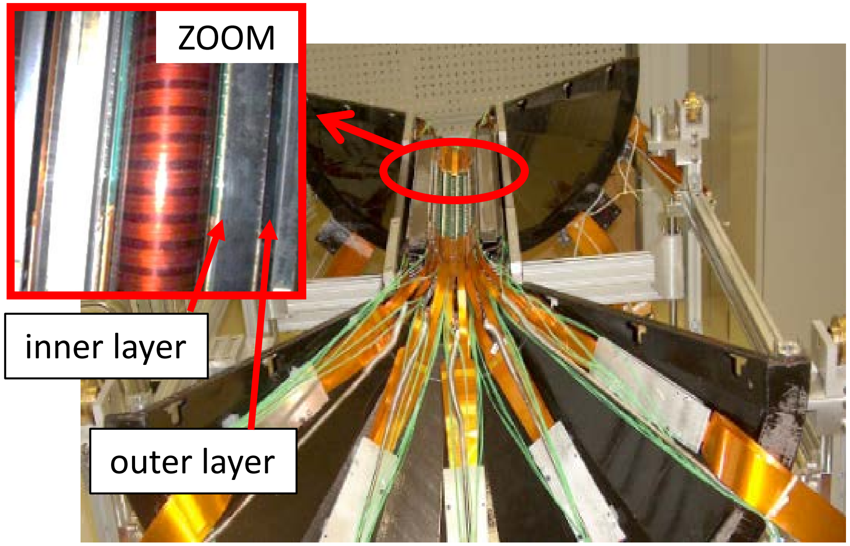
GOALS

- location of primary and secondary vertices
- tracking decays of short-lived particles
- contribution to first level trigger



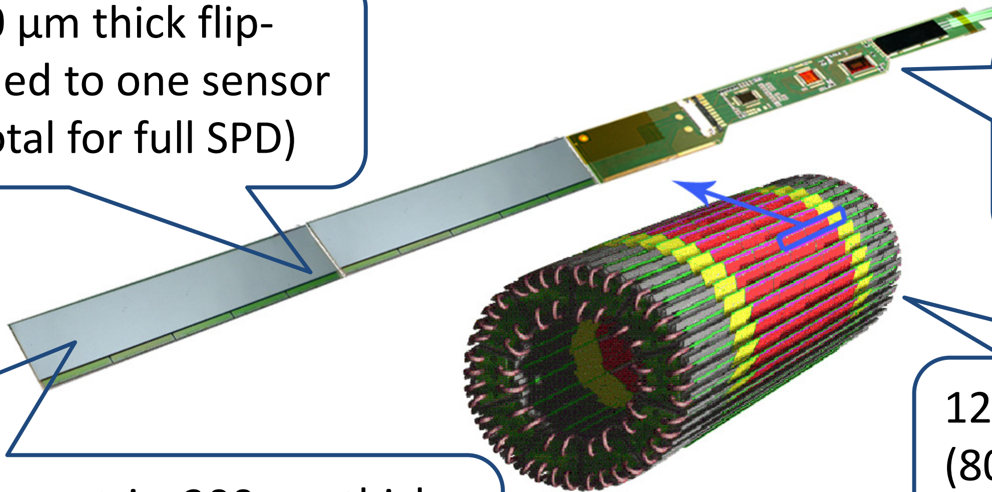
CHARACTERISTICS

- coverage: |η|< 2 for inner layer and |η|< 1.4 for outer layer
- matrix readout: 256 µs
- spatial precision: 12 µm in rϕ and 100 µm in z
- pixel size: 425 µm x 50 µm (z x rϕ)
- material budget: ~1.1% X_0 per layer
- power consumption: 1.35 kW



ALICE pixel detector

5 pixel chips 300 µm thick flip-chip bump bonded to one sensor (1200 chips in total for full SPD)

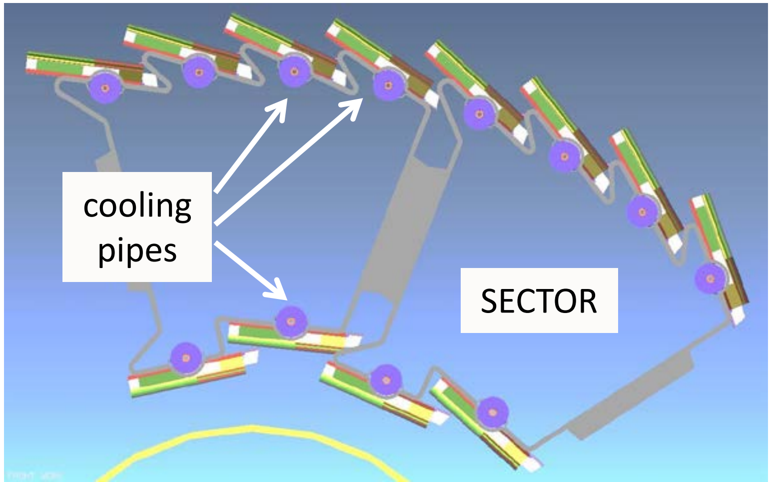


Multi Chip Module to configure and read the half-stave

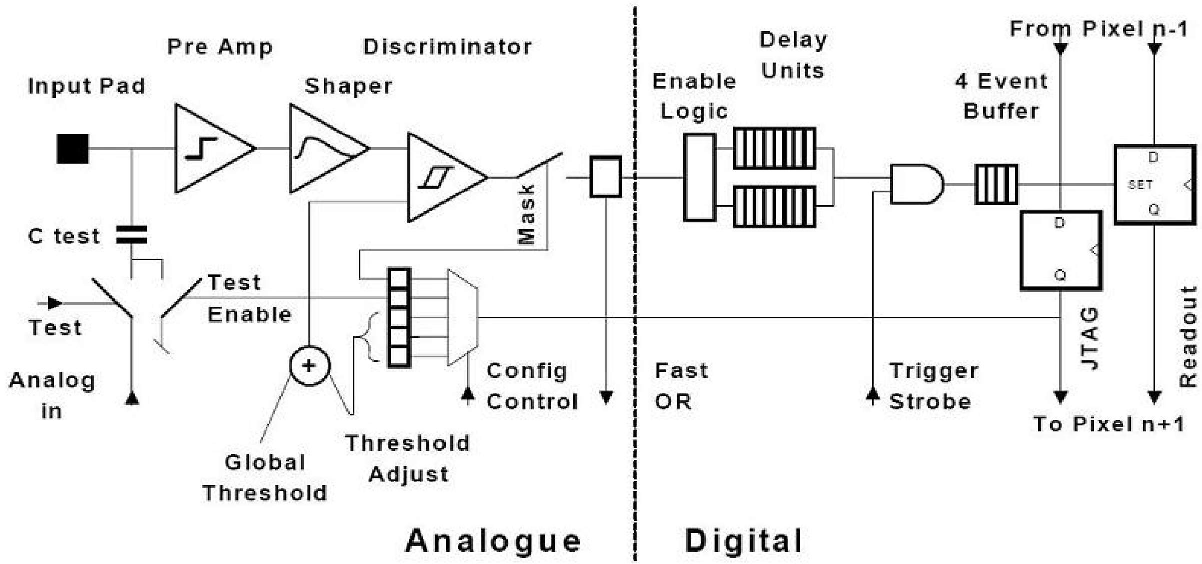
p⁺n silicon sensor matrix, 200 µm thick, reverse biased at 50 V (~9.8×10^6 pixels in total for full SPD)

120 half-staves in total (80 outer, 40 inner layer) divided into 10 sectors

- evaporative cooling system with C_4F_{10}
- cooling pipes under each half-stave, embedded in the carbon fiber support
- monitoring of T-p at the plant and up/downstream the detector

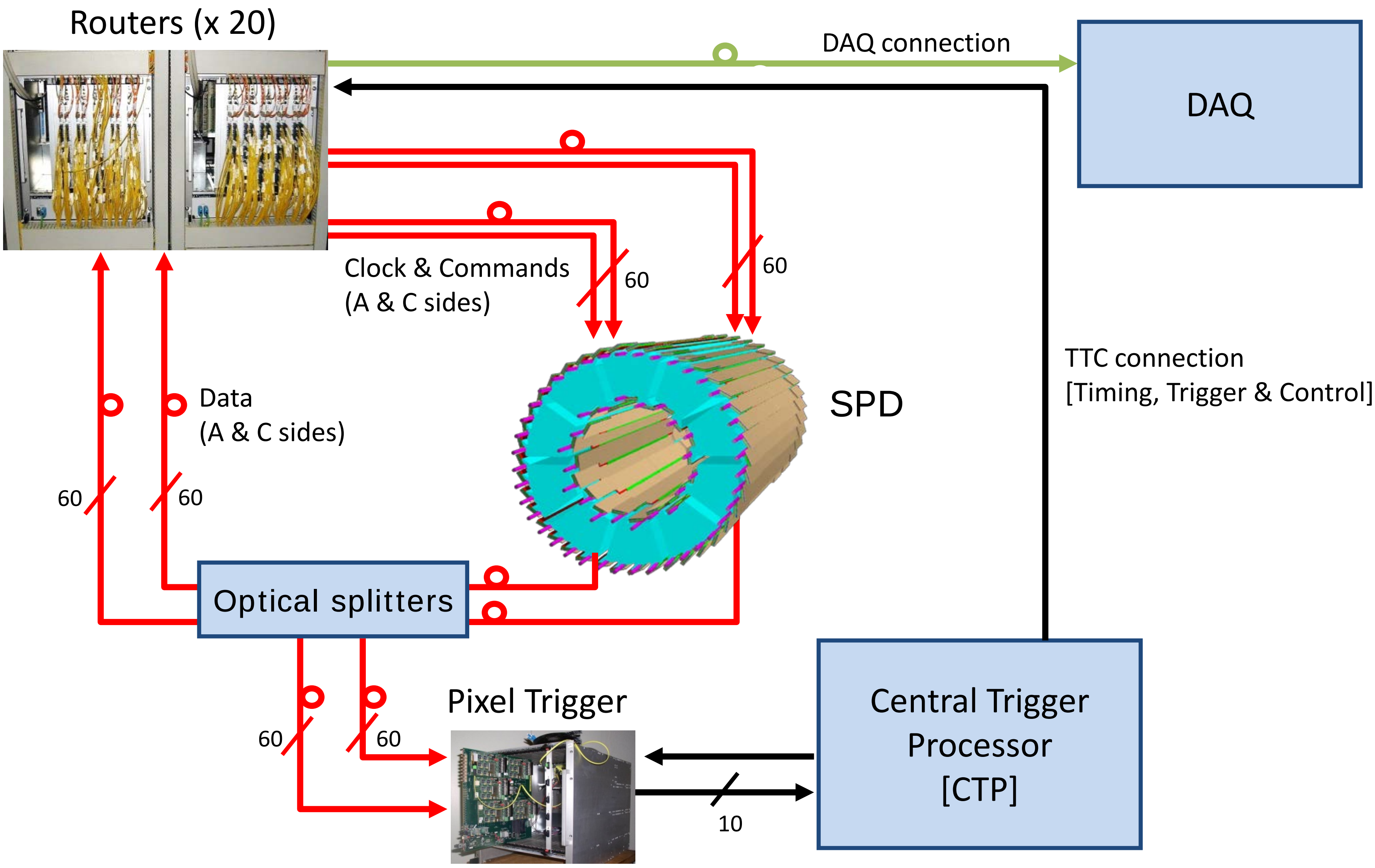


ALICE pixel chip

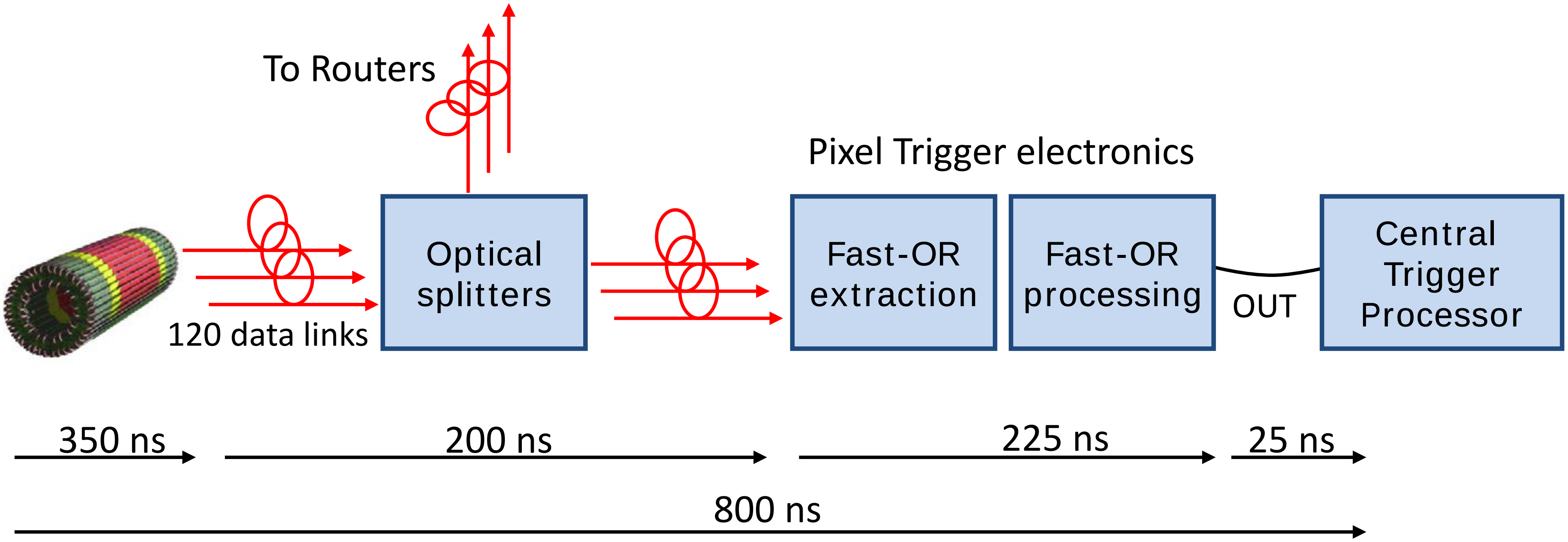


- Standard chain of preamplifier - shaper - discriminator
- Possibility of analogue pulse injection and mask at pixel level
- Fast-OR (trigger) output after discriminator
- L1: data in 4 stages FIFO, L2: data in shift registers for readout
- In total 42 DACs + 8 ADCs for biases / working parameters
- Full SPD read out in 256 µs

Detector integration



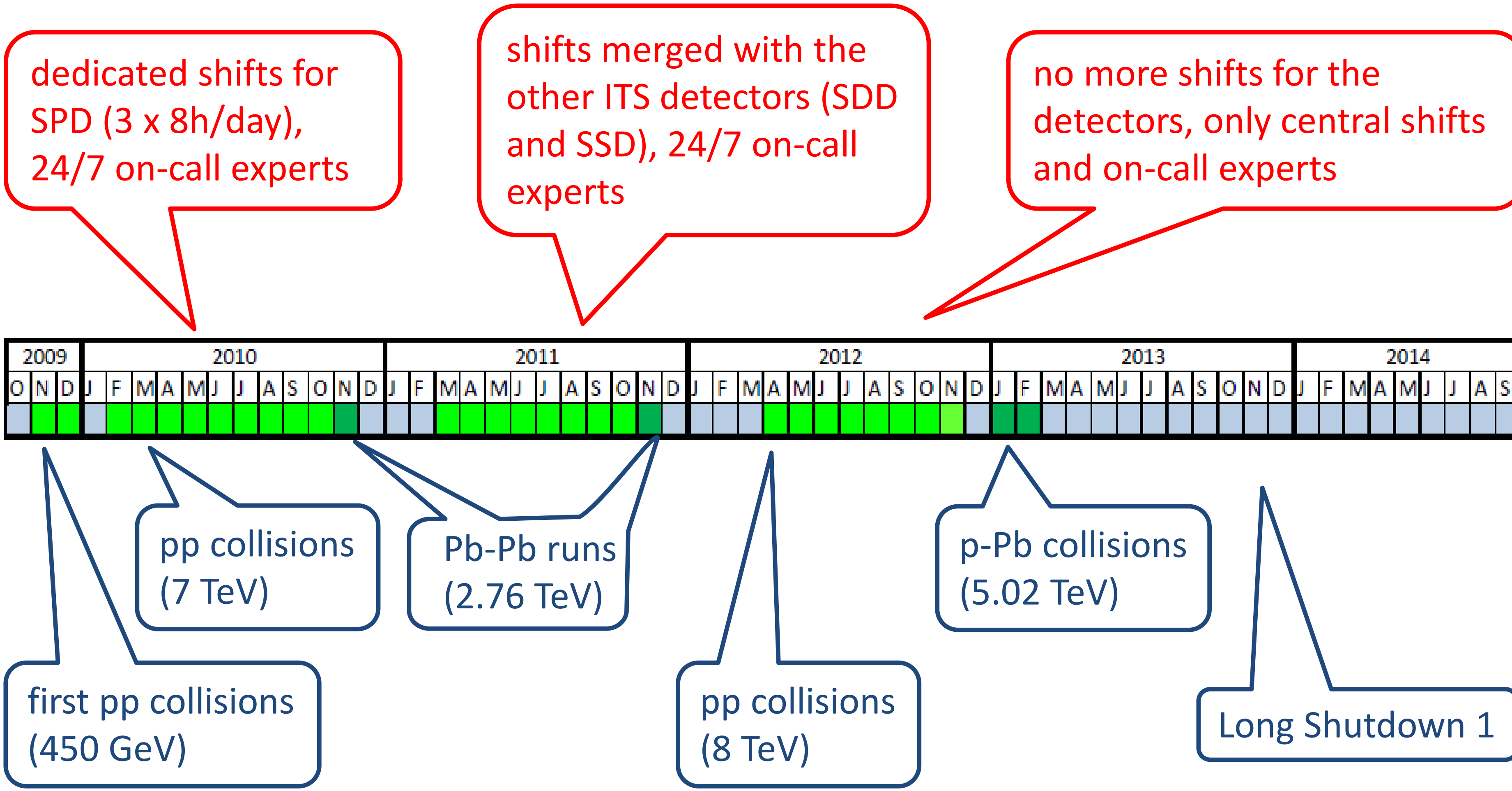
Pixel trigger integration



- Fast-OR active on registration of at least 1 hit per readout chip
- Contribution to the first level of trigger in ALICE
- IN: 1200 bits every 100 ns from the SPD to the Pixel Trigger
- OUT: 10 programmable outputs based on Boolean logic propagated to CTP
- Maximum latency at CTP input = 800 ns → installed at 40 m from SPD

Detector operation

DETECTOR OPERATIONS



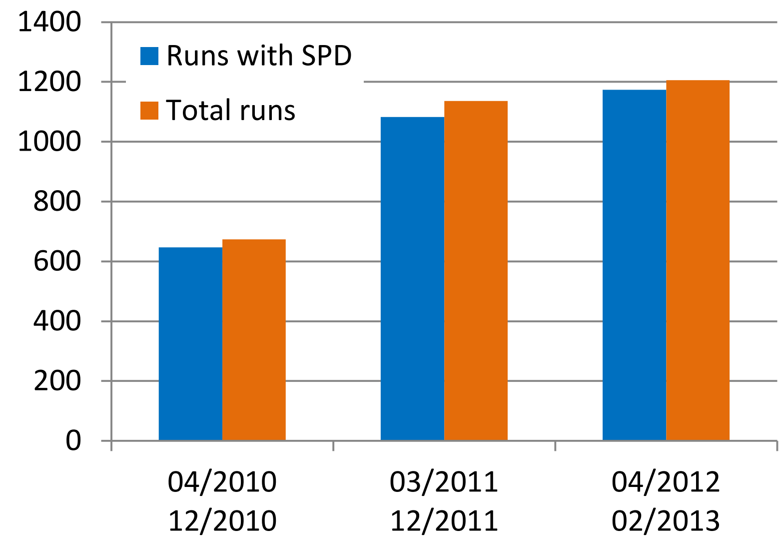
LHC CONDITIONS

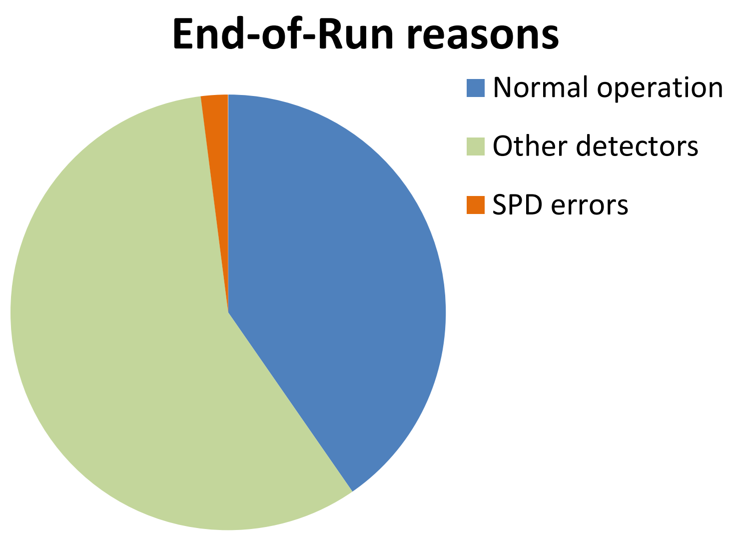
Operational procedures

- Until “stable beams” reverse bias on the sensor (50 V) is off -> safe state
  - voltage ramped up when stable beams declared
- Configurations checked at the start of each run
  - front-end configuration and parameters of trigger algorithms are linked to trigger conditions in a central Alice Configuration Tool
  - mask of noisy pixels (order of 0.1‰) and chips included/excluded from trigger are also associated to the configuration
- No difference in the operation of the detector in pp and Pb-Pb runs

Run statistics

- Statistics based on physics runs
- Excluded calibration / commissioning runs
- SPD included in readout in more than 96% of runs
- End-of-Run reasons automatized and recorded in logbook and database since Sep 2011
- SPD contributed to ~2% of EOR (~3.4% of errors coming from Alice detectors)



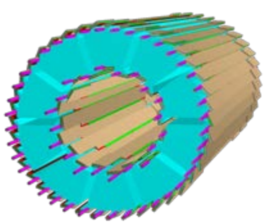


Error handler

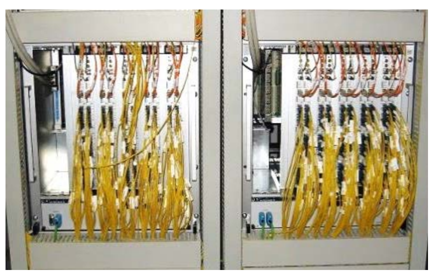
The driver layer reads the errors from the Routers and stores them in a database, in parallel with data acquisition (no disturbances).
Errors are flagged with priorities, PE avoids cascade of secondary errors.

The errors can be fetched from DB and used for debugging / statistics.

database



DETECTOR



ROUTERS

C++ DRIVER

USER INTERFACE

Errors from trigger + Routers + LinkRx + optical connections + half-staves are formatted and stored in the Router memory.

The errors are notified to the shifters through standard alarms.

Operational half-staves

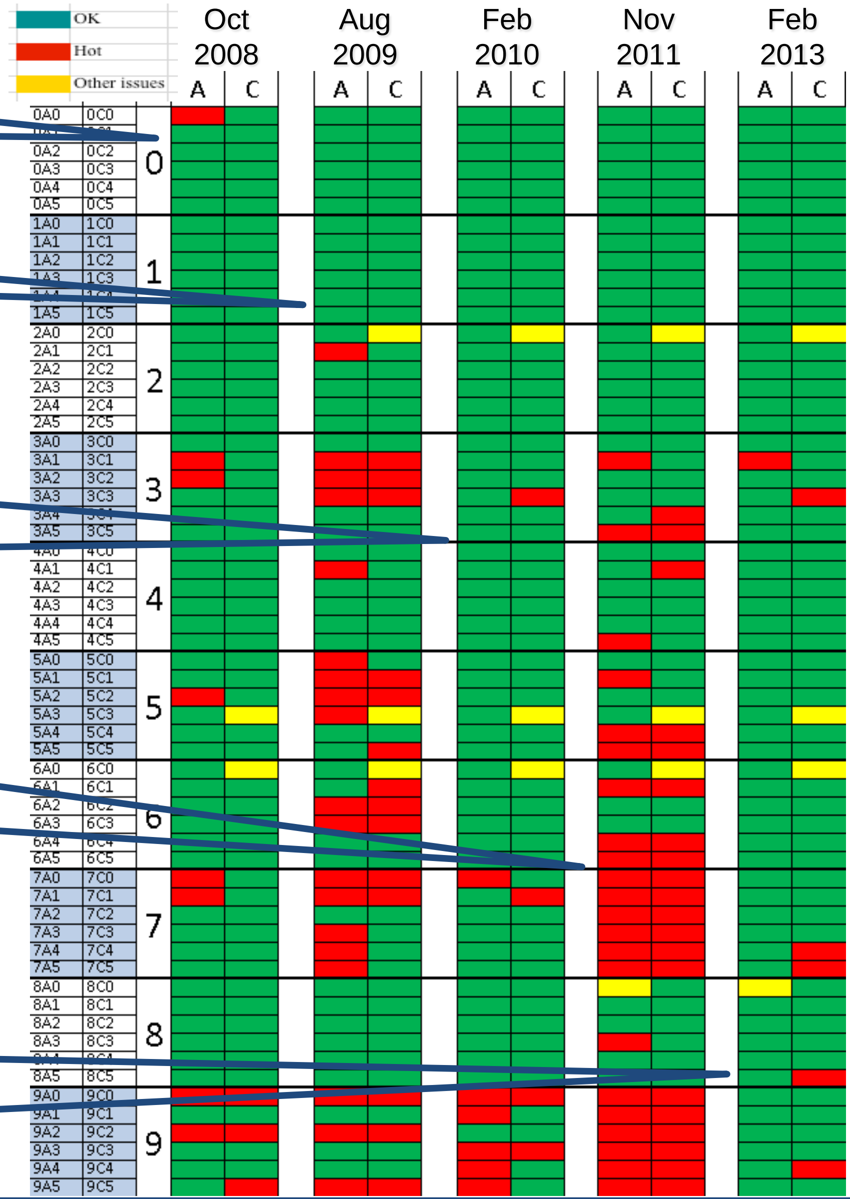
2008: situation during first beams

2009: 30% off after the long shutdown

2010, after few months :
counter-flow wise cleaning, new input lines, liquid pressure control per line

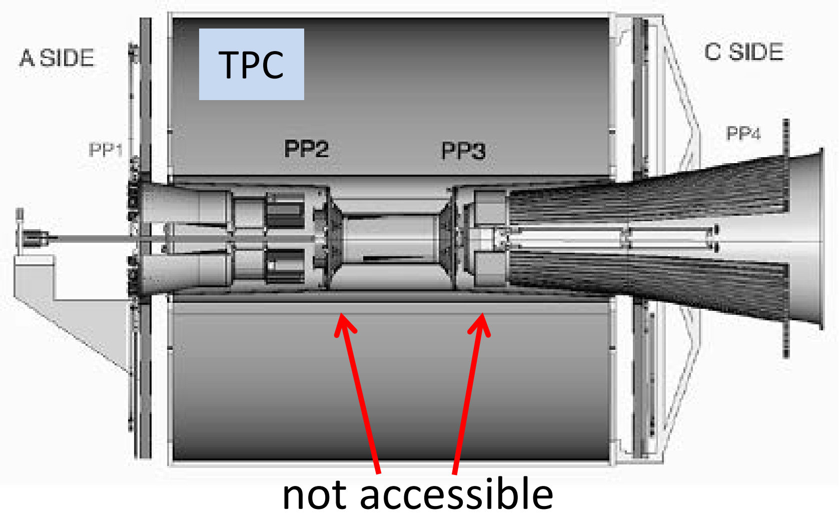
2011: situation slowly worsens after every tech. stop, in Nov 2011 only 63% of the SPD is on

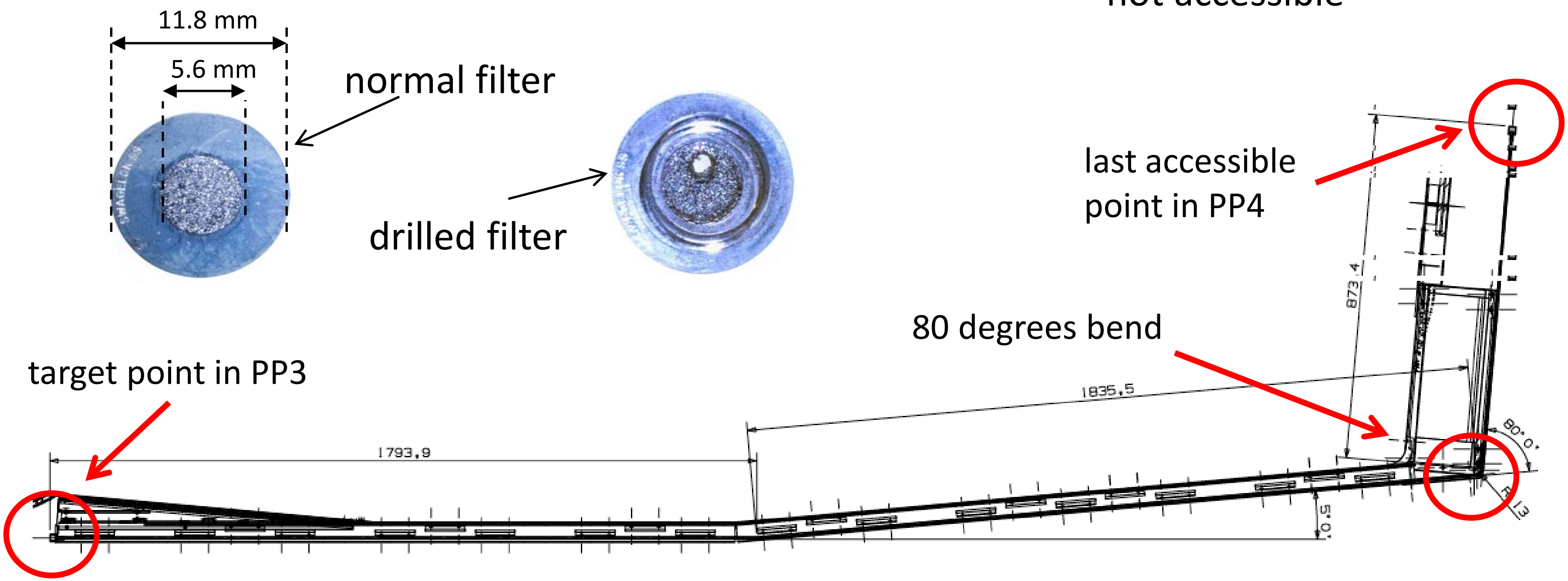
2012-2013: the cure! Challenging filter drilling operation, new filters installed at plant level, stable until end of Run1



Drilling operation 1/2

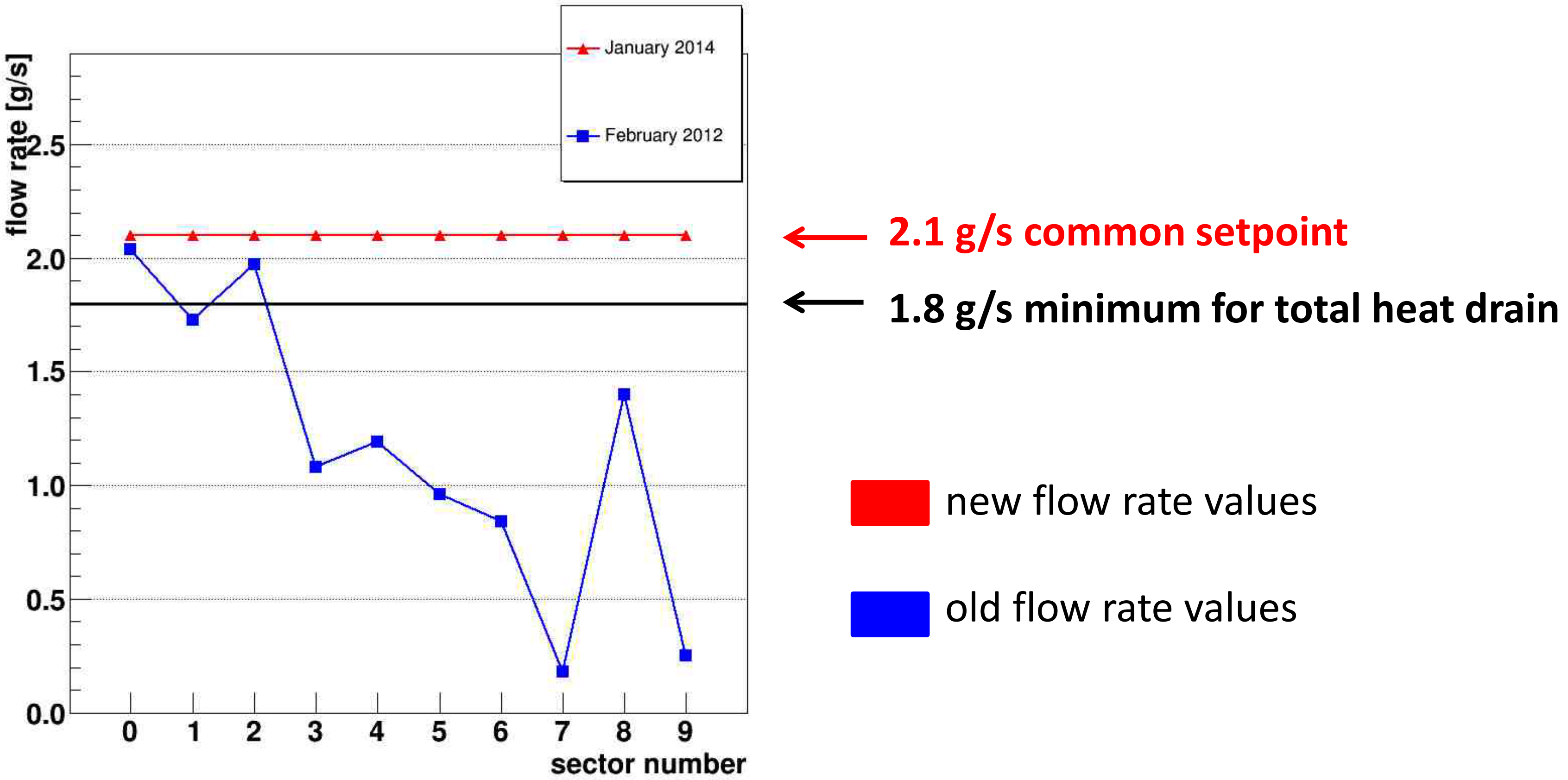
- 4.5 m from last accessible point to clogged filters
- Inner diameter of cooling pipe 4 mm !
- Drilling done with tungsten carbide tip welded on twisted stainless steel cable
- Cleaning with vacuum pump + magnet in the pipe + counter-flow cleaning fluid





Drilling operation 2/2

- More than 100 filters frilled in the lab to optimize the procedure
- Drilling and cleaning done on each filter of the 10 sectors of SPD
- Comparison with February 2012, before the drilling started
- New values of freon flow set at 2.1, i.e. nominal value + contingency



Efficiency calibration

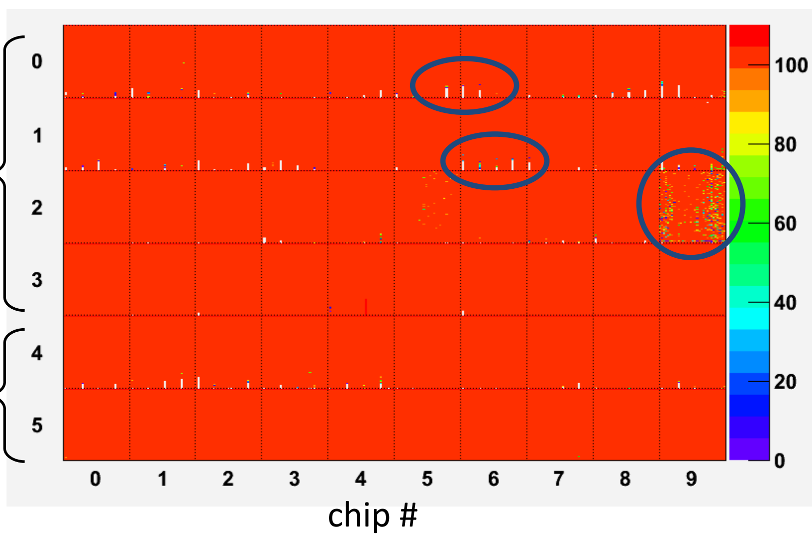
- Internal pulser of known amplitude to detect inefficient regions
- Injection tests and cosmic data accumulated for cross checking
- Efficiency optimized acting in parallel on
  - global voltage reference biases
  - global threshold of the discriminator at chip level
  - bias of the first preamplifier stage

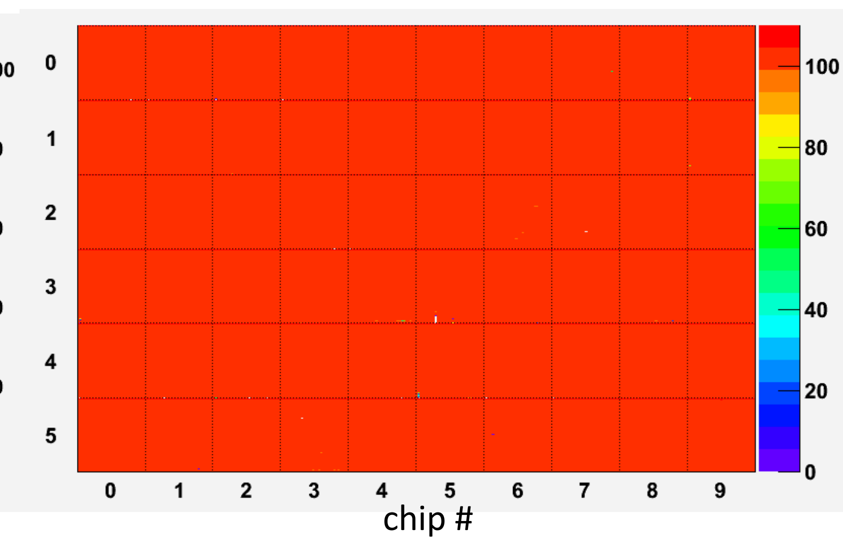
At every technical stop

Half sector: before tuning after tuning

outer layer

inner layer



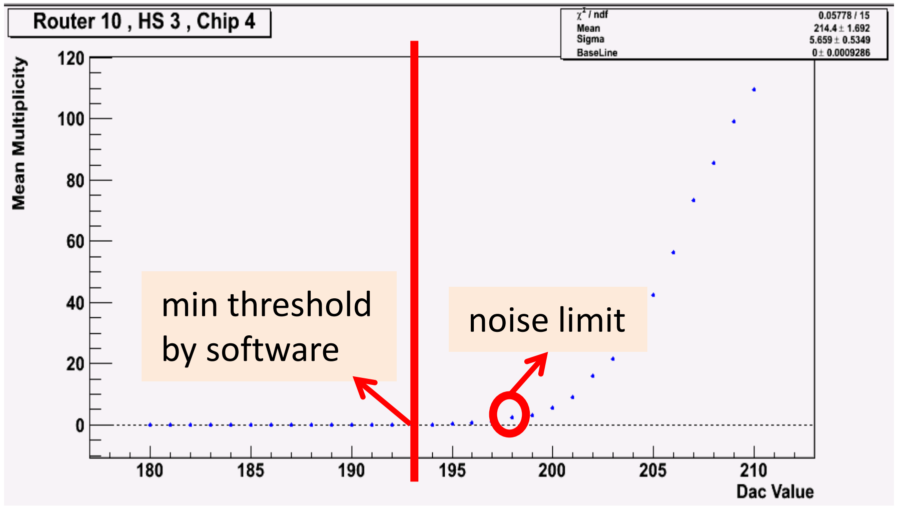


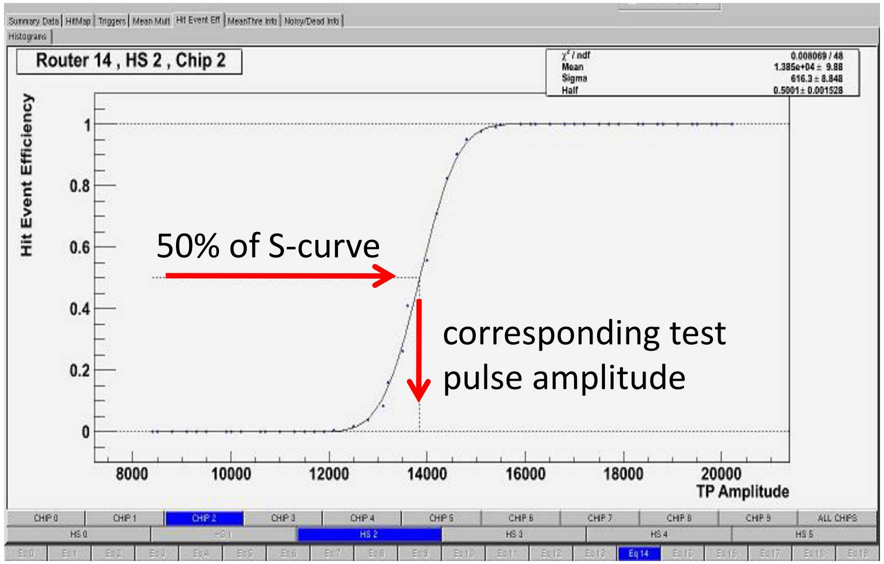
Threshold adjustment

<u>Minimum threshold scan</u>
finds the lowest threshold value at which the chip can be operated without noise

<u>Mean threshold scan</u>
finds the conversion factor between charge deposited on the detector and corresponding DAC value, with different amplitudes of internal pulser

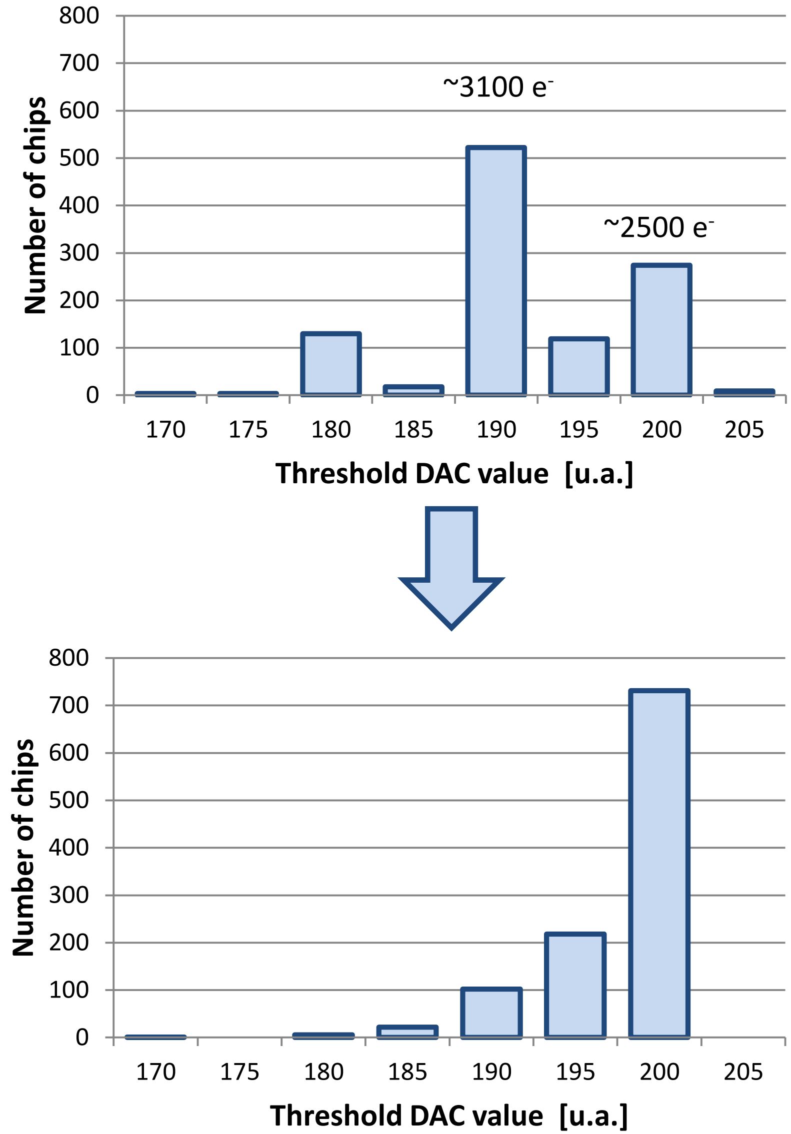
Calibration at every technical stop + regular minor adjustments





Threshold optimization

- Big campaign for threshold adjustment in 2010
- Default setting before was around 3100 electrons, now 2500 electrons
- Increasing number of noisy pixels masked, bus still negligible fraction
  - Noisy pixels 2010 : 0.006%
  - Noisy pixels 2012 : 0.01%
- Average noise for pixels ~300 electrons



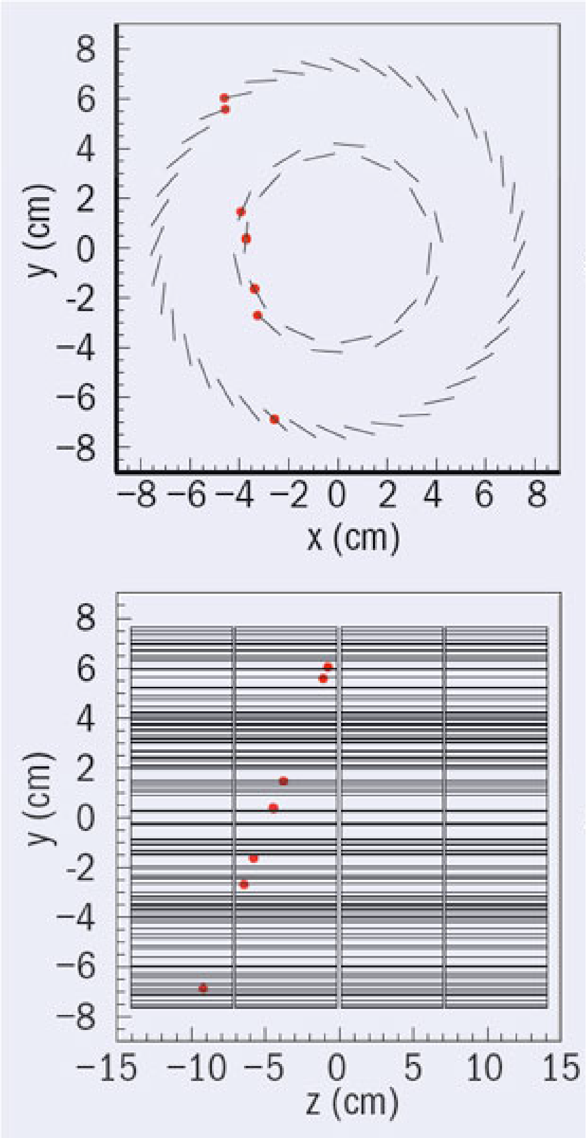
Trigger selection

- 10 programmable algorithms, with adjustable thresholds
- Input from trigger group on threshold values

Output	Name	Algorithm
1	Minimum Bias	$(I+O) \geq th_0$ and $I \geq th_1$ and $O \geq th_2$
2	High Multiplicity 1	$I \geq th_1$ and $O \geq th_2$
3	High Multiplicity 2	$I \geq th_1$ and $O \geq th_2$
4	High Multiplicity 3	$I \geq th_1$ and $O \geq th_2$
5	High Multiplicity 4	$I \geq th_1$ and $O \geq th_2$
6	Past Future Protection	$(I+O) \geq th_0$ and $I \geq th_1$ and $O \geq th_2$
7	Background 0	$I \geq O + offset_{Inner}$
8	Background 1	$O \geq I + offset_{Outer}$
9	Background 2	$(I+O) \geq th_{(Inner+Outer)}$
10	Cosmics	Selectable coincidence

Trigger calibration

- Performed manually for the cosmic data taking in 2008-2009
  - studied dependence of trigger output on trigger DACs in pixel chip
- Automatic calibration procedure in place since 2009
  - trigger configuration checked at every technical stop
  - fast-OR tuned with 4 dedicated DACs
- Rate of cosmic rays periodically checked
  - coincidence between top and bottom outer layer
  - very high purity: 99.5% of good events



Long shutdown activities

- Cooling improvements
  - final drilling activities on filters
- Revision of the firmware of readout electronics
  - high readout time during p-Pb run
  - problem in the firmware of the electronic boards identified
- New VME controller for crates with readout electronics
  - replaced National Instruments controller with CAEN controller
  - modified the software for communication with crates
- Migration of control software
  - upgraded all machines at P2 to new operating systems
  - old software for User Interface (based on PVSS) migrated to new platform (WinCC)

Conclusions

- Stable working point of Silicon Pixel Detector found through calibrations
  - periodical checks of efficiency uniformity and thresholds, both for readout and trigger chains
- Smooth operation of the detector during Run1
  - cooling issues successfully solved
  - error monitoring functionalities added and improved
  - issue related to the management of trigger buffers identified and solved
- Preparing for Run2

More details on End-of-Run

- Some errors with less severity
- Errors on readout electronics useful for debugging purposes

Error reason	# runs	
Detector requiring calibration	3	1 for missing communication with Pixel Trigger, others for faulty module that was switched off
Detector busy	13	of which 8 with data format errors on different modules
Cdh error	5	errors in electronics or in data format
Detector not ready	6	of which 1 for problem in CAEN mainframe (power supply) that was rebooted
Config error	1	configuration lost in 1 half-sector
Hardware error	2	of which 1 for testing purposes
High busy time	3	first p-Pb runs with issue of high readout time, solved with new firmware version