2.5/3D Integrated Circuit Technology

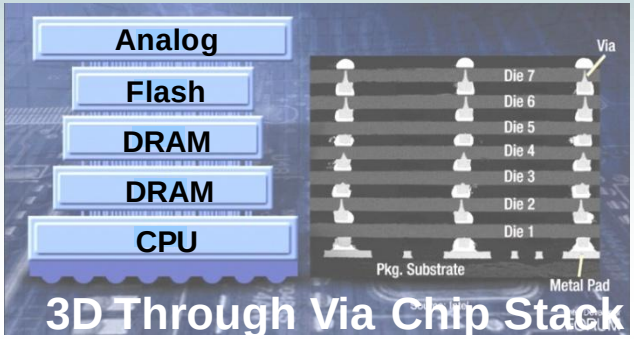
Capabilities and Industry Readiness

Robert Patti, CTO

rpatti@tezzaron.com

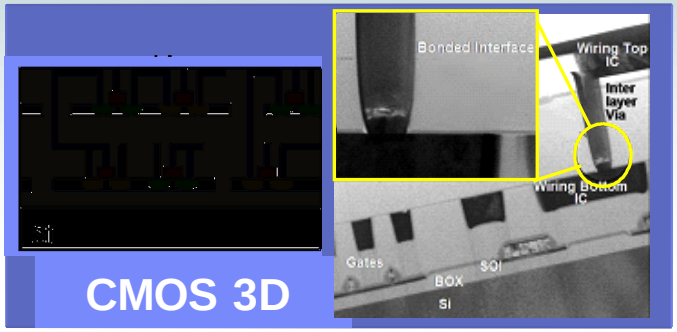
Span of 3D Integration

Packaging



IBM/Samsung

Wafer Fab



IBM

Tezzaron 3D-ICs

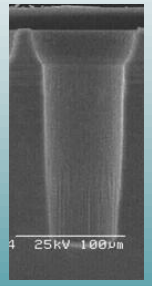
100-1,000,000/sqmm

1000-10M Interconnects/device

1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors

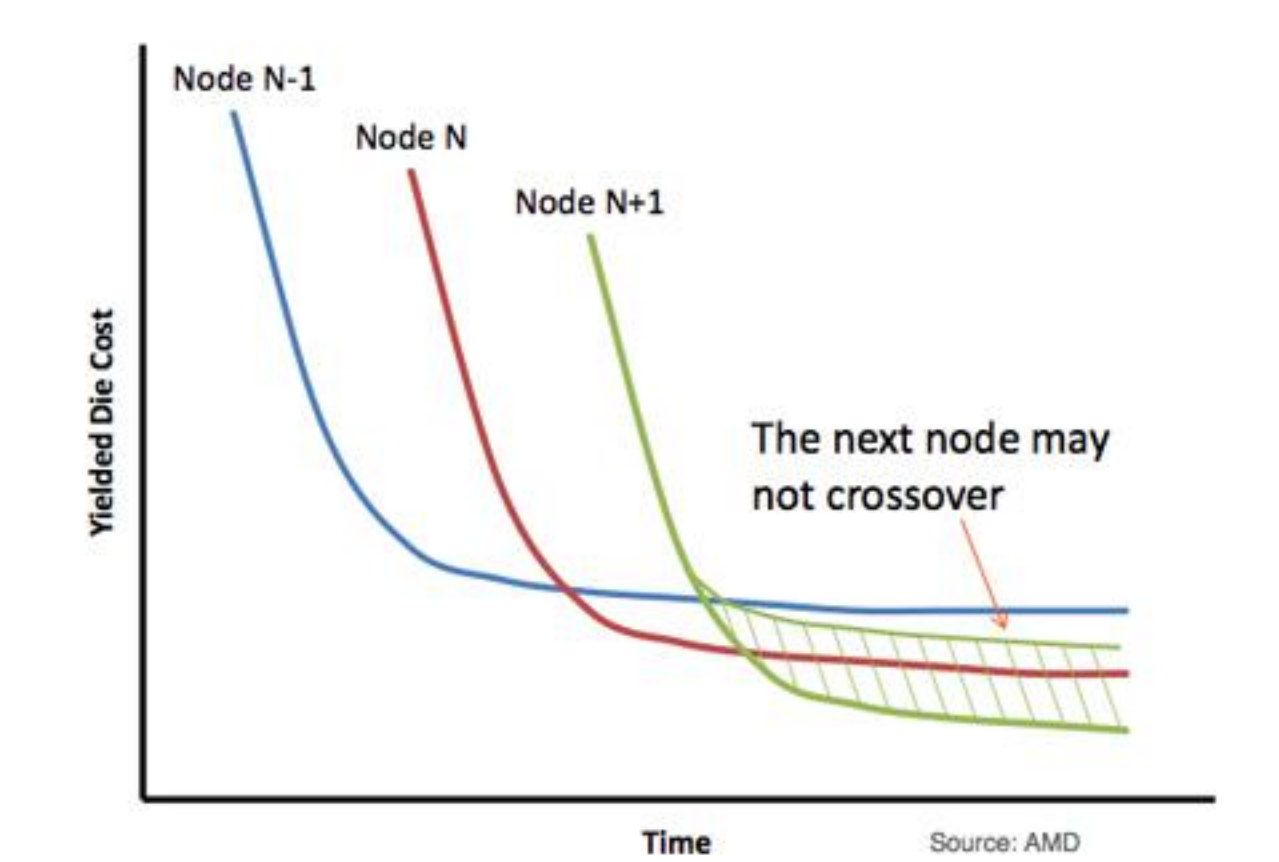


100,000,000s/sqmm

Transistor to Transistor

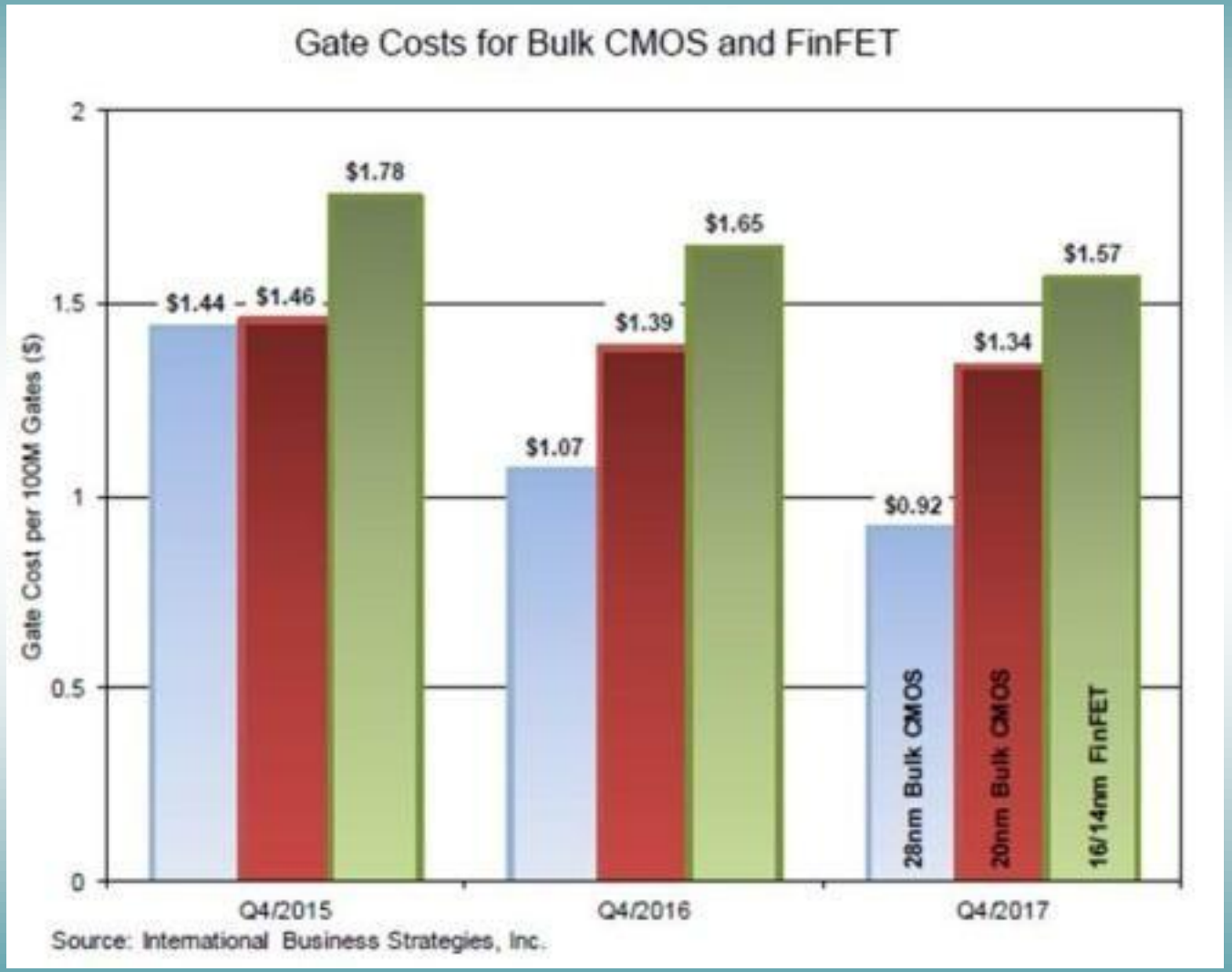
- Ultimate goal

Why 3D? – Expiring Economics

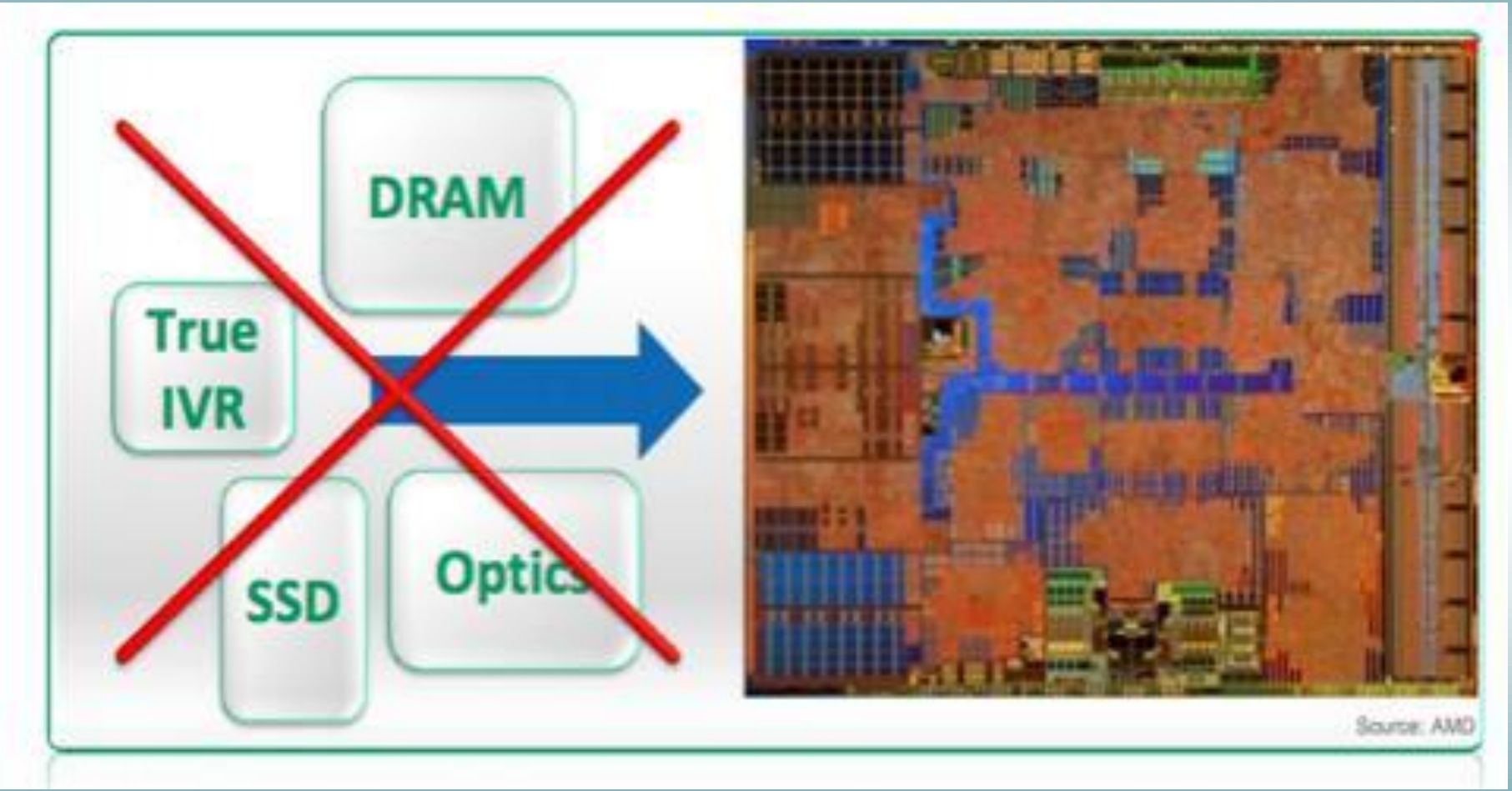


AMD 2014 3D-ASIP

Why 3D? – Expiring Economics

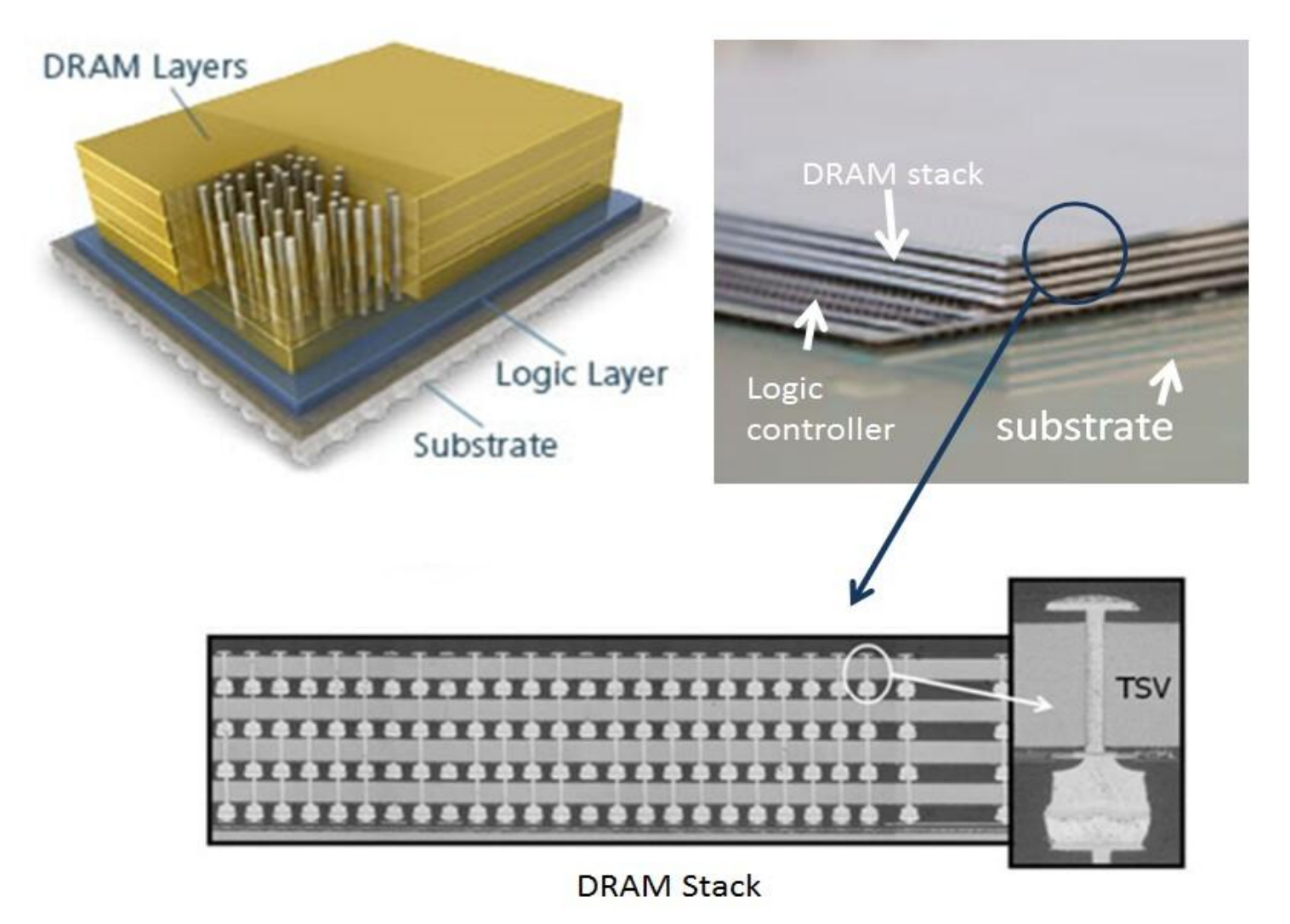


Why 3D? – Apples & Oranges

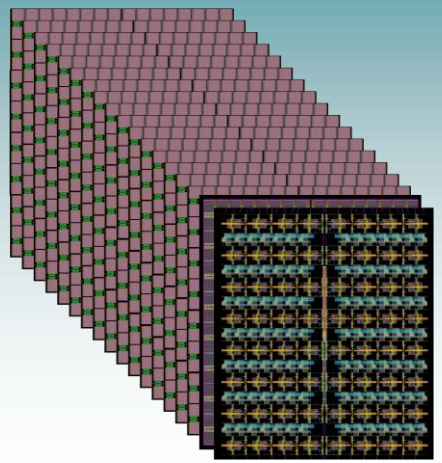


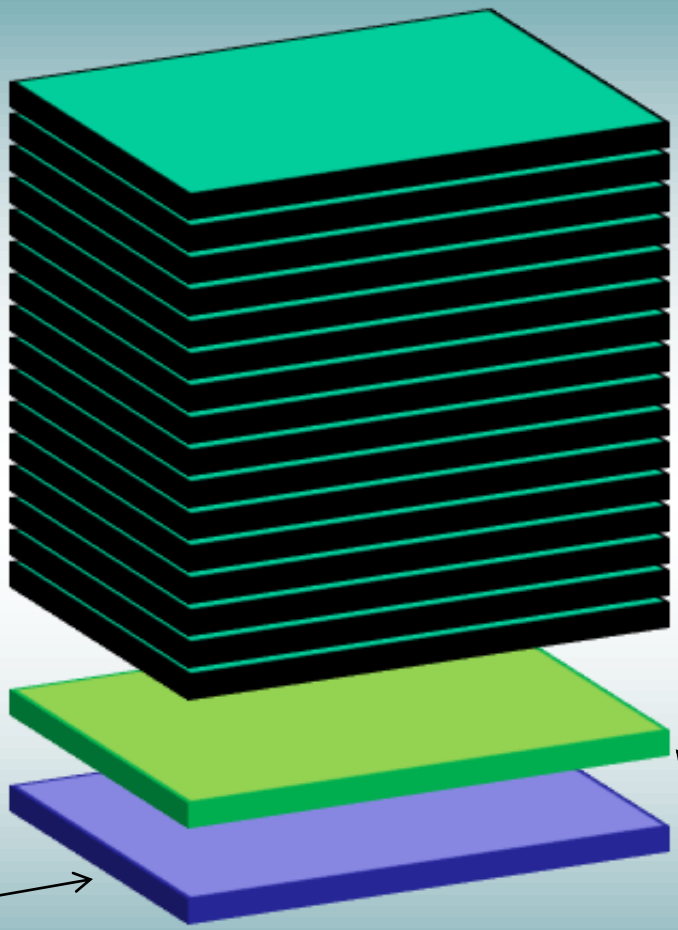
AMD 2014 3D-ASIP

HMC Micrograph



Gen4 “Dis-Integrated” 3D Memory





DRAM layers
4xnm node

2 million vertical connections per lay per die

I/O layer contains: I/O, interface logic and R&R control CPU. 65nm node

Controller layer contains: sense amps, CAMs, row/column decodes and test engines. 40nm node

Better yielding than 2D equivalent!

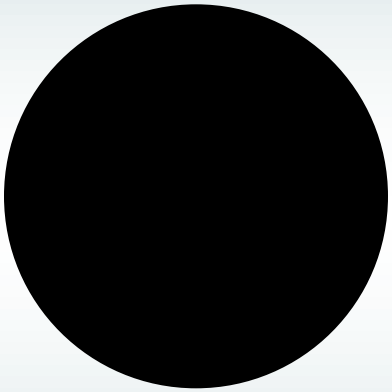
3D Interconnect Characteristics

	SuperContact™ I 200mm Via First, FEOL	SuperContact™ IV 200mm Via First, FEOL	SuperContact™ V 300mm Via F/L, FEOL	SuperContact™ VI 300mm Via F/L, FEOL	Interposer TSV	Bond Points	Die to Wafer
Size L X W X D Material	1.2 µ X 1.2 µ X 6.0µ W in Bulk	0.6 µ X 0.6 µ X 2µ W in SOI	1.2 µ X 1.2 µ X 6µ W in Bulk	0.8 µ X 0.8 µ X 6µ W in Bulk	10 µ X 10 µ X 100 µ Cu	1.2 µ X 1.2 µ Cu	2.5 µ X 2.5 µ Cu
Minimum Pitch	<2.5 µ	1.2 µ	2.4 µ	1.6 µ	30 µ	2.4 µ	5 µ
Feedthrough Capacitance	2fF	0.2fF	1.5fF	1.2fF	150fF	<<	<25fF
Series Resistance	<1.5 Ω	<1.75 Ω	<2.0 Ω	<3.0 Ω	<0.5 Ω	<	<

Small fine grain TSVs are fundamental to 3D enablement

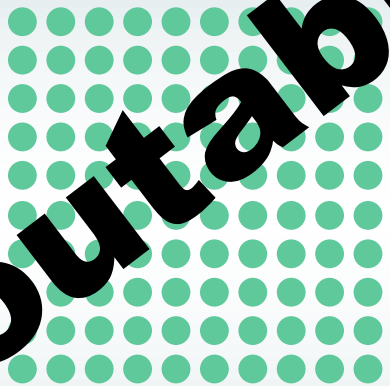
Tiny, Common, Cheap, Fast and…

One



10µ Diameter
Copper TSV

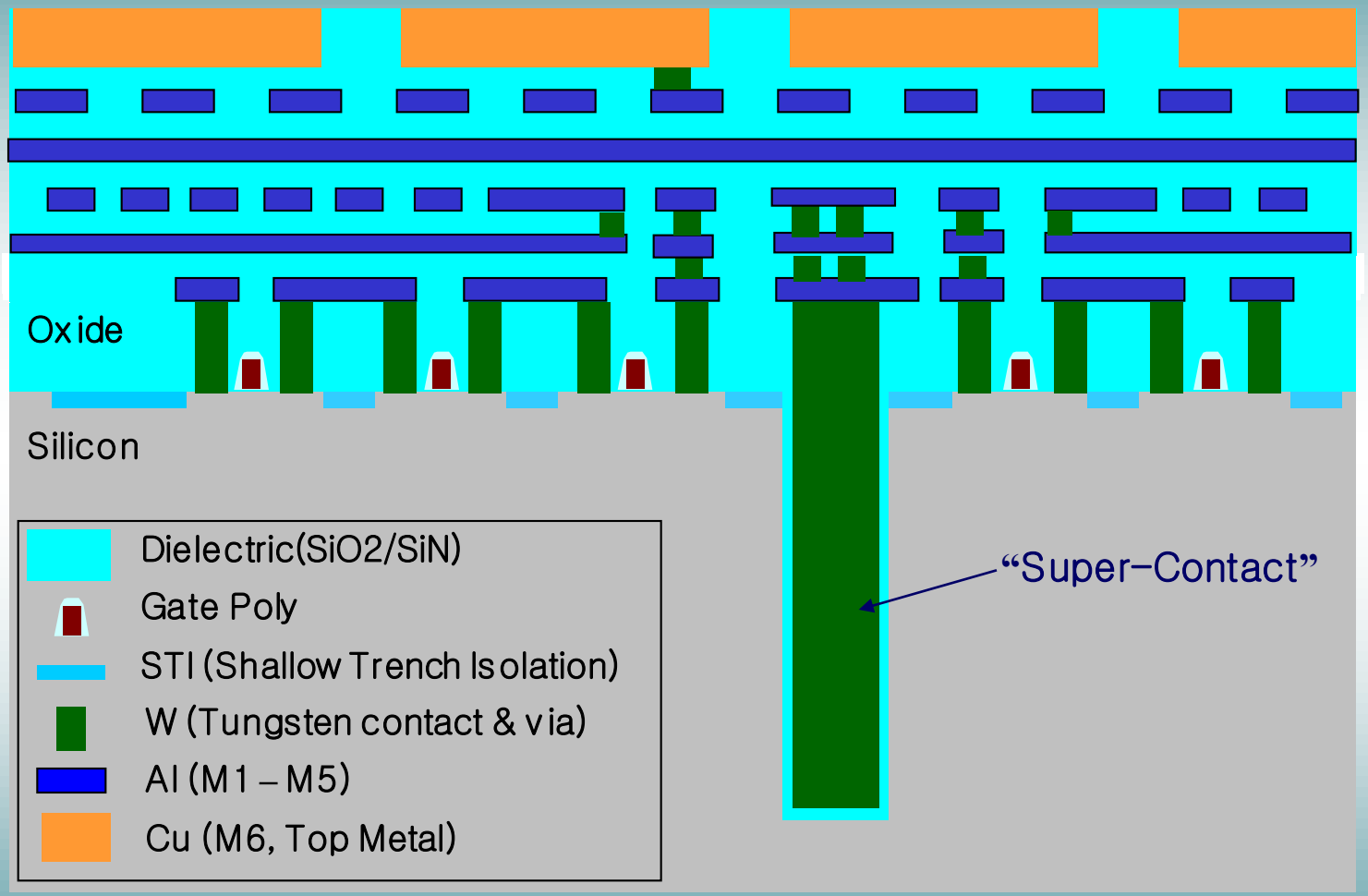
100



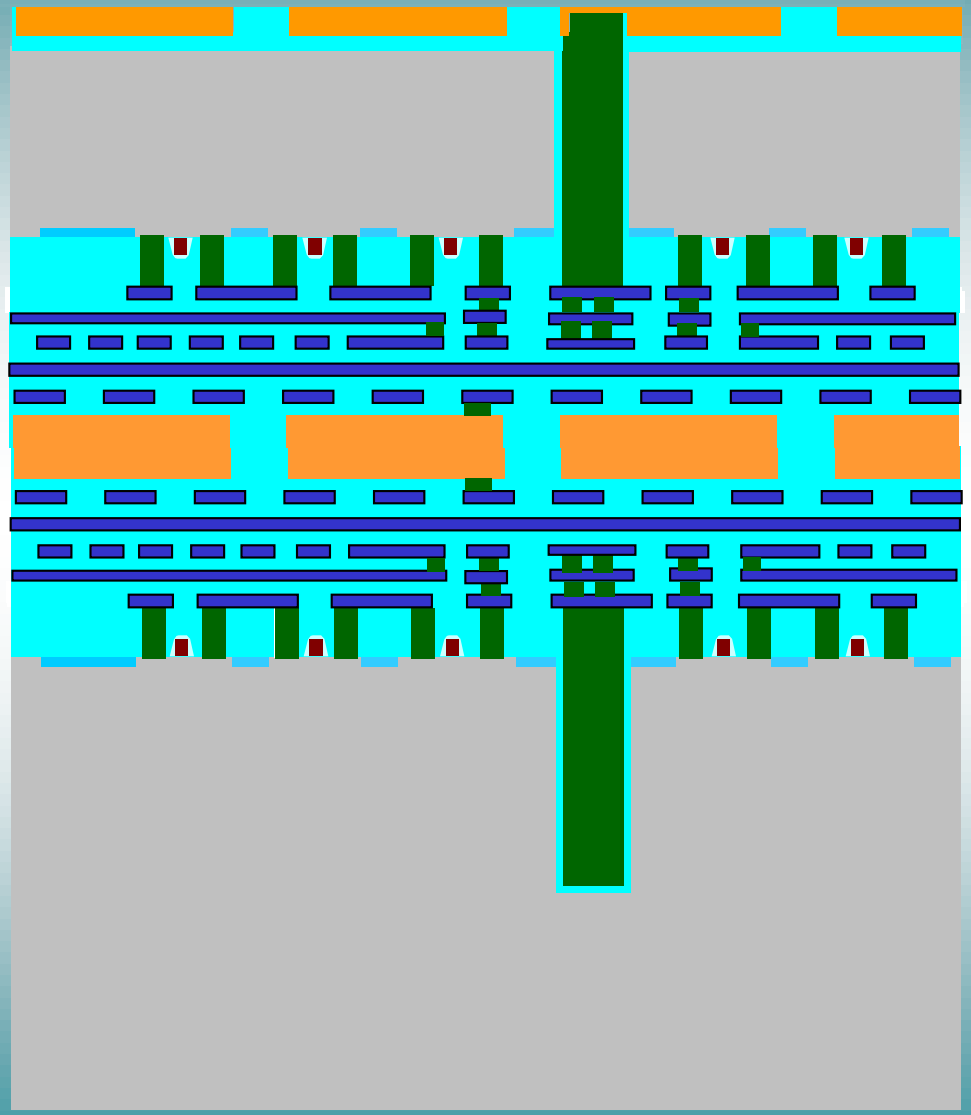
Routable

1µ Diameter
Tungsten SuperContact

A Closer Look at Wafer-Level Stacking



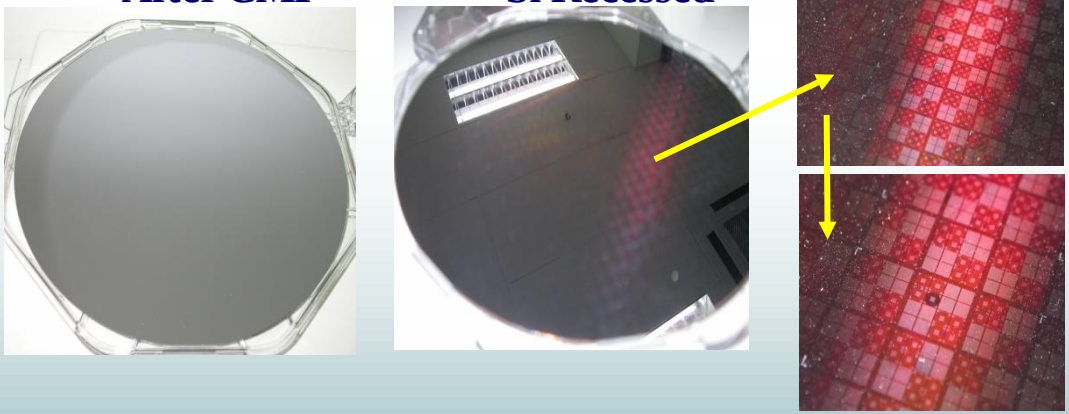
Next, Stack a Second Wafer & Thin:



Stacking Process Sequential Picture

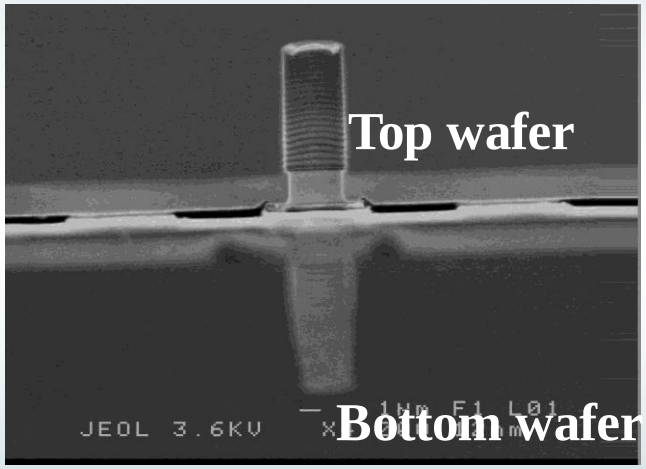
Two wafer Align & Bond → Course Grinded → Fine Grinded

→ After CMP → Si Recessed

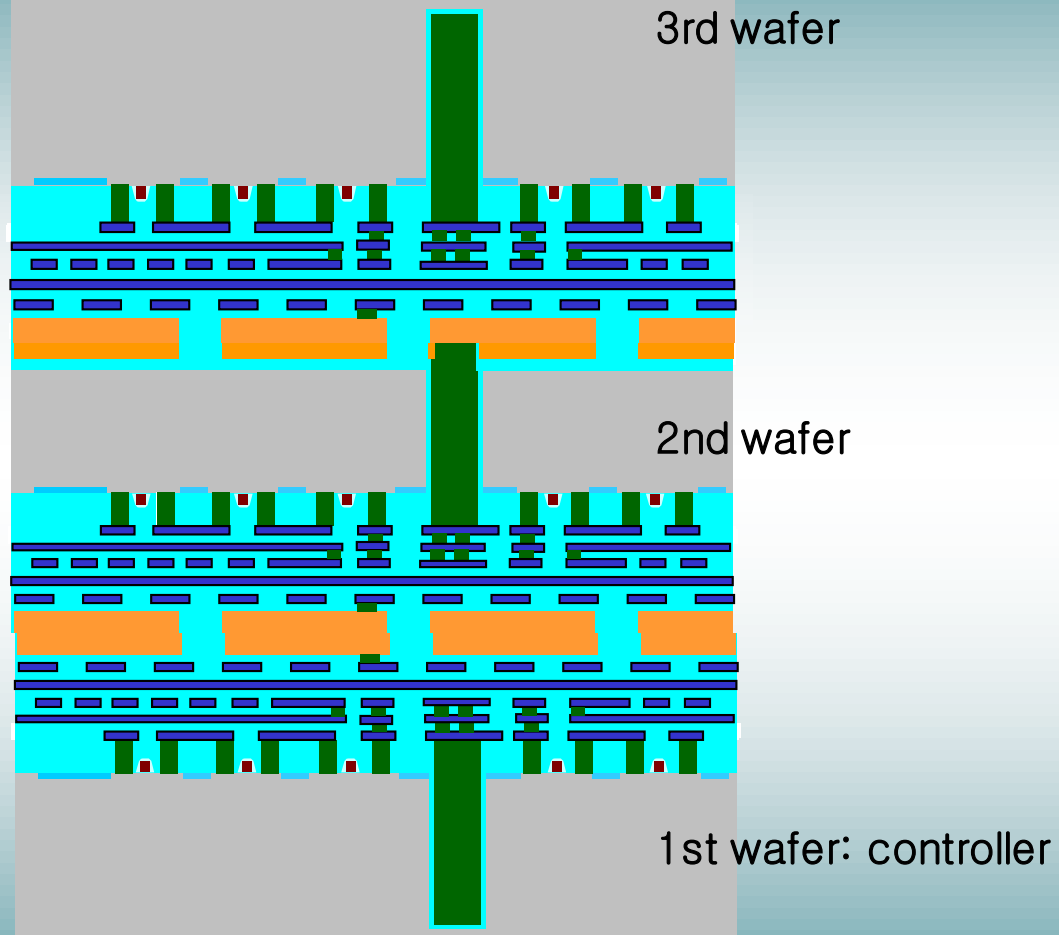


High Precision Alignment

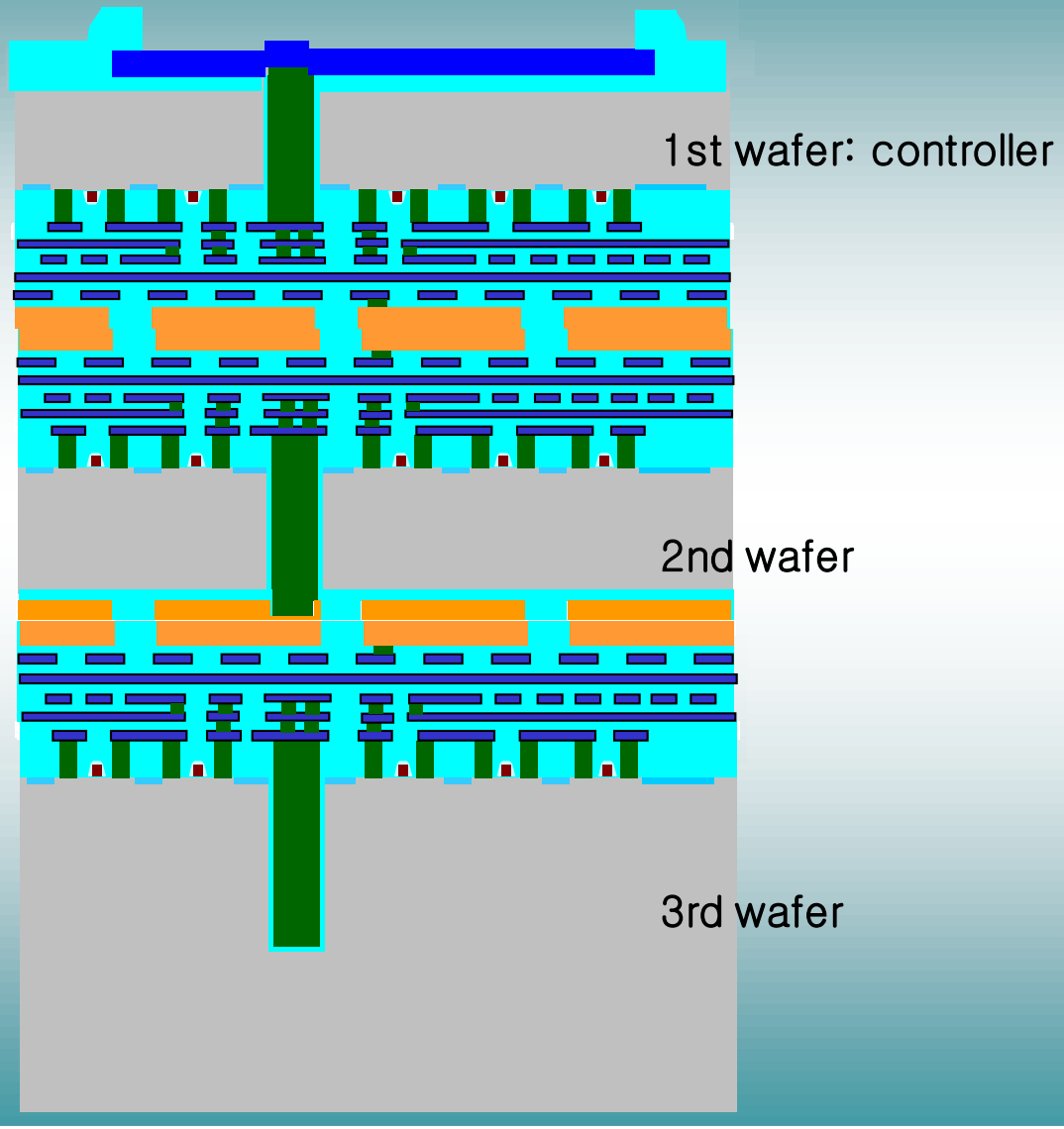
Misalign=0.3um



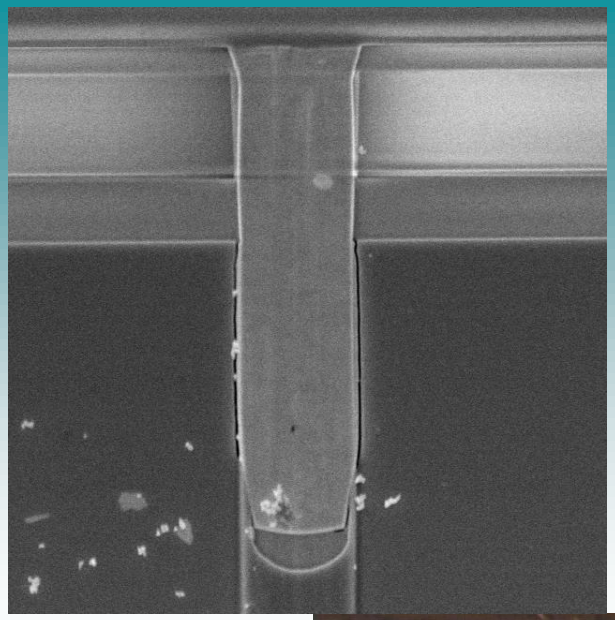
Then, Stack a Third Wafer:

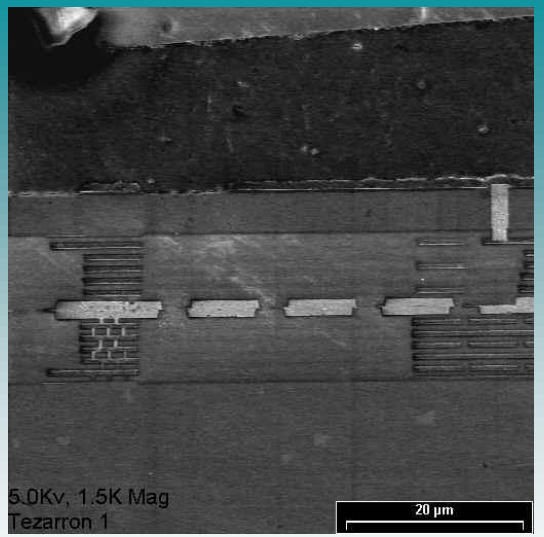


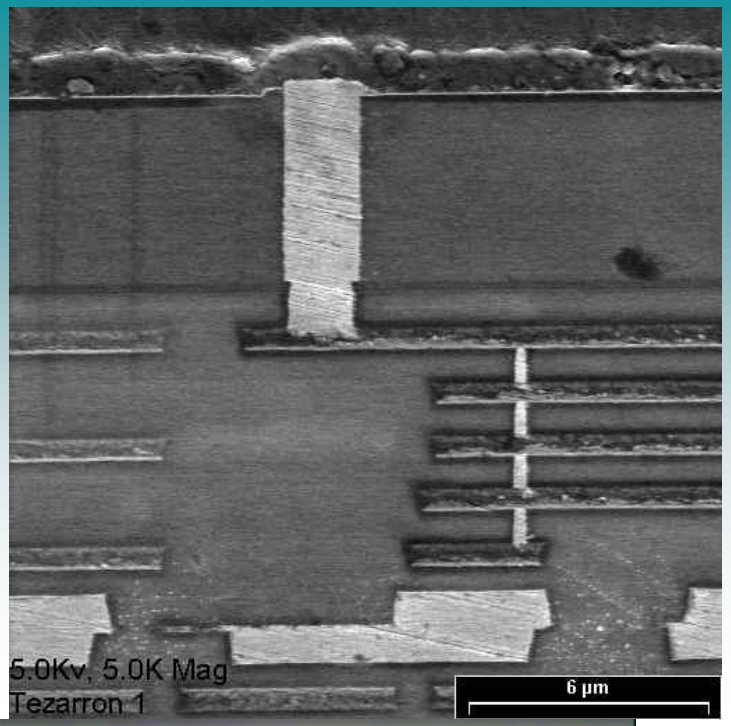
Finally, Flip, Thin & Pad Out:

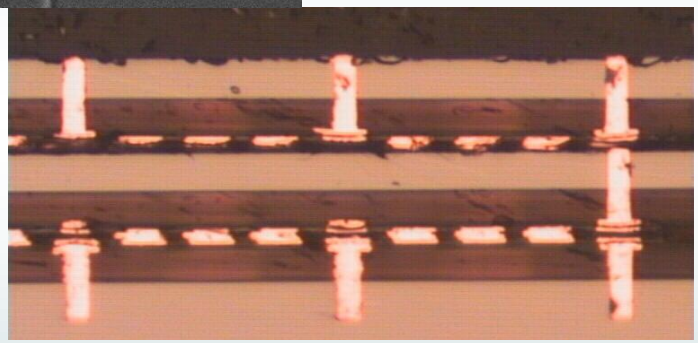


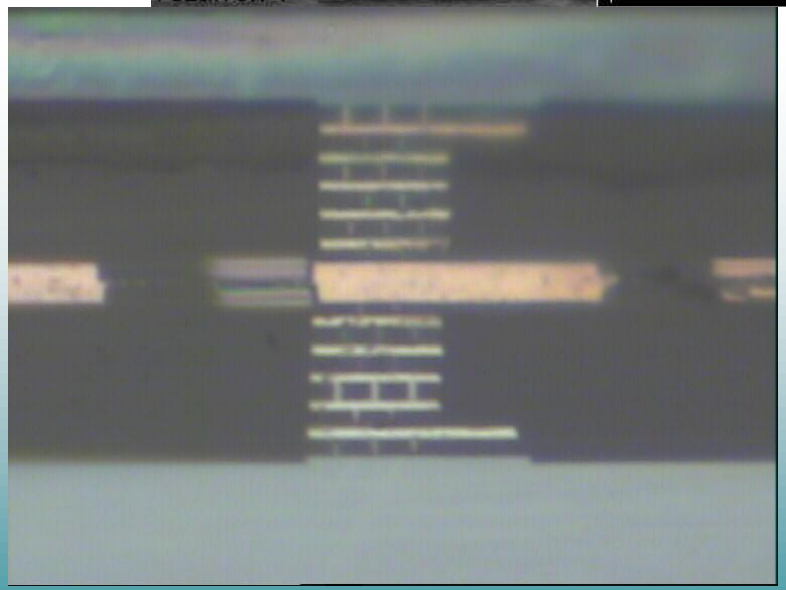
This is the completed stack!

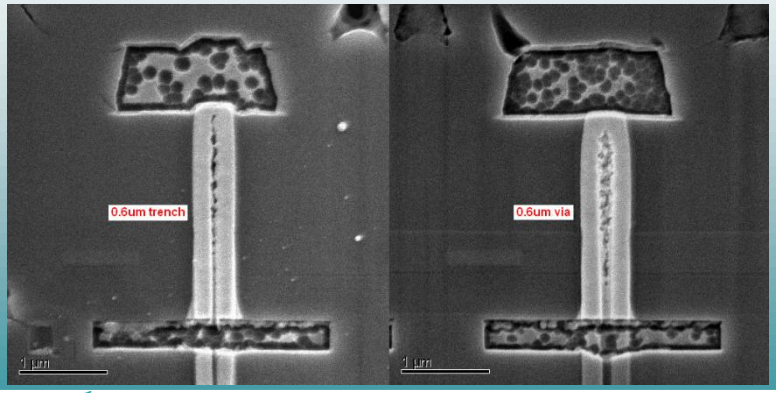



5.0Kv, 1.5K Mag
Tezarron 1
20 µm

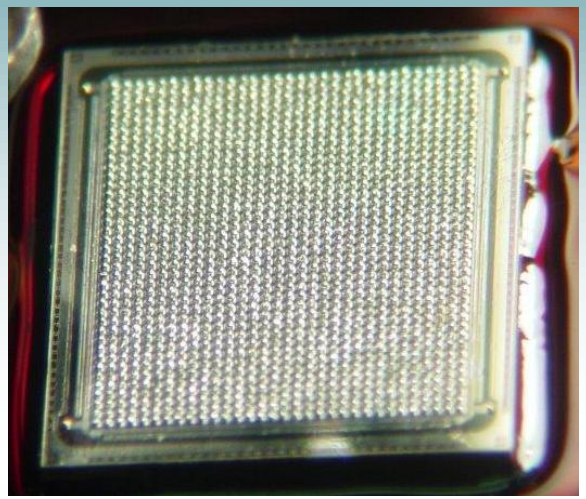

5.0Kv, 5.0K Mag
Tezarron 1
6 µm

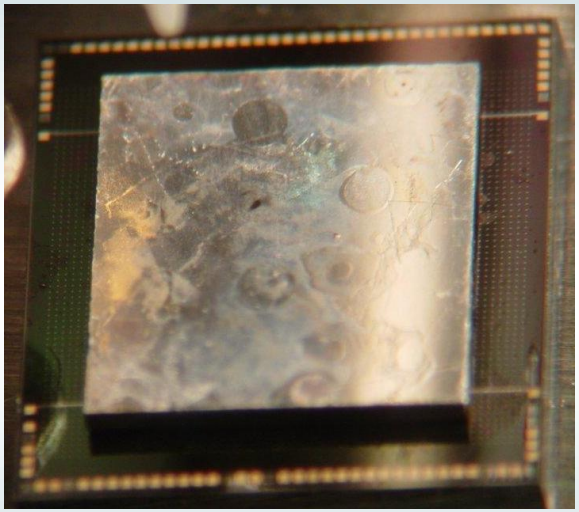


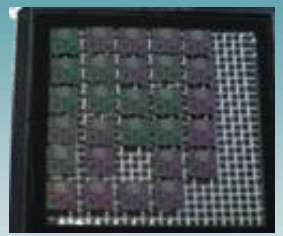


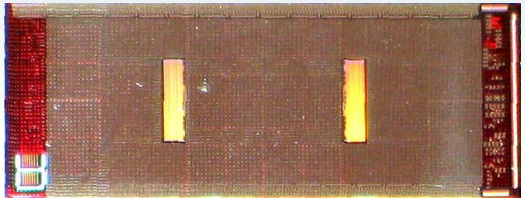

0.6um trench
0.6um via

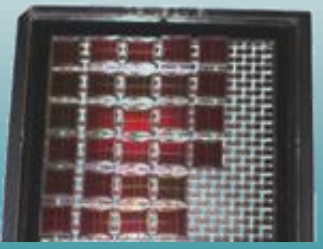
3D Devices

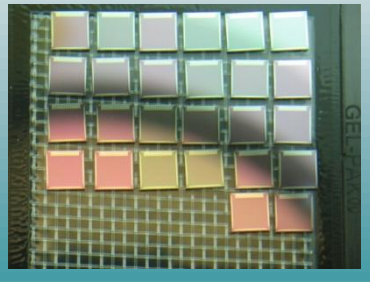


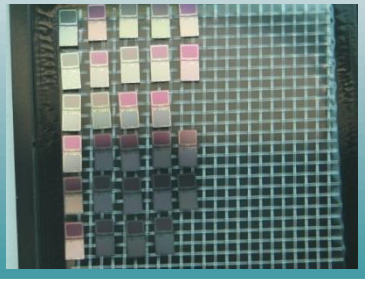


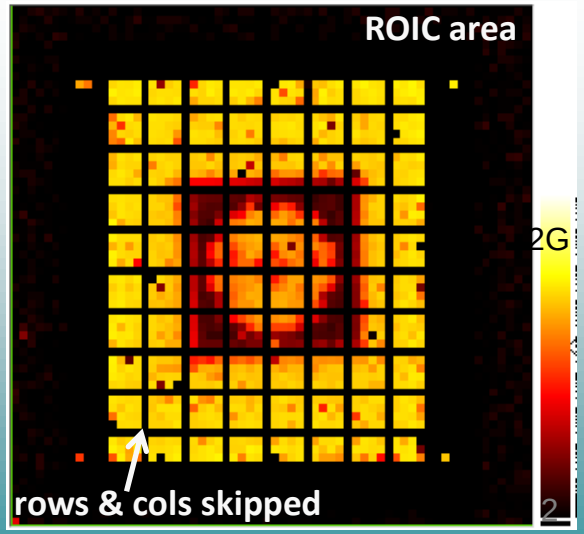




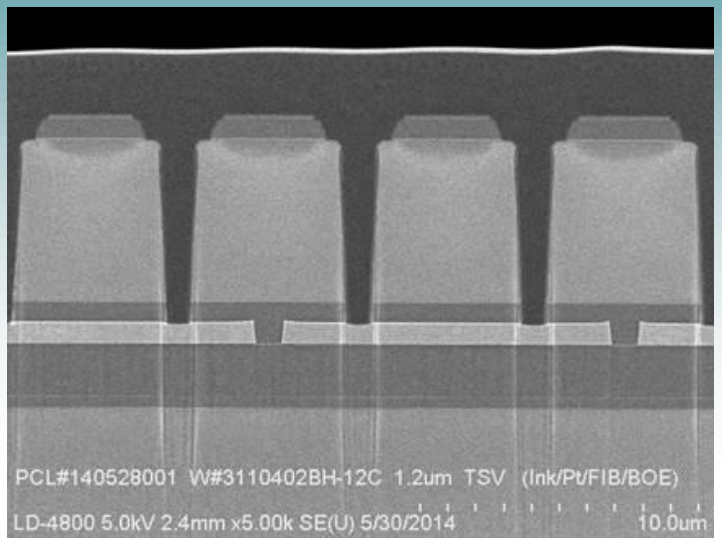


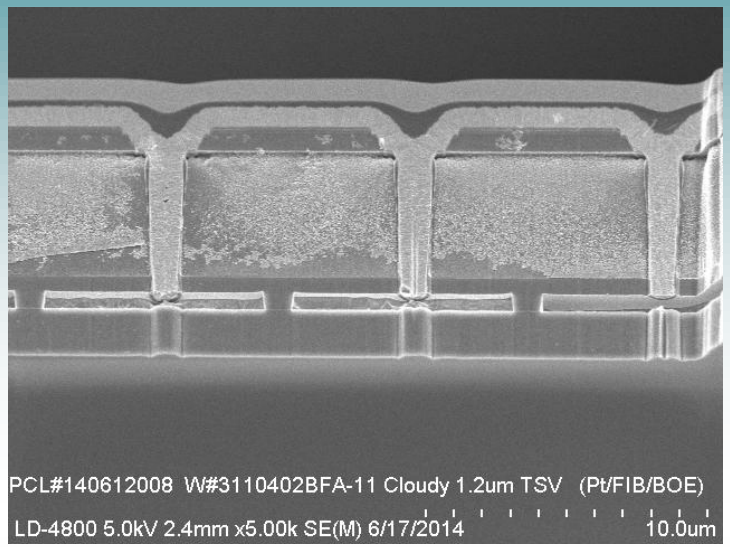


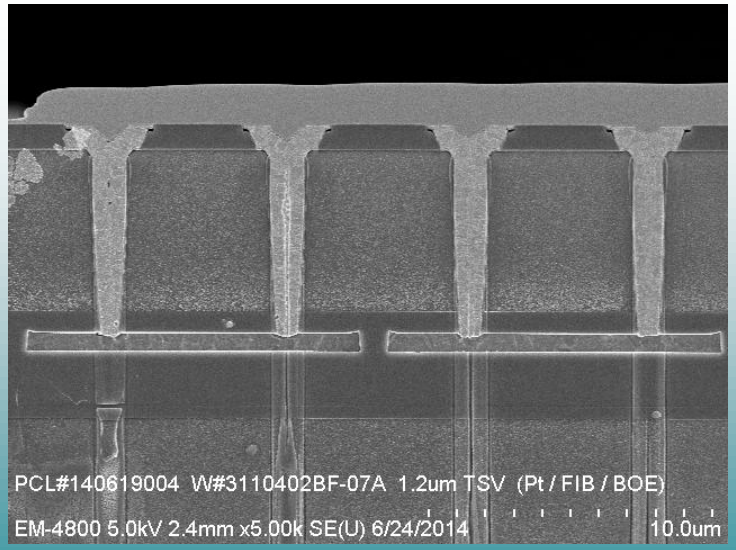




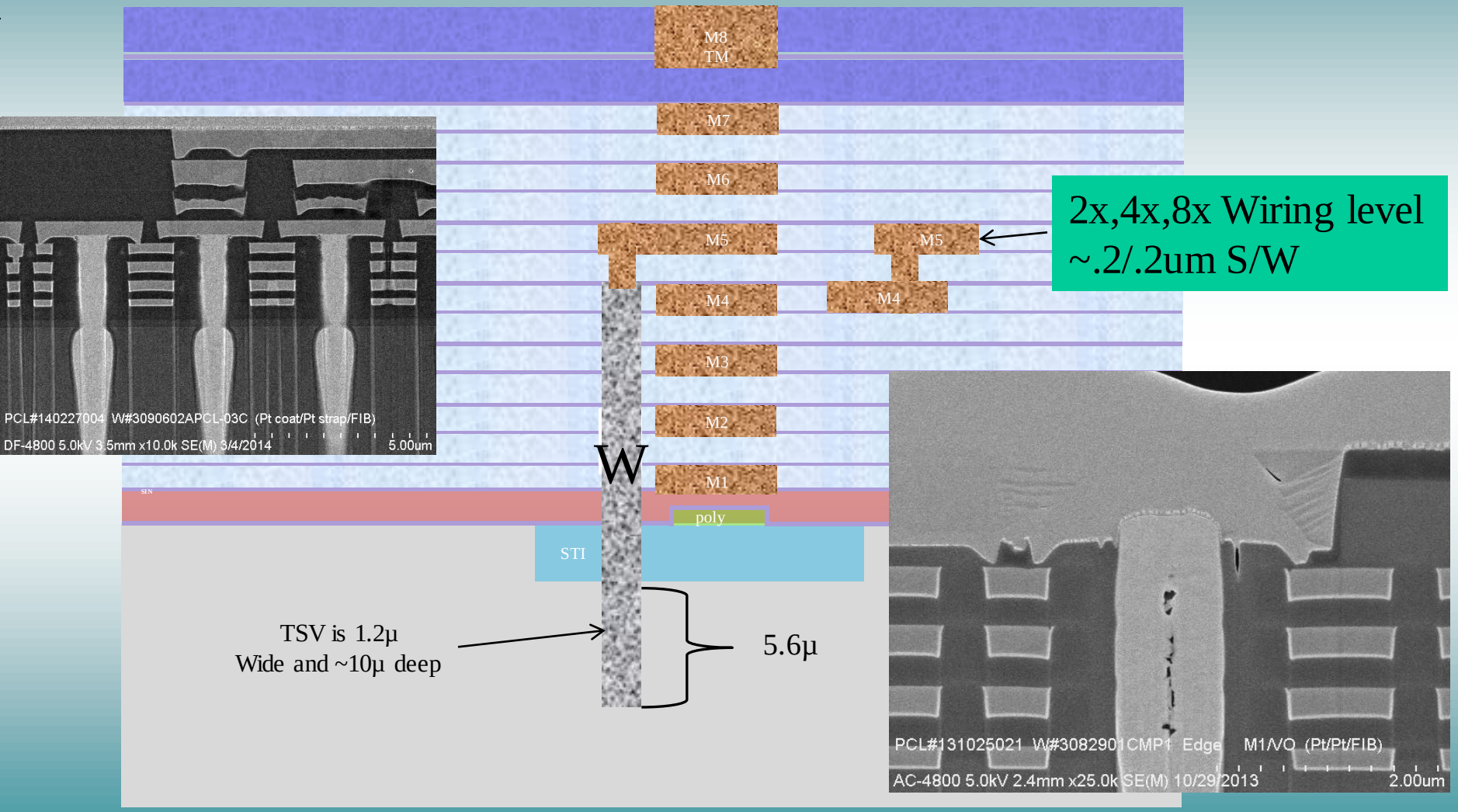
TSV Insertion





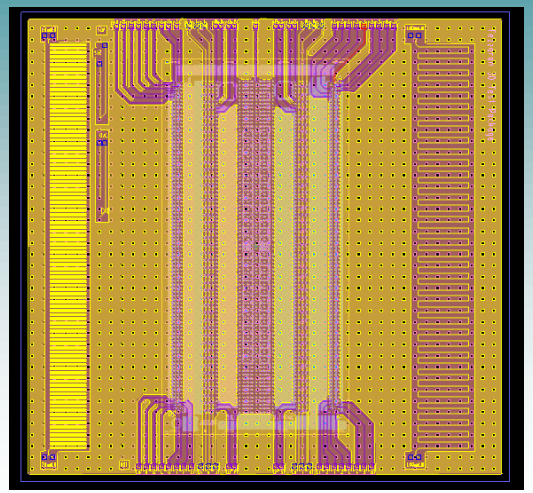


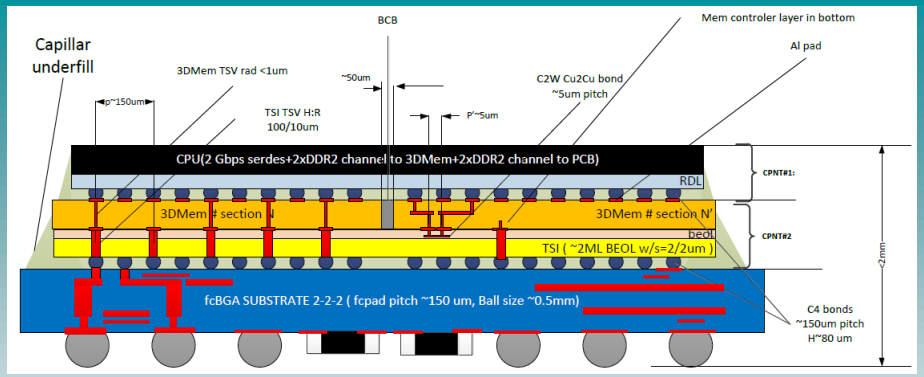
Near End-of-Line TSV Insertion



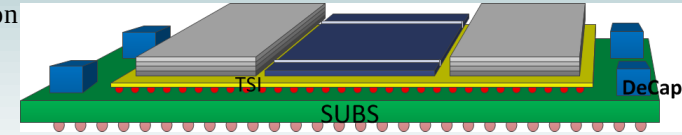
2.5/3D Circuits

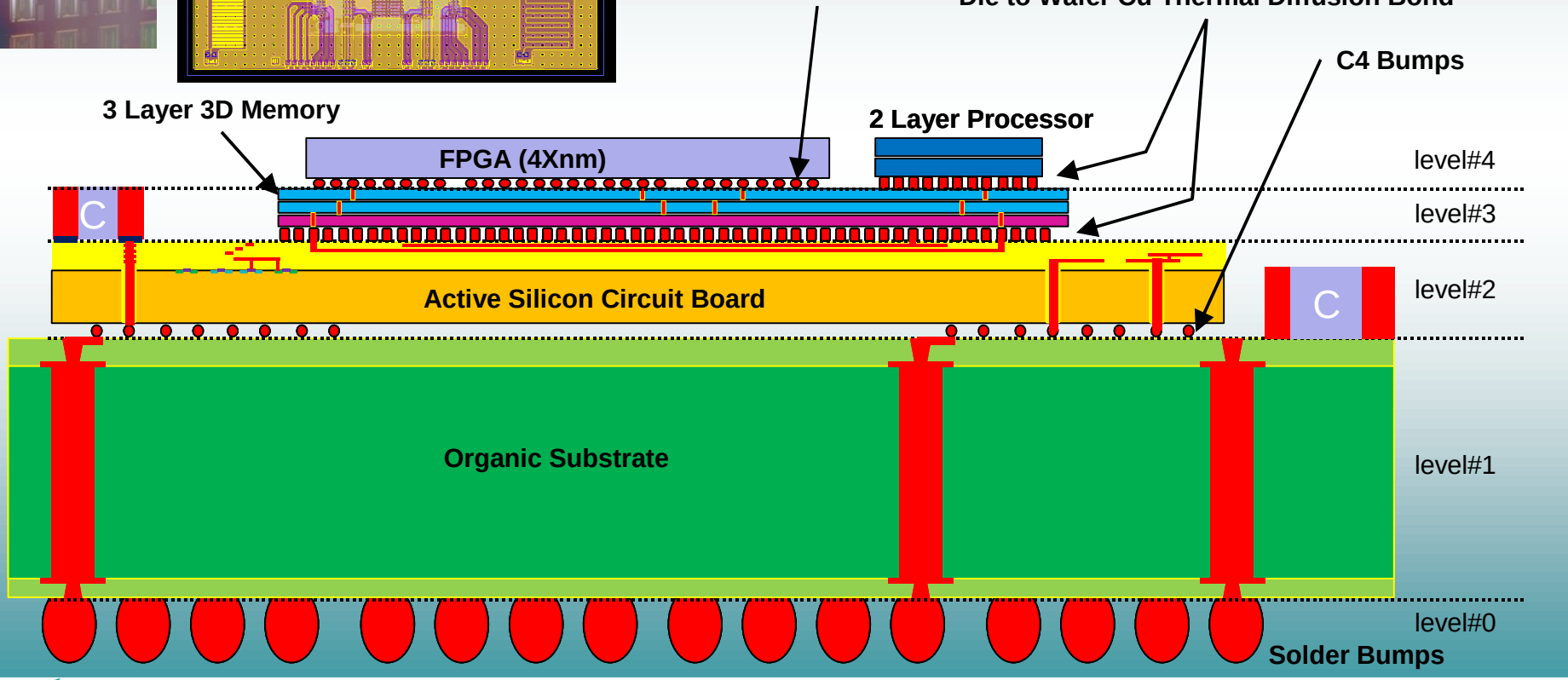
IME A-Star / Tezzaron Collaboration



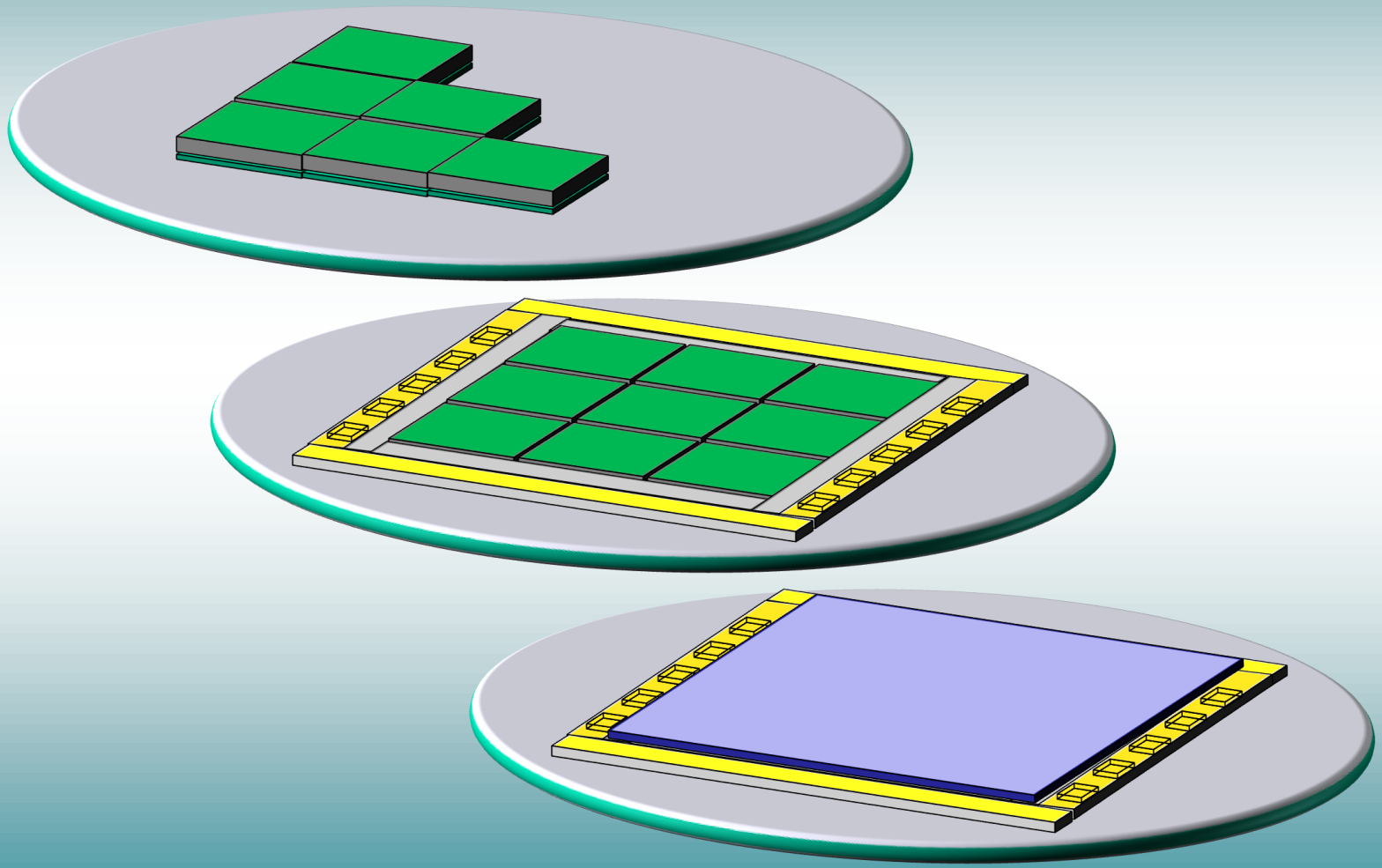


IME A-Star / Tezzaron Collaboration

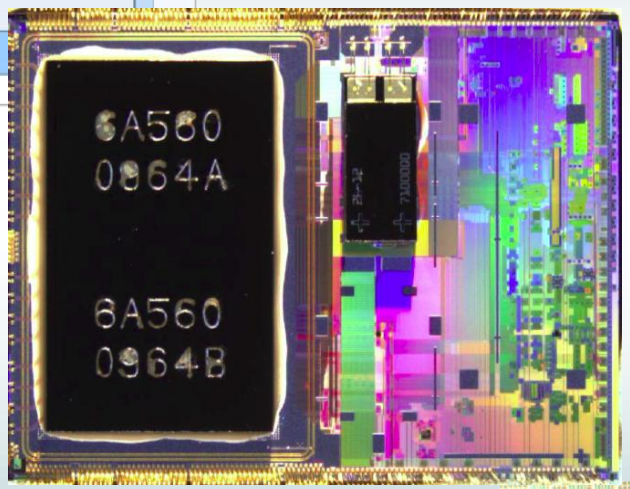


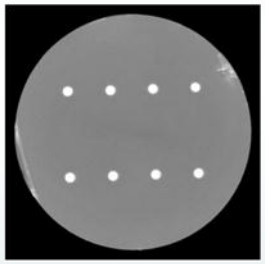


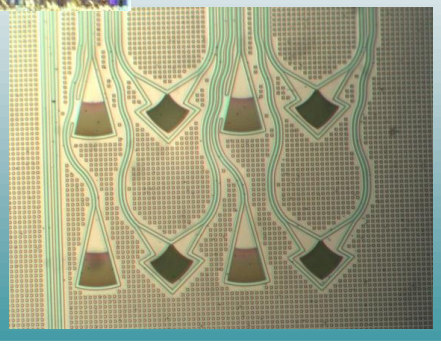
Wafer-scale FPA



Luxtera 2.5D Photonic Data Pump

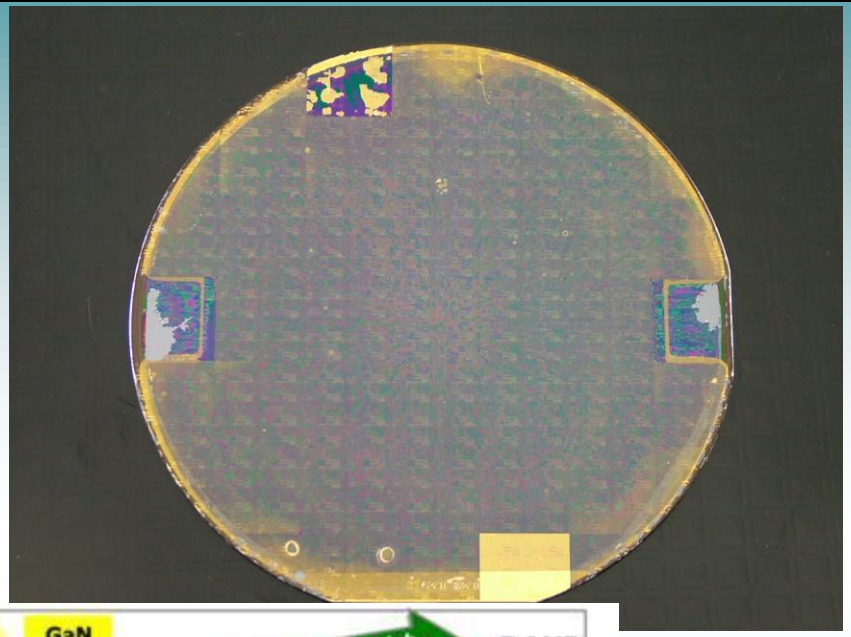




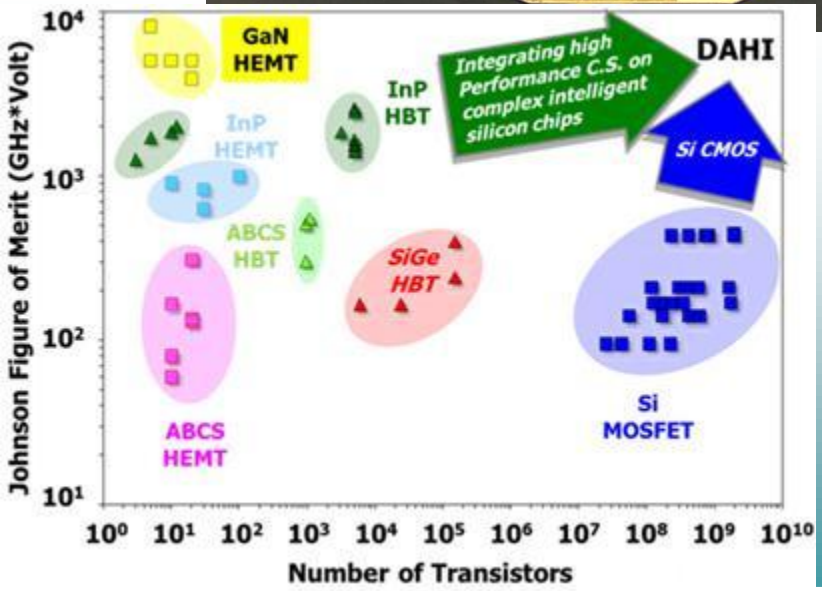


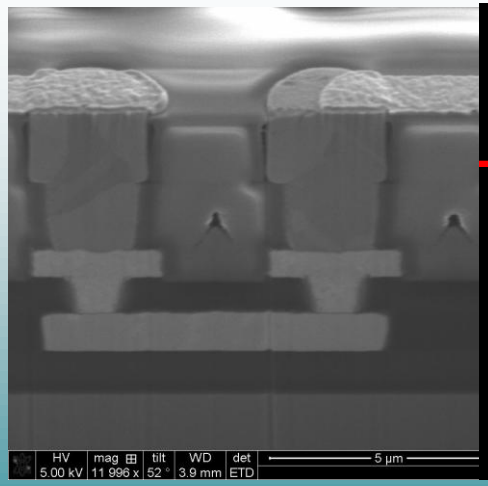
- 2.5pJ/bit power
- Bare metal protocol
  - Ultra low latency
  - Protocol agnostic
- 8 core Fiber
- 25Gb SERDES or 3.125Gb interface
- Self-calibrating self-tuning
- >1.6Tb/s payload

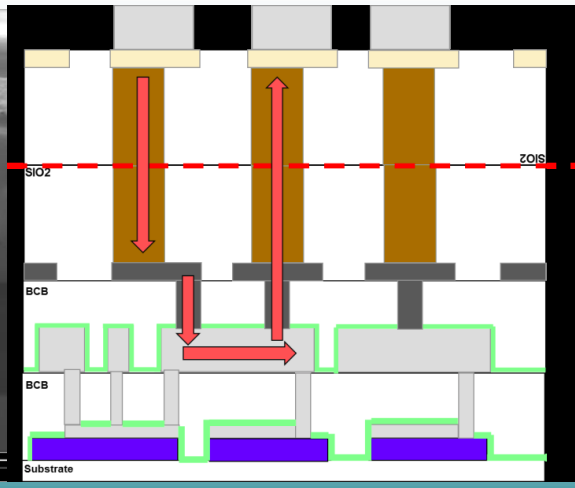
Mixed CMOS-3/5 100mm InP/CMOS



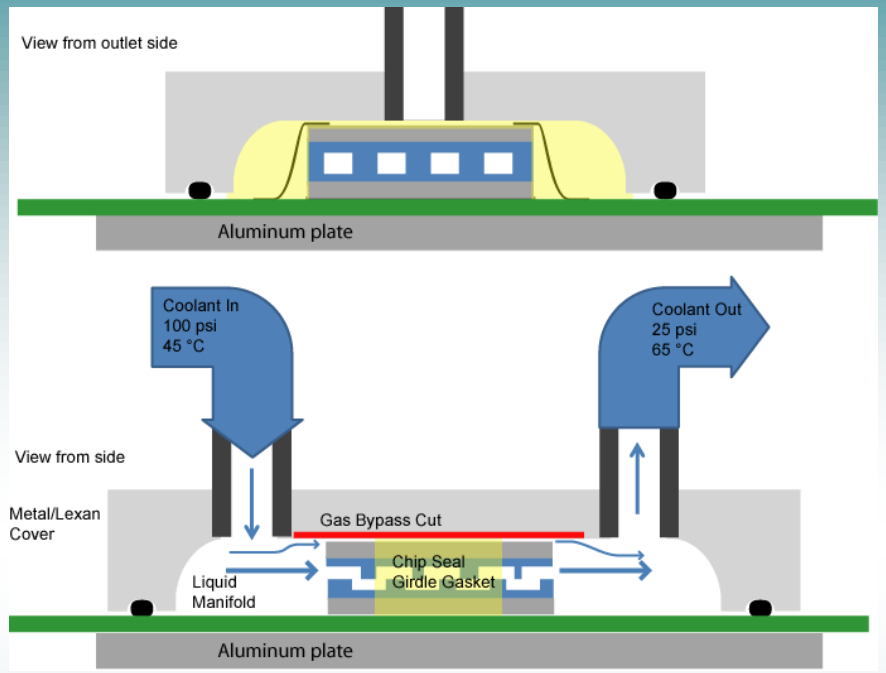
- GaN
- 3D CMOS/InP/GaN
- Graphene

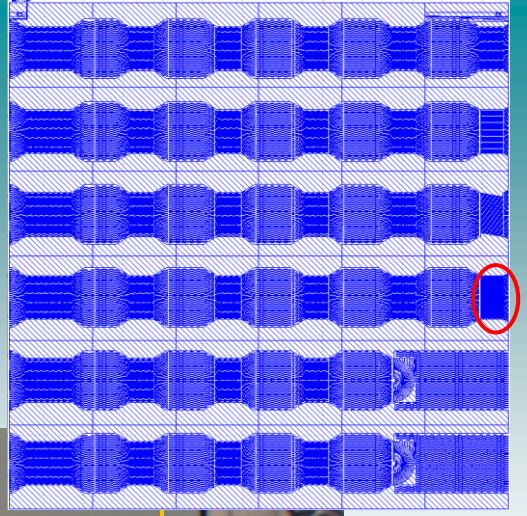


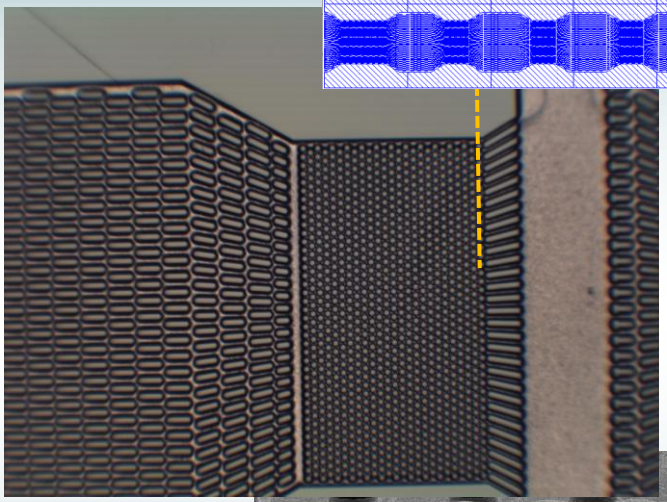


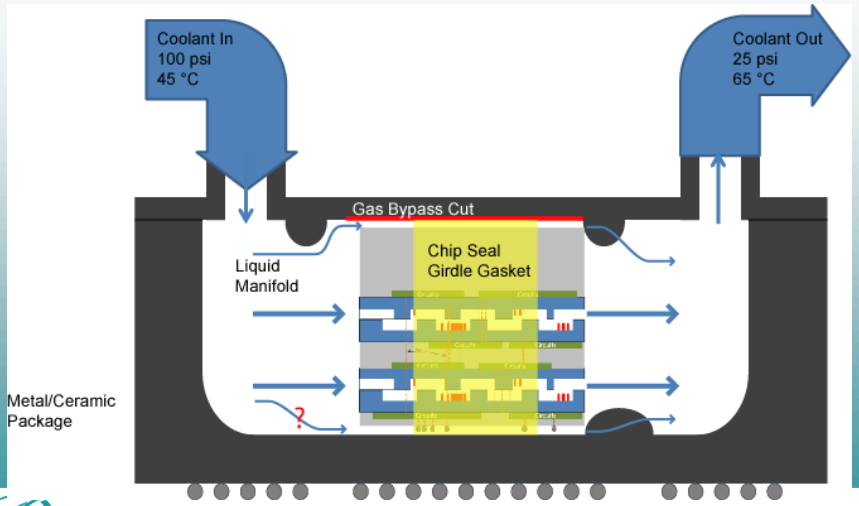


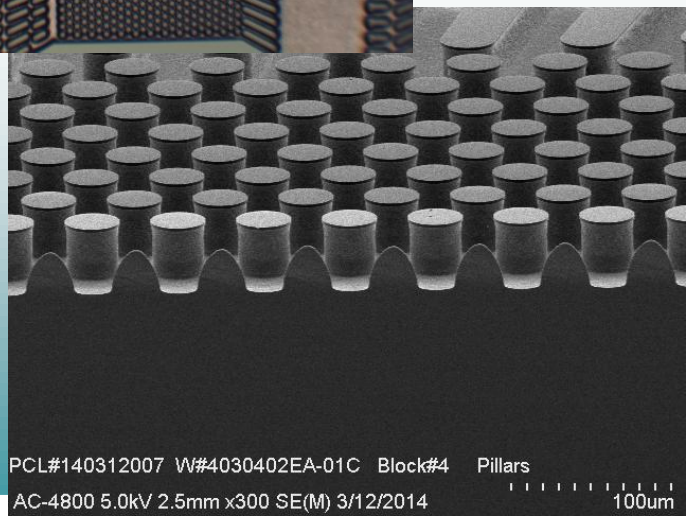
Cooling Block Illustrations





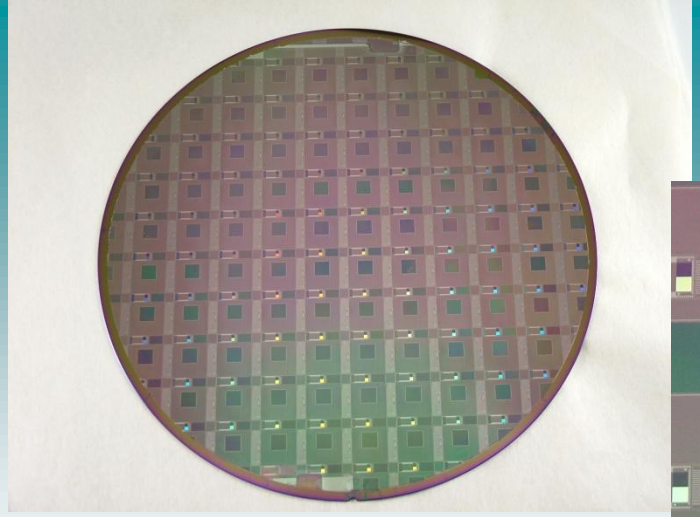


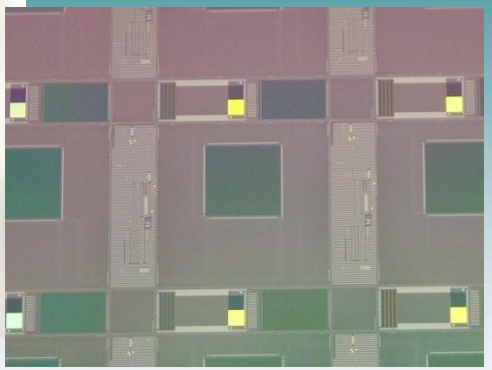


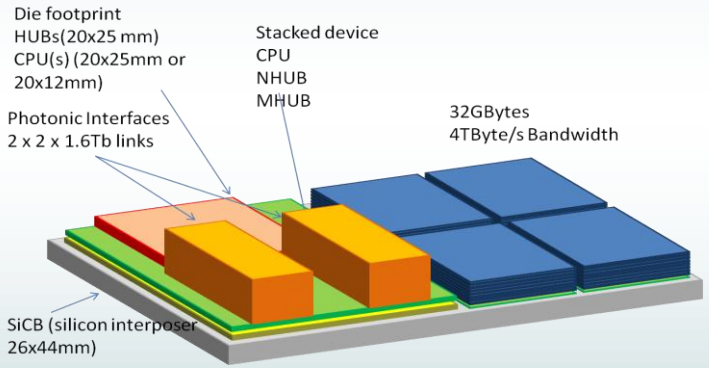


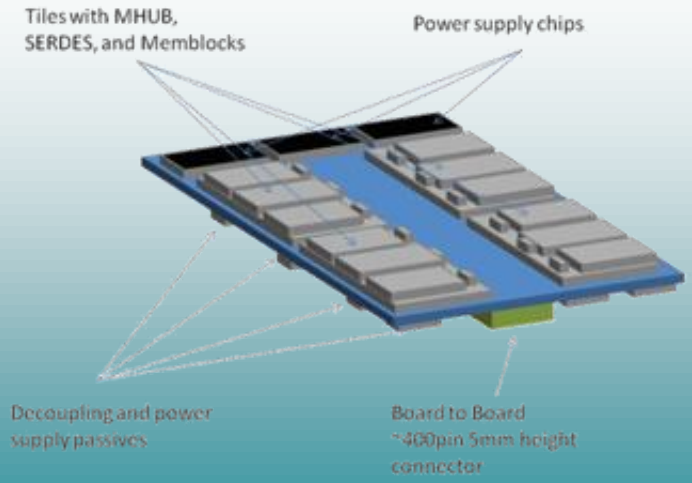
“5.5D” Systems

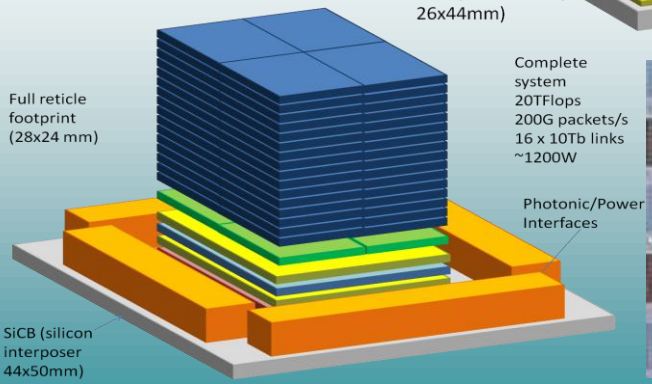
- SIP/SSIP
  - Power Conversion
  - Cooling
  - Photonics
- Optimization
  - Extending to power
- Mixed PCB/IC Metaphor

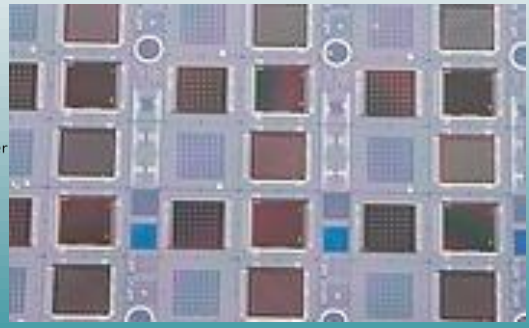




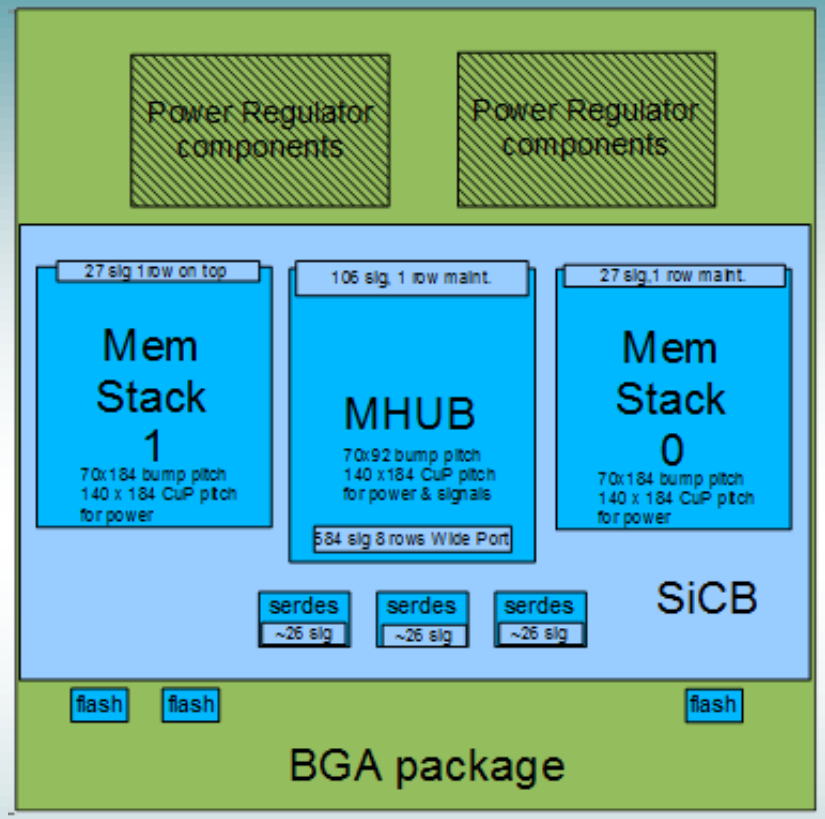


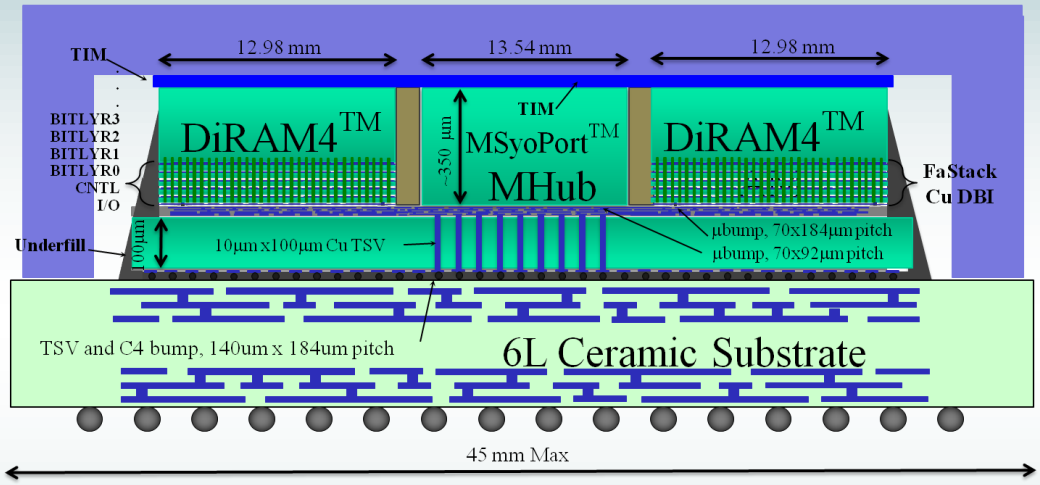






Package Floor Plan





Tezzaron/Novati 3D Technologies

- "Volume" 2.5D and 3D
- Interposers
- Cu-Cu, DBI®, Oxide, IM 3D assembly
- 193nm, 248nm, I-Line Litho
  - 70nm PS
  - 35nm DP
- 90nm CMOS
- 200/300mm
- Avalanche, SPM
- Fab1 Class 10 68K sf
- Fab2 Class 100 12K sf

Fusion Verses Bump Bonding

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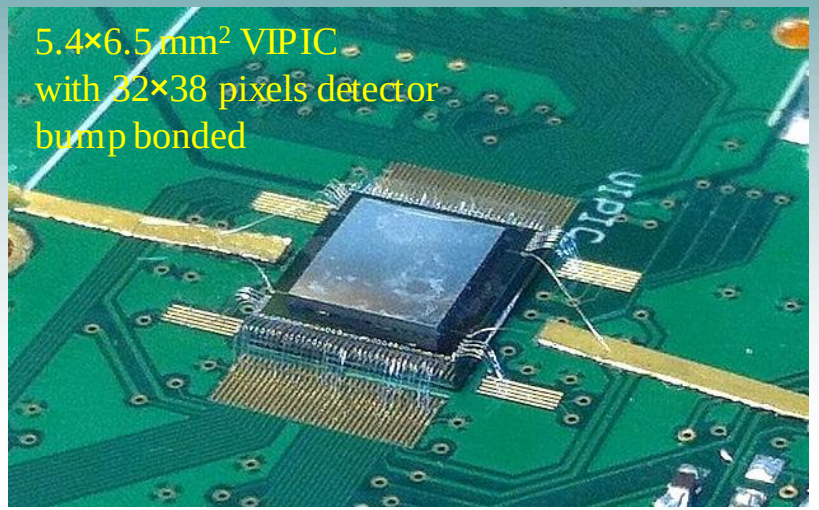
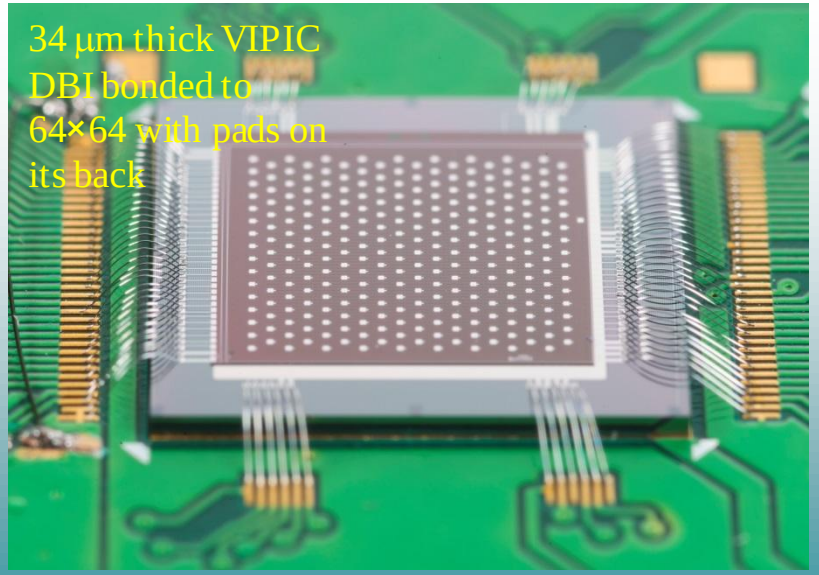
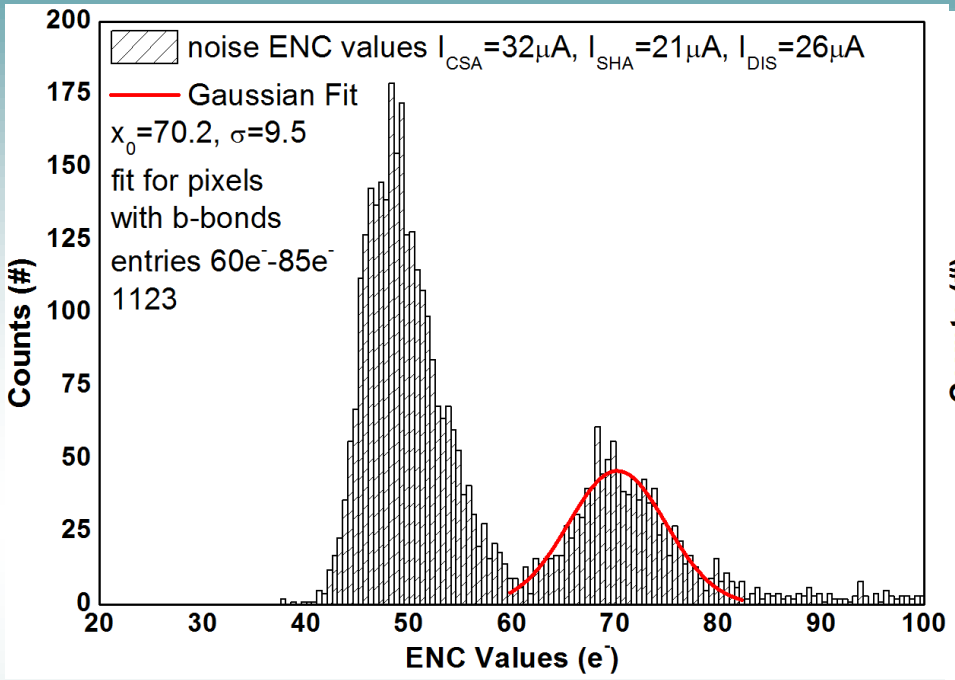
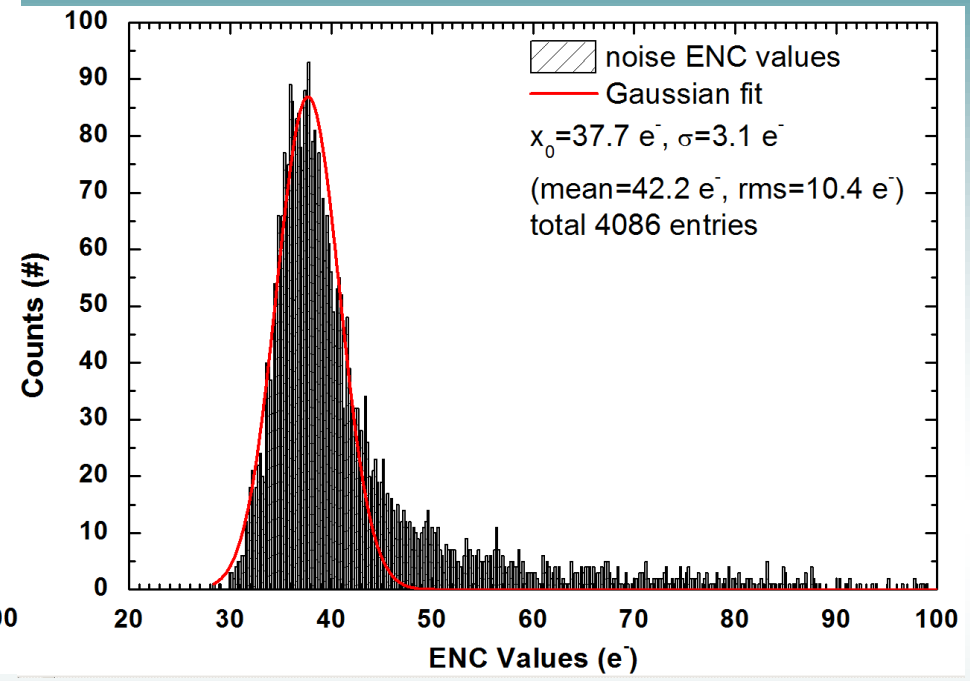




ENC comparison: bump vs. fusion bonded



Bump-bonded VIPIC



Fusion bonded VIPIC

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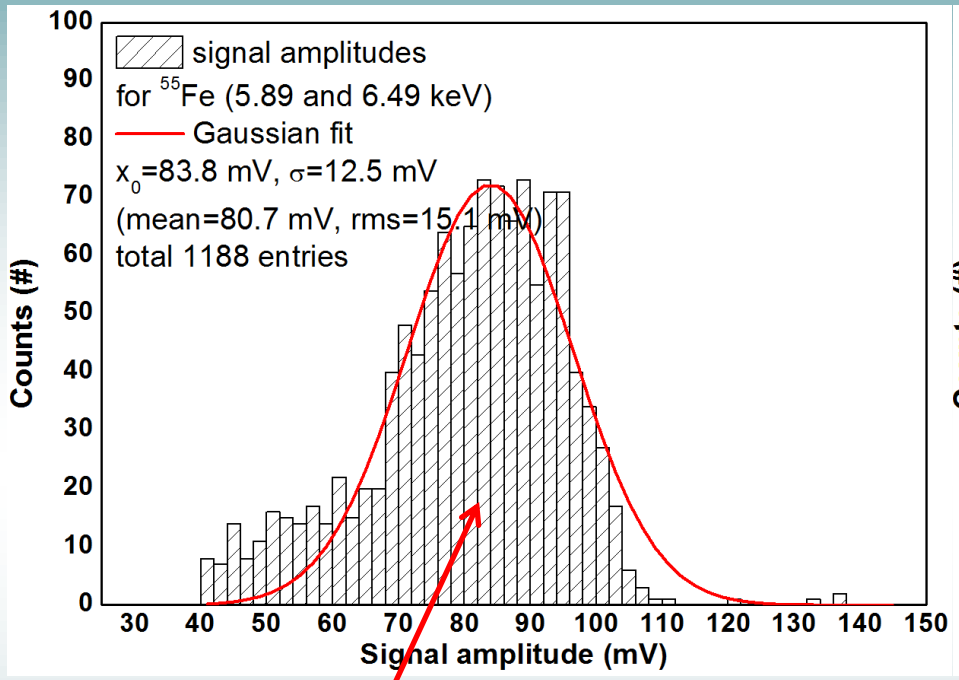
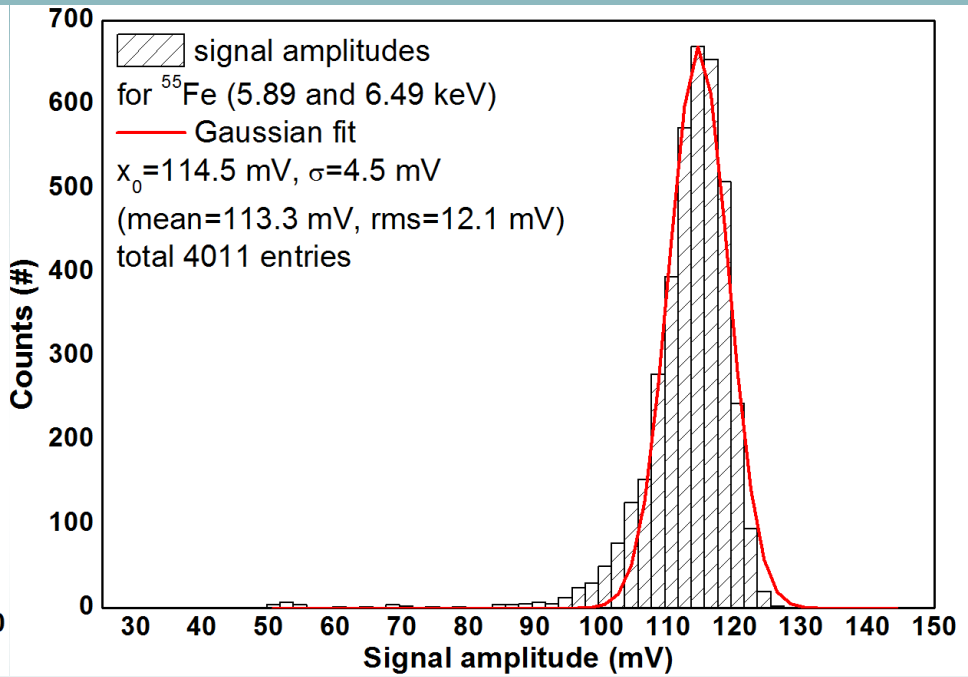
Signal amplitude comparison: bump vs. fusion bonded





32×38 =1216 pixels bump-bonded

Amplitude for bump-bonded VIPIC

Amplitude for fusion bonded VIPIC

Gain is higher for fusion bonded device

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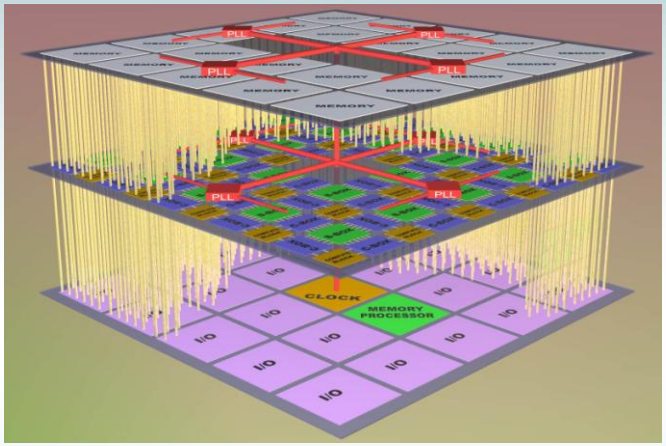
Summary

- "One stop" 2.5/3D solution provider
- Open technology platform
- Volume 2.5D Si interposer production
- Volume 3D assembly
- TSV Insertion
- Silicon, 3/5 materials, carbon nanotubes



Sensors

Computing

MEMS

Communications