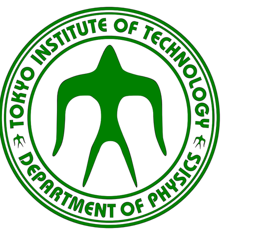
# IBL Modules Construction Experience and Developments for Future Upgrade

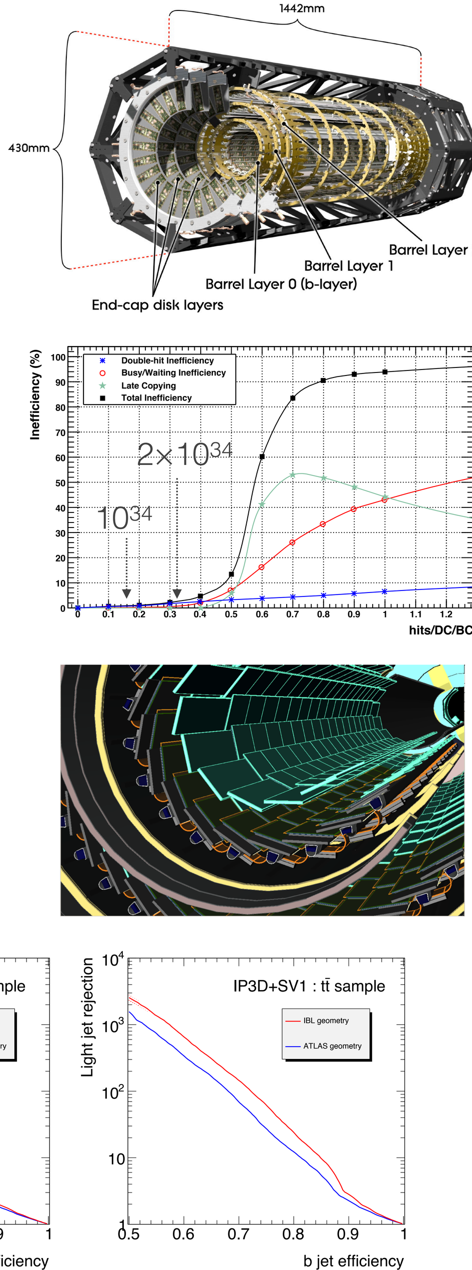



Kazuki Motohashi (Tokyo Institute of Technology, Japan) on behalf of the ATLAS Collaboration

The first upgrade of the ATLAS Pixel Detector is the Insertable B-Layer (IBL), just installed in May 2014 in the core of the detector itself. Two different silicon sensor technologies, planar n-in-n and 3D, were used, connected with the new generation 130nm IBM CMOS FE-I4 readout chip via solder bump-bonds. Production quality control tests were set up to verify and rate the performance of the modules before integration onto staves. An overview of module design and construction, the quality control results and production yield will be discussed, as well as future developments foreseen for future detector upgrades.

## ATLAS Pixel Detector & Insertable B-Layer (IBL)

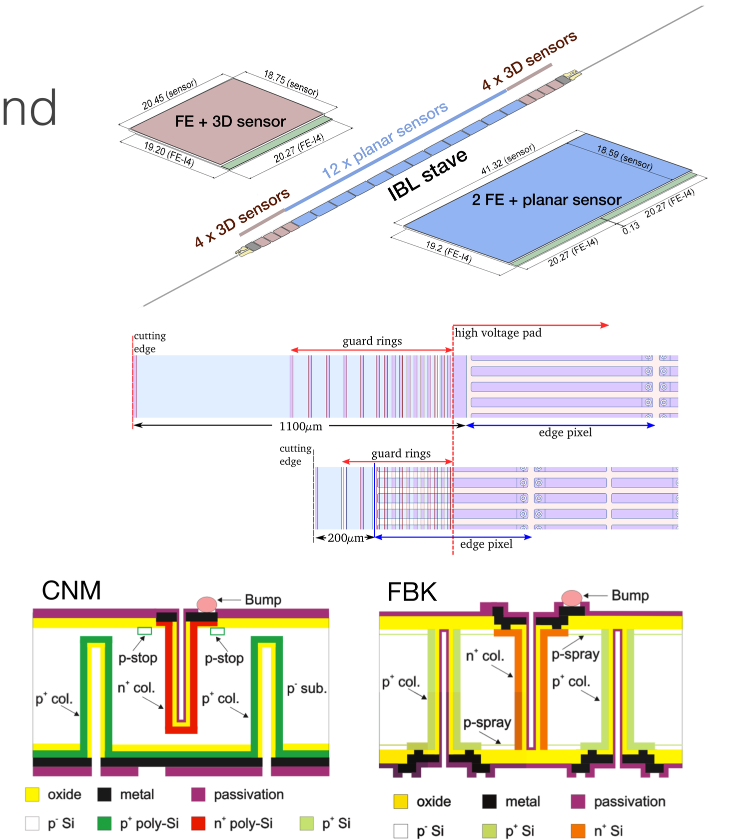
The **ATLAS Pixel detector** is the innermost part of the ATLAS detector. It provides charged particle tracking with high efficiency over a wide angle range. In the LHC **Run2** (2015-), with high beam energy and **high luminosity** the event pileup is increased, leading to high occupancy that can induce readout inefficiencies. In order to preserve tracking performance, a fourth layer of the Pixel detector called **Insertable B-Layer (IBL)** has been inserted between a new beam pipe and the inner Pixel layer (B-layer). The IBL located close to the interaction point at R~3 cm significantly improves the performance of vertexing, **b-quark tagging**, etc. The project provides a test of technologie future upgrade of the pixel detector a high luminosity around $5\times10^{34}$ cm$^{-2}$s

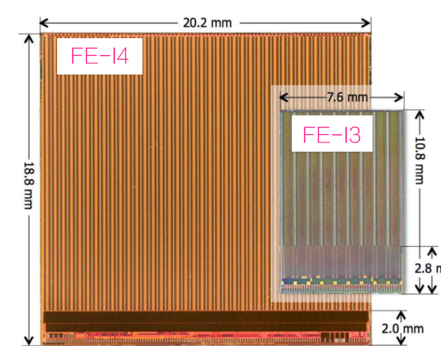



## IBL Sensors & Front-End Chip

The IBL staves are populated in the centre with double-chip **planar** sensor modules and in the forward with single-chip **3D** sensors.

1. Planar sensor by CiS
   - Conservative established technology
   - type: n-in-n
   - thickness: (250 μm →) 200 μm
   - inactive edge: (1100 μm →) 200 μm
2. 3D sensor by CNM & FBK
   - New technology with complex fabrication process
   - type: n-in-p
   - thickness: 230 μm
   - inactive edge: 200 μm

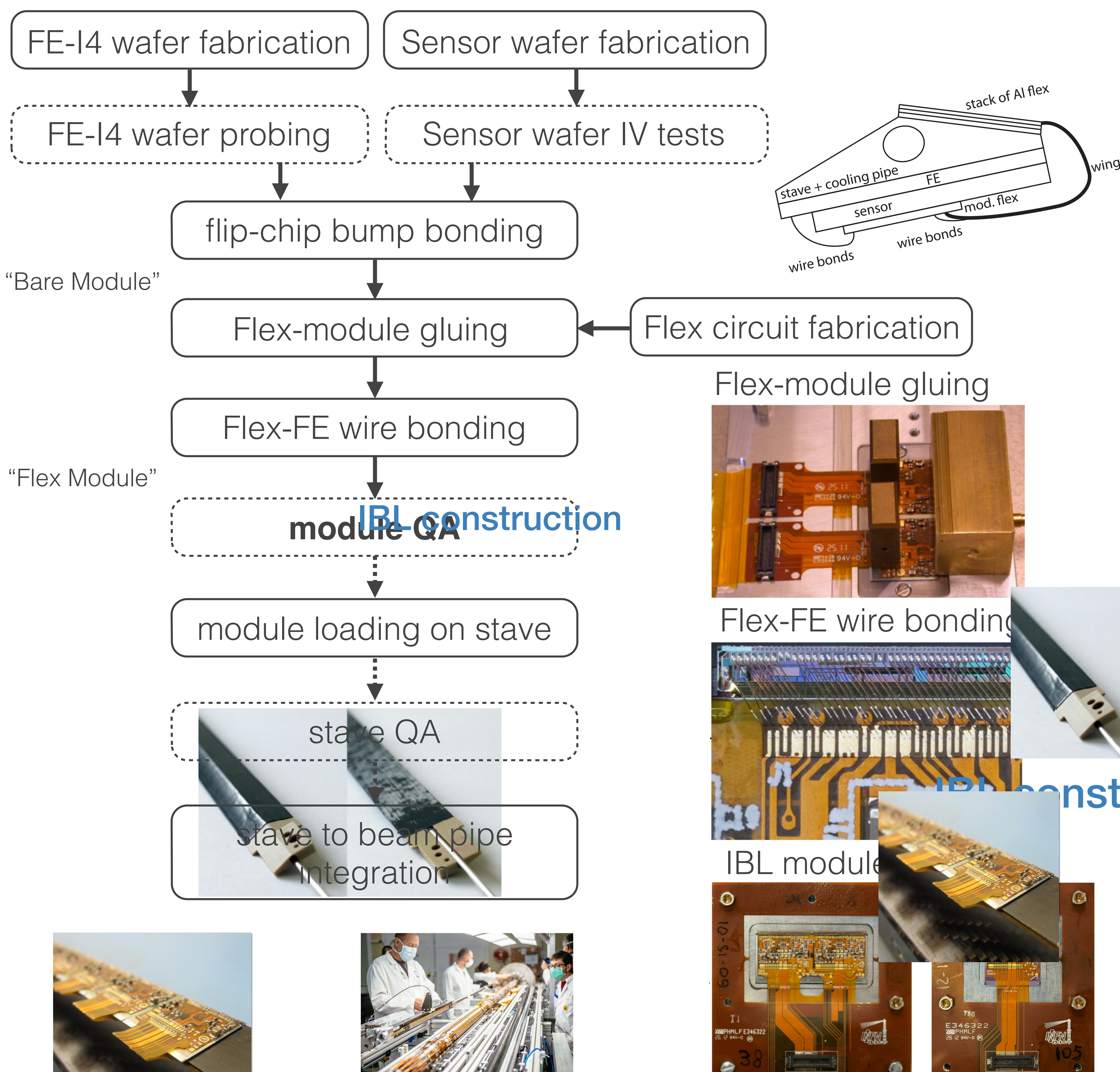



A new front-end chip, **FE-I4**, is connected with a sensor by flip-chip bump bonding.

- Largest FE chip of pixel detector for HEP
- 130 nm CMOS technology
- 26,880 pixels (50 × 250 μm²)
- Active area up to 90%
- Local memory-based architecture

## Flow of the IBL Module Construction

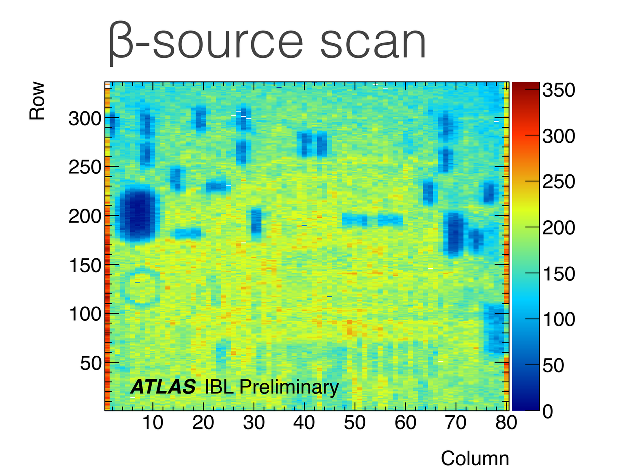



## IBL Module QA

In order to select modules with good performance, a number of modules (~900) were tested and ranked. The QA procedure is divided into several processes. Obviously bad modules are thinned out in the early stage and not tested thereafter for saving time.

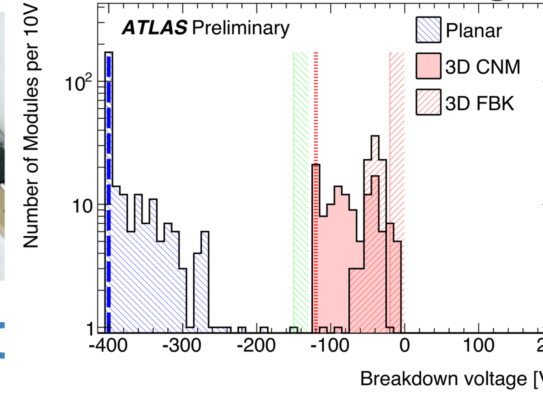
1. Preliminary electrical test after assembly
   - check if wire-bonds properly done
2. Electrical test at ambient temperature
   - IV curve, noise scan, etc
3. Thermal cycling
   - between -40°C and +40°C
4. Complete test and calibration at operation temperature (~ -15°C)
   - electrical test, **β-source scan**

β-source scan



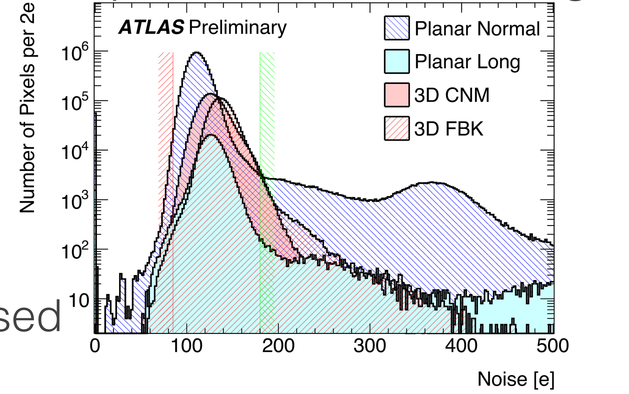

**IBL requirement:**
**< 1% pixel defects per FE**

Breakdown voltage



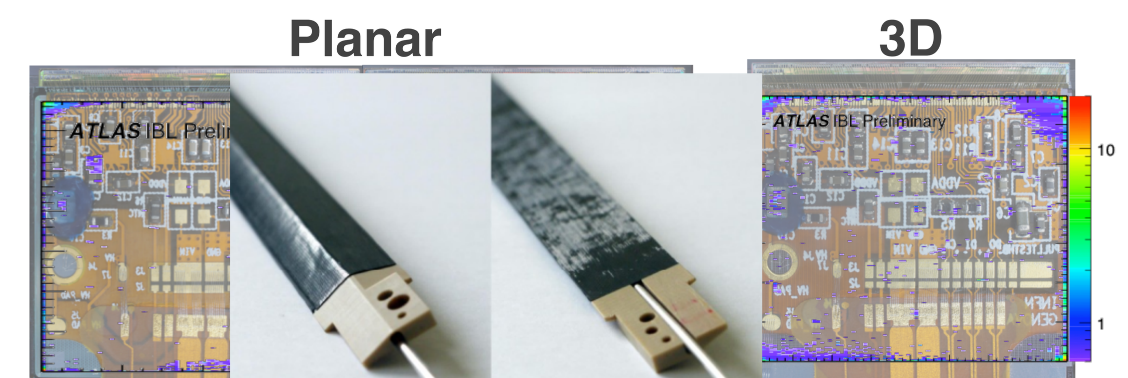

99.5% modules passed

Equivalent Noise Charge




99.8% pixels passed

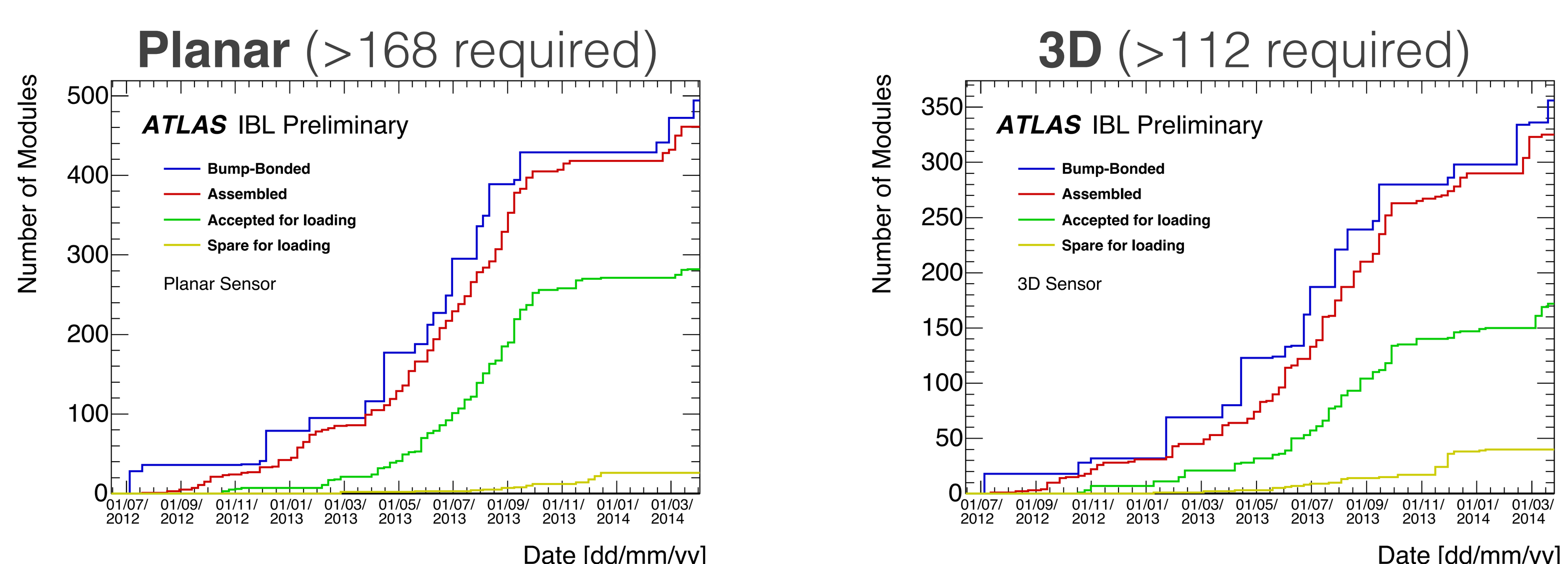
Planar 3D



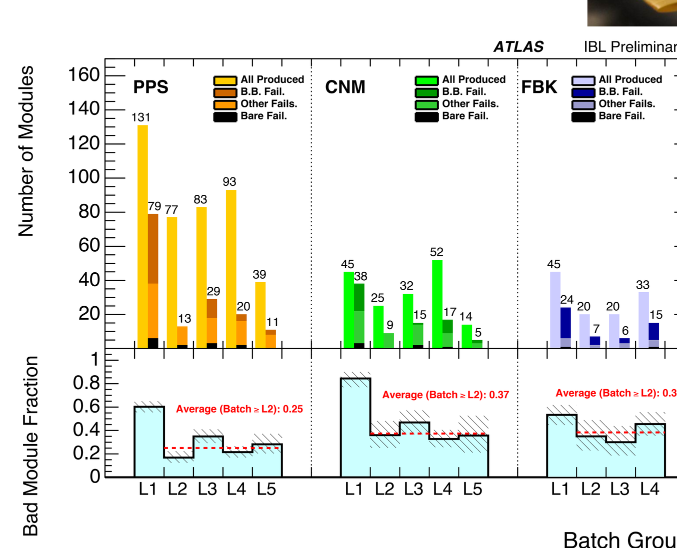

Overlay of the total number of disconnected pixels for planar and 3D sensors loaded onto staves with pictures of double-chip and single-chip modules.

## Trend of the Module Production

**Planar** (>168 required) **3D** (>112 required)




## Conclusion




A good yield of the IBL module production was achieved (**~75% for planar** and **~62% for 3D**). Success in first large scale application of 3D sensor technology and implementation of new large size front-end chip is an important milestone for future upgrade of pixel detectors. The IBL has been inserted into the core of the ATLAS detector in May 2014.

International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL2014), 1–5 September 2014, Niagara Falls, Canada