Pixel Module Production and Qualification for the Phase I upgrade of CMS

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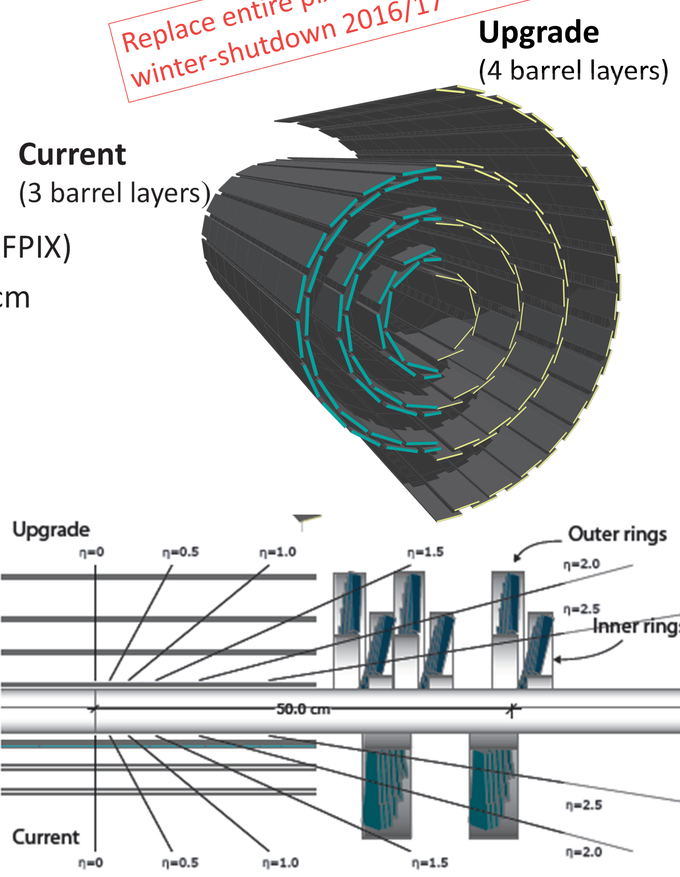
CMS Pixel Upgrade for Phase I

- Present Pixel Tracker designed for maximum $L_{inst} = 1 \times 10^{34}$ cm^{-2} s^{-1}
  → Expected in 2015!
- LHC luminosity after long shutdown 2: $L_{inst} = 2 \times 10^{34}$ cm^{-2} s^{-1}
  → Likely before 2018

The Upgrades

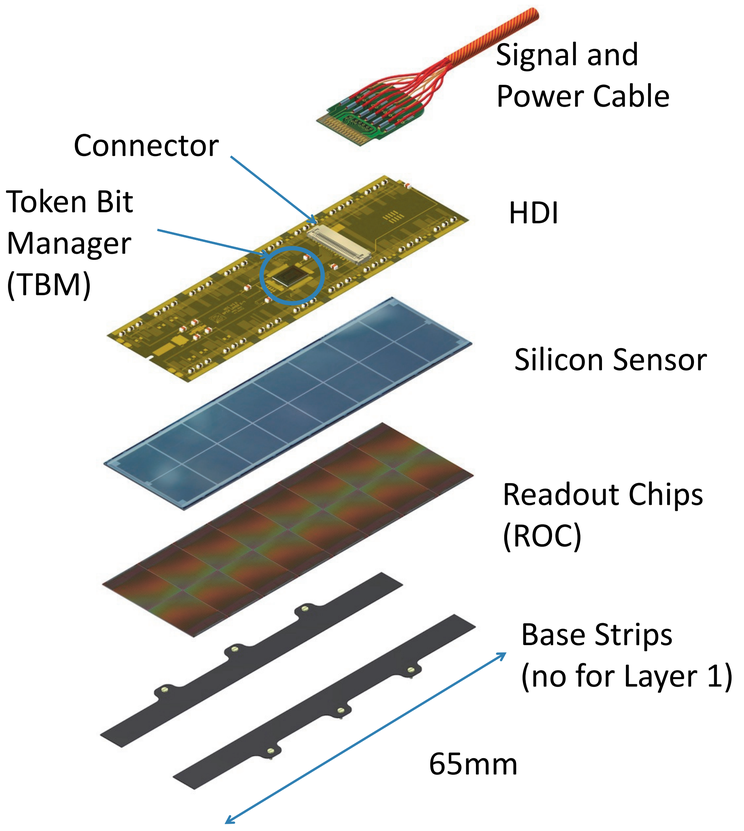
- One layer more with respect to the current detector (BPIX and FPIX)
  → Additional barrel layer with minimal inner-most radius: 2.9 cm
  → BPIX: 1184 modules, 79 Mpixels (1.6 x current BPIX)
  → FPIX: 672 modules, 45 Mpixels (2.5 x current FPIX)
  → Improved efficiency and resolution
- New ROC developed with incrased buffers to reduce data loss and digital output to gain in communication speed
- Less material budget:
  - Ultra-light support structure (carbon fibre)
  - Electronic services partially moved outside the tracking volume
  - Powering scheme optimized (DC-DC converters)
  - CO_2 cooling (less cooling material than present C_6F_{14})

Replace entire pixel detector in winter-shutdown 2016/17



Pixel Detector Module

A module is the smallest unit of the CMS pixel detector



Silicon Sensor

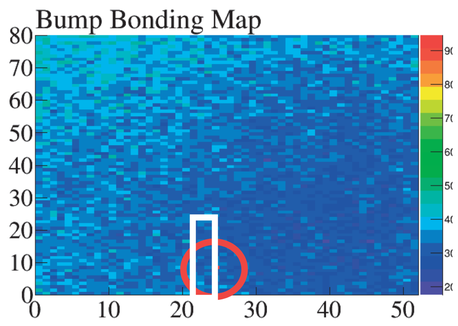
- N^+-n sensor. Pixel size: 100 x 150 µm. Thickness: 285 µm.
  → Efficiency fully sufficient at the expected radiation level of 1.5 x 10 ^{15} n_{eq}/cm^2 (250 fb^{-1} @ R=3cm)
- Sensor vendor (CIS) performs IV measurements on each wafer

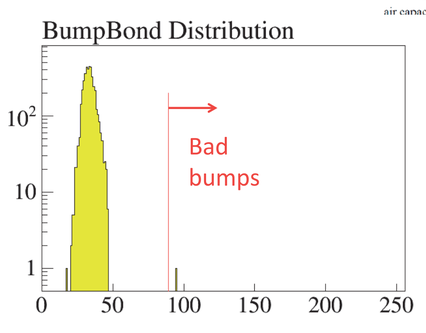
Bare Module Test

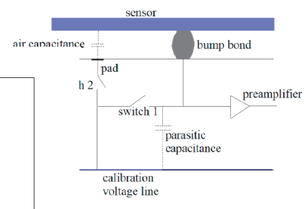
- 1 Sensor layer and 16 ROCs connected via Bump Bonding in two rows.

IV performance is repeated at production centers
→ Grading criteria: **$I_{150V} / I_{100V} < 2$; $I_{150V} < 2$ µA**

- Test of Bump Bonding quality:
  → Internal pulses (*CalS*) injected capacitively into Silicon.
  → The response efficiency is measured for decreasing VthrComp (increasing threshold) to take the threshold at which efficiency reaches 50%
  → Cut at reasonable value to distinguish reliably between good and defective bumps

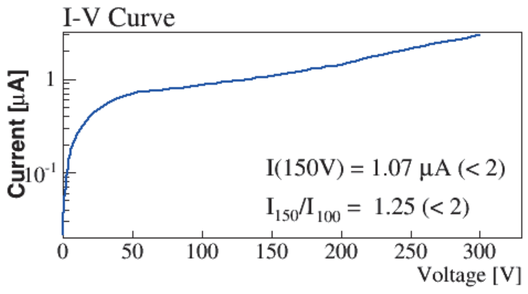






Readout Chip (ROC)

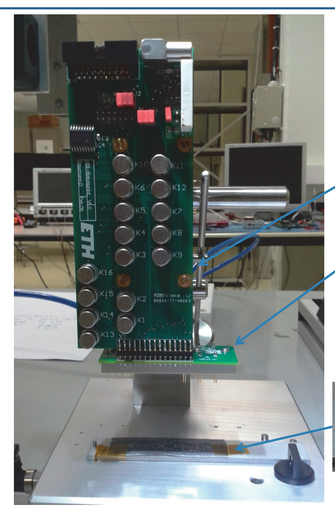
- Double column readout (Dedicate chip designed for L1 in progress)
- Larger trigger latency buffers and additional readout buffer to reduce data loss
- 160 MHz digital readout to increase bandwidth



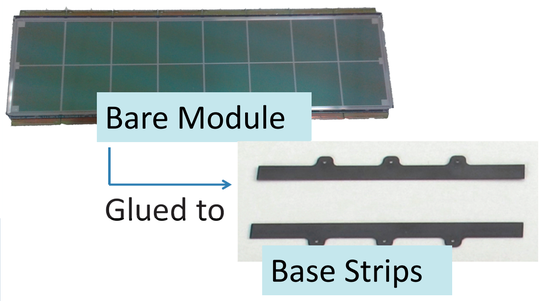
- ROCs will be produced by IBM
- Each wafer will be tested at PSI (248 ROCs per wafer)
- Wafers will be sent to external company for further processing:
  → bump deposition, wafer thinning and dicing

HDI & TBM Test

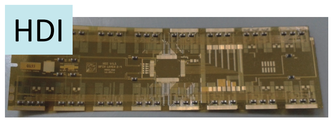
- ROCs are connected and powered through a Hight Density Interconnect (HDI). They will be produced and tested by High Tec MC AG
- Token Bit Manager (TBM) controls the readout of the ROCs and distributes clock, trigger and resets. They will be produced by IBM and will be tested on wafer.
- Finally both components are tested with a needle probe card



Full Module Assembly

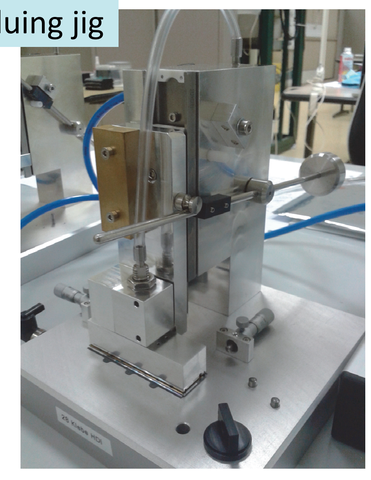


TBM Glued and wire bond to

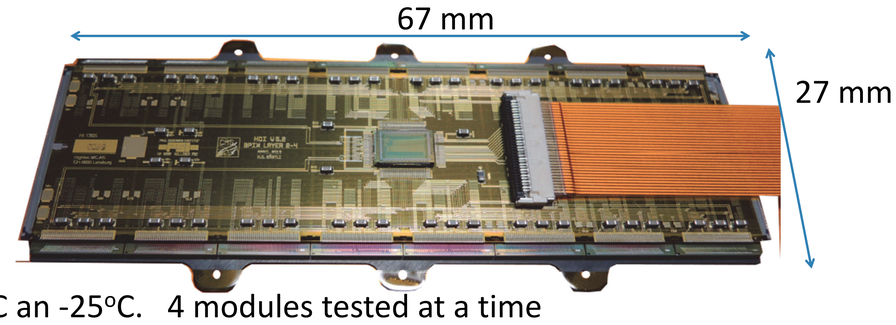


- Glue HDI to Bare Module at gluing station
- Wire bond ROC pads to HDI

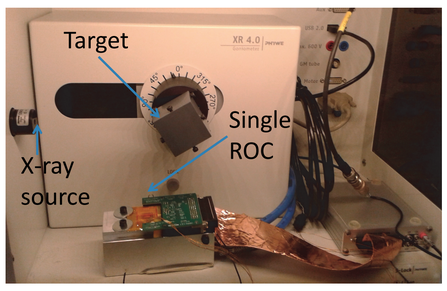
Gluing jig

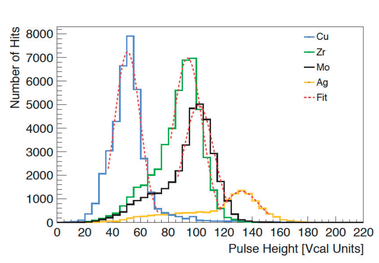


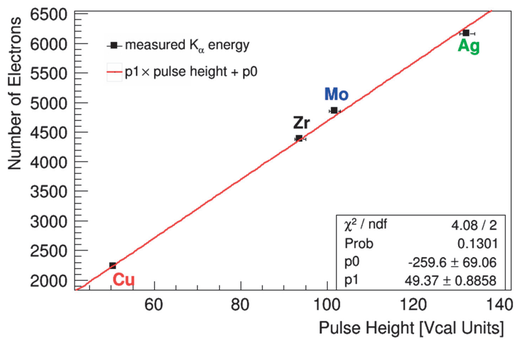
Full Module Ready!! (to be tested)



1. **Cold Box Test**
   - 10 Thermal cycles between +17ºC an -25ºC. 4 modules tested at a time
   - Full Test and IV at +17ºC an -20ºC (it includes: To determine defective pixels, bump bonds and trim bits, noise measurement, trim all ROC to a certain threshold, PH calibration and IV).
2. Vcal – energy calibration with **X-rays**







- To test the entire module readout chain, and for setting threshold, an internal calibration pulse (Vcal) is used.
- Absolute energy calibration is performed using well defined X-ray fluorescence lines from different target materials.

→ **Calibration Line: 50 e$^-$ per Vcal** (chip psi46dig 2.1)

Plots from RWTH Aachen University

MODULE PRODUCTION PLAN FOR CENTERS:

- BPIX Layer 1+2 (320 modules): Swiss consortium (PSI, ETH)
- BPIX one-half Layer 3 (176 modules): CERN, NTU and HIP consortium
- BPIX one-half Layer 3 (176 modules): INFN consortium
- BPIX Layer 4 (512 modules): German consortium (Desy, KIT, RWTH, Hamburg Univ.)
- FPIX: US consortium