VeloPix: The Pixel ASIC for the LHCb VELO Upgrade

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On behalf of the VeloPix design team

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Outline

- Introduction
- VeloPix vs Timepix3
- Readout architecture
- GWT serializer
- Summary

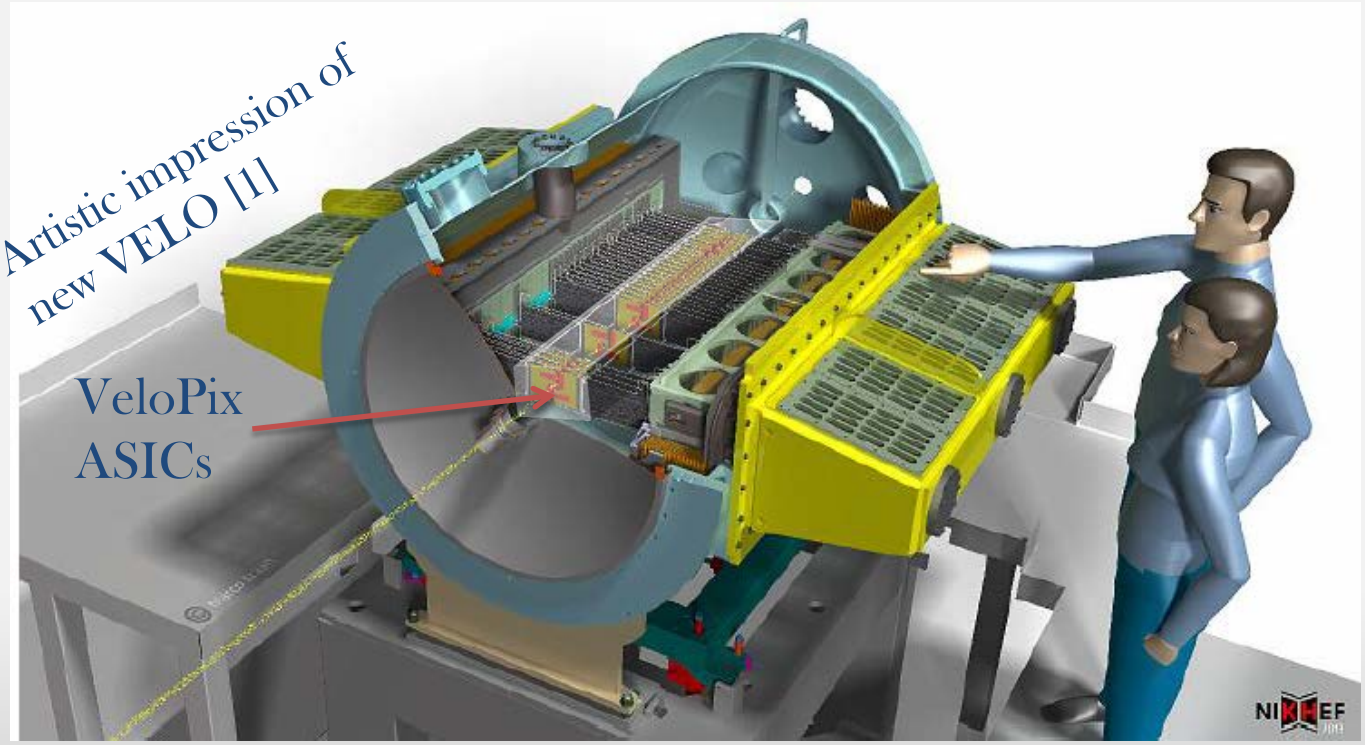
Introduction

- VeloPix: Hybrid pixel detector (HPD) Readout ASIC for the LHCb VELO upgrade
- The ASIC reads out all bunch crossings at 40 MHz

<u>The VELO upgrade:</u>

- Approx. 2.85 Tbit/s
- 26 module pairs
- 624 ASICs
- 41 Mpixels*

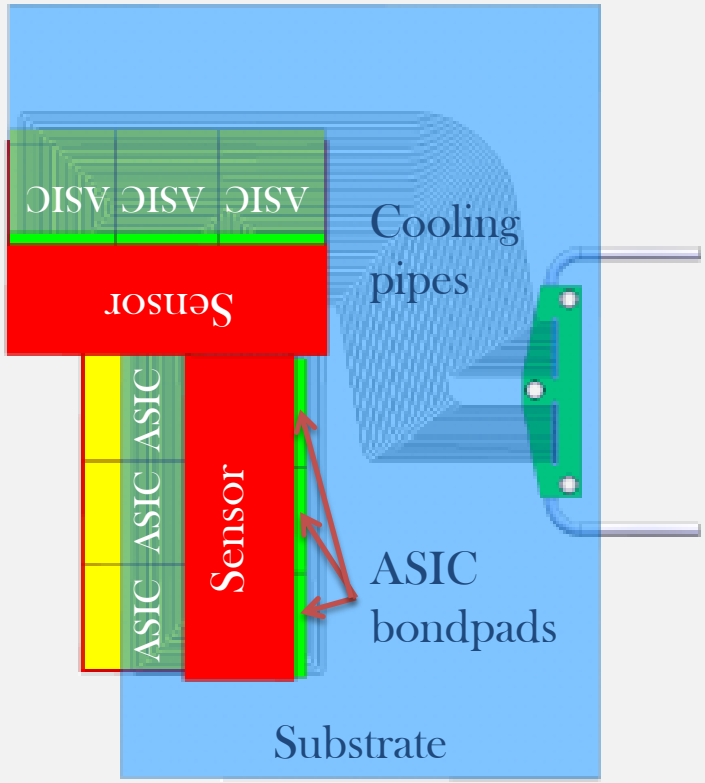
See talk by Eddy Jans: "The VELO Pixel Upgrade"



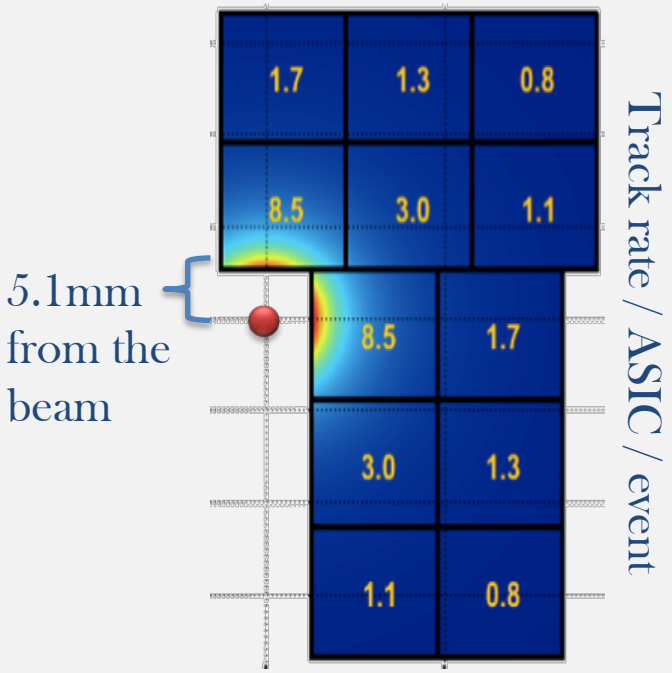
*Nokia Lumia 1020 (2013) also has 41 MP camera

VeloPix ASIC module (12 ASICs)

Module of 12 VeloPix ASICs [1]:



Track rates for module [2]:

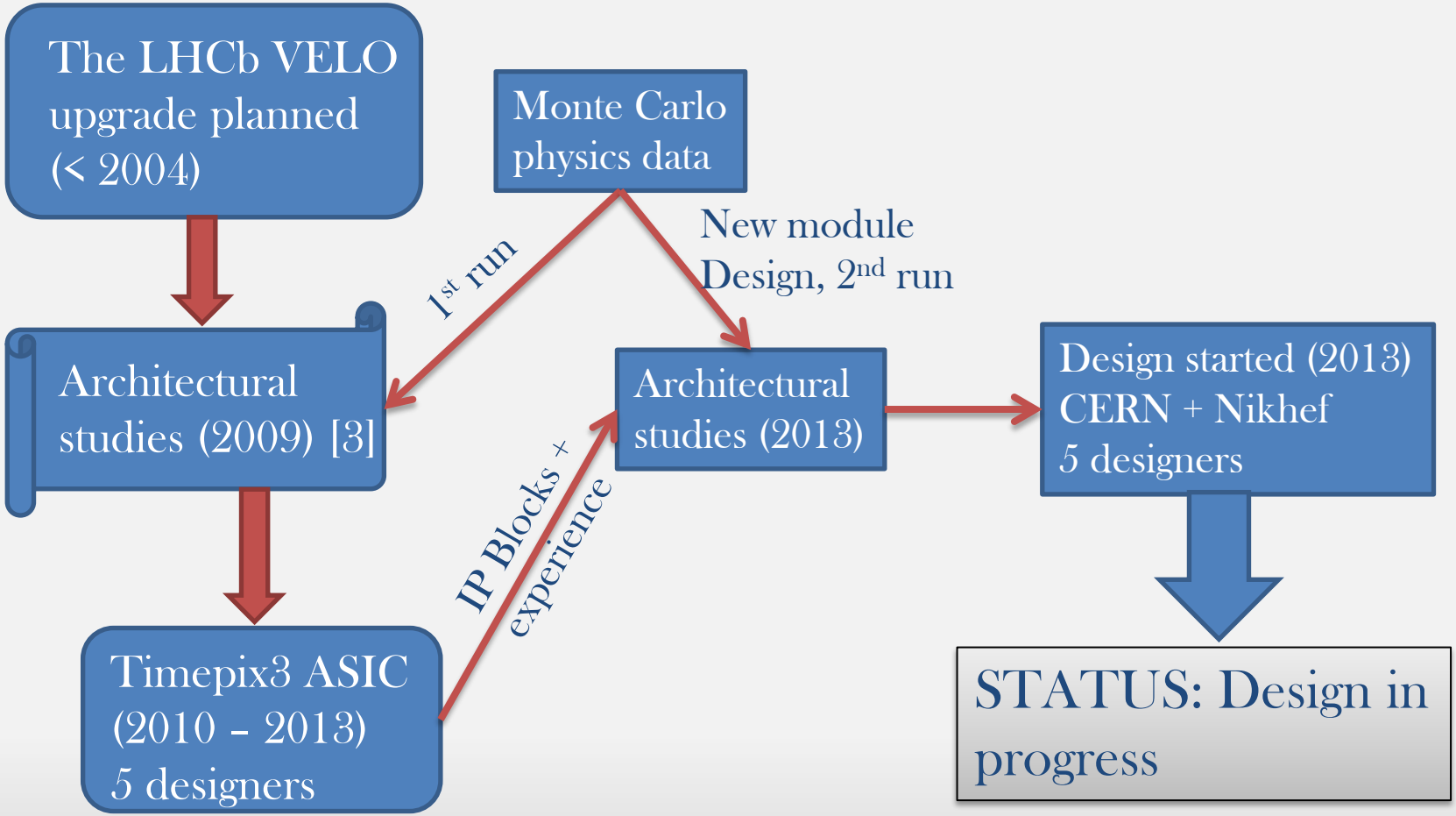


Highly non-uniform radiation dose:
8×10^{15} to 2×10^{14} n_{eq}/cm^2

Peak rates:
Hottest chip 15.1 Gbits/s
hottest module: 61.2 Gbits/s

See Oscar Augusto's talk about the module cooling:
"Evaporative CO2 Microchannel
Cooling for the LHCb VELO Pixel Upgrade."

VeloPix project timeline



VeloPix ASIC specifications

Feature	VeloPix	Timepix3 [2]
Readout type	Continuous, trigger-less, binary	Continuous, trigger-less, ToT
Timing resolution/range	25 ns, 9 bits	1.5625 ns, 18 bits
Power consumption	< 1.5 W cm^{-2}	< 1.0 W cm^{-2}
Pixel matrix, pixel size	256 x 256, 55 um x 55 um	256 x 256, 55 um x 55 um
Radiation hardness	400 Mrad, SEU tolerant	-
Peak hit rate	900 Mhits/s/ASIC 50 khits/s/pixel	80 Mhits/s/ASIC 1.2 khits/s/pixel
Sensor type	Planar silicon, e- collection	Various, e- and h+ collection
Max. data rate	20.48 Gbps	5.12 Gbps
Technology	130 nm CMOS	130 nm CMOS

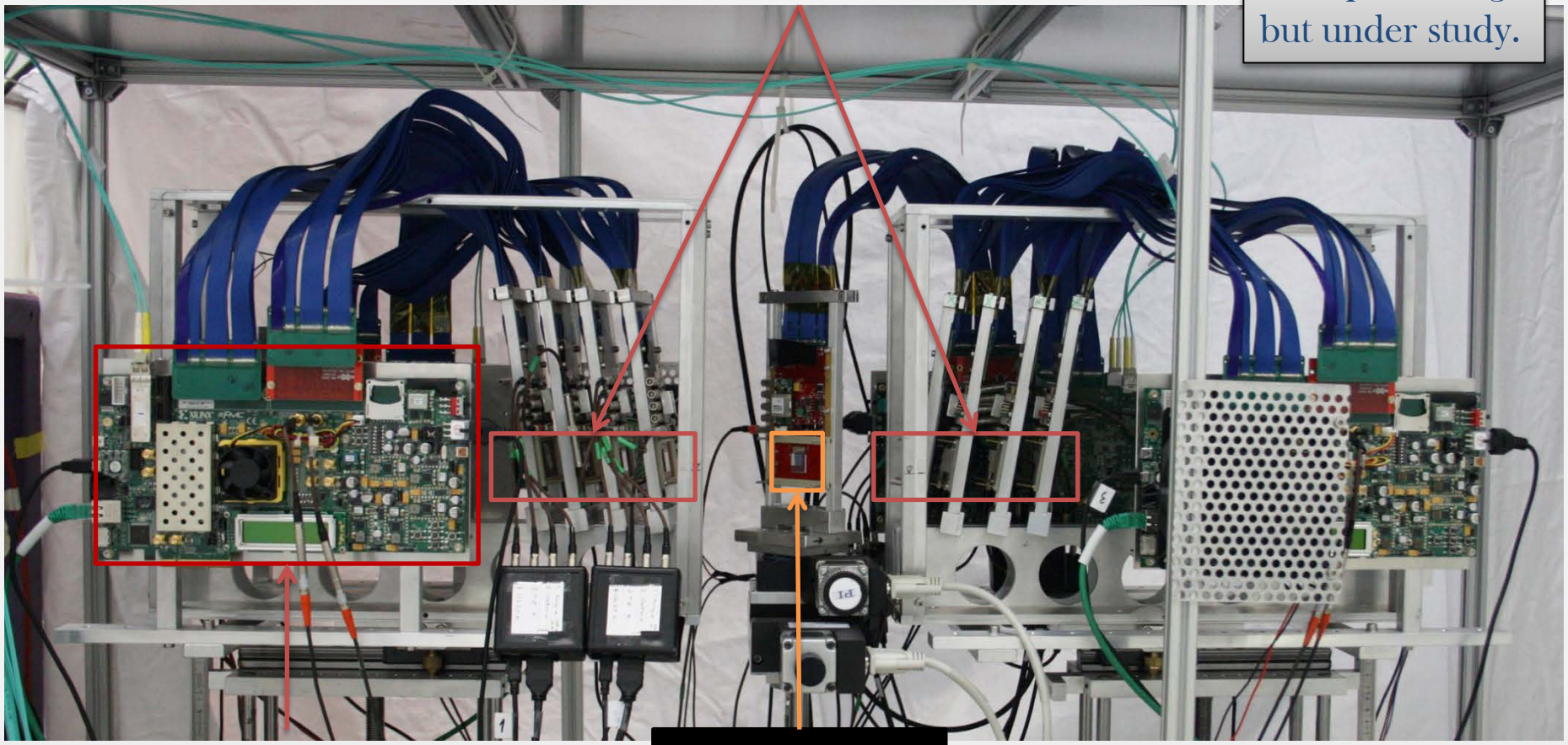
> x 10

x 4

Timepix3 first testbeam

8x Timepix3 telescope

Data promising, but under study.



SPIDR readout

Timepix3 DUT

Mechanics: CERN

The LHCb VELO upgrade testbeam effort.

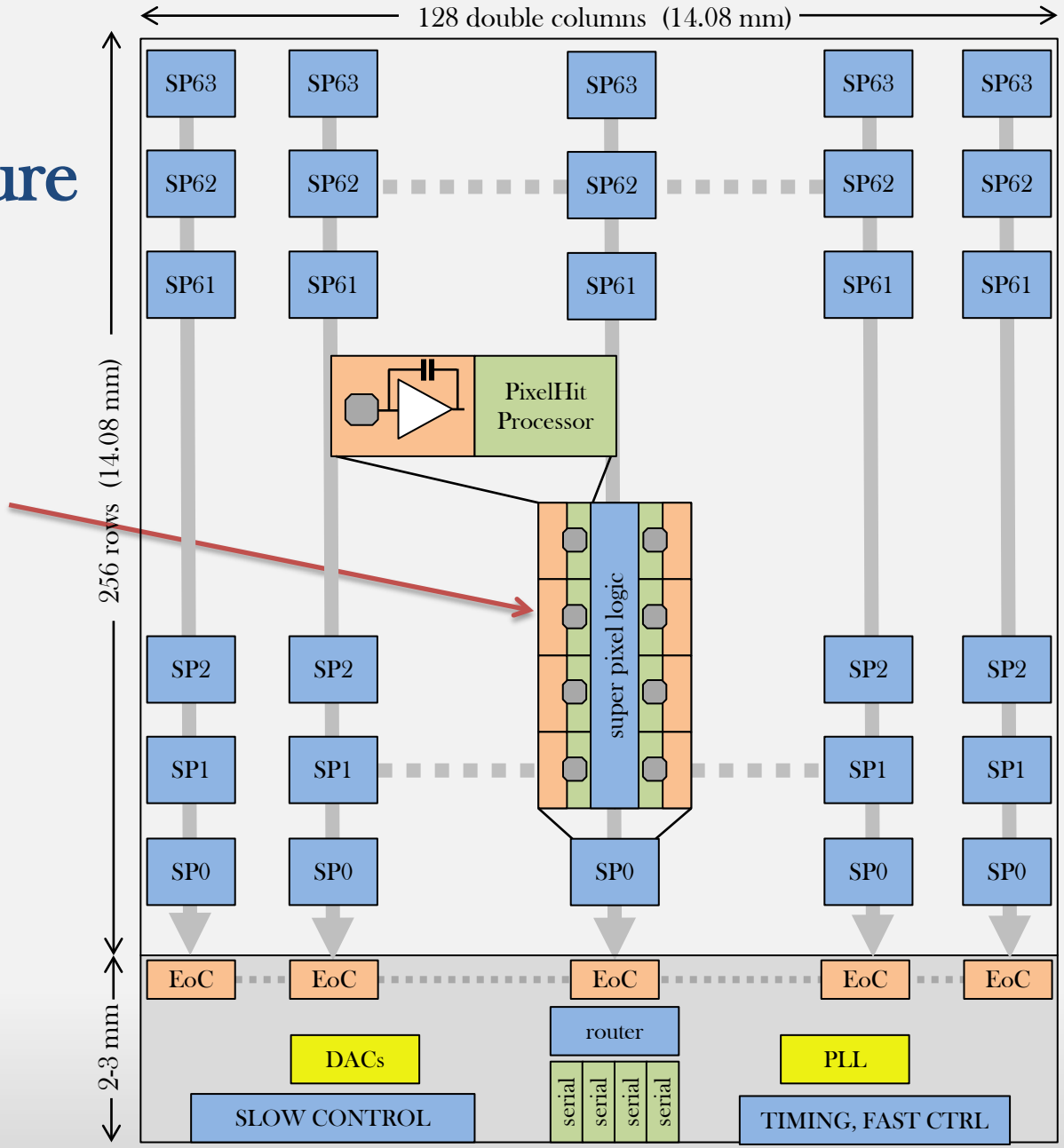
See [4] for more about Timepix3.

VELOPIX ARCHITECTURE

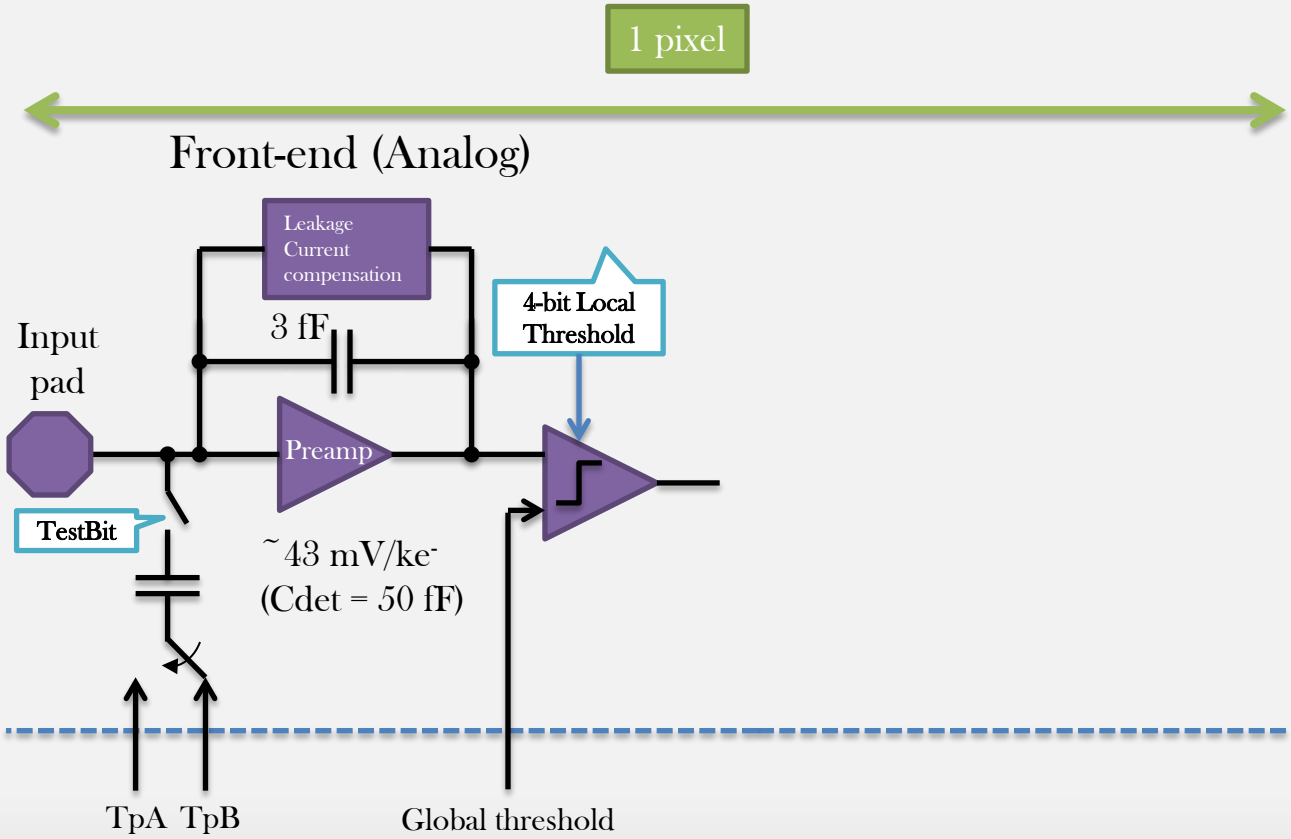
VeloPix Architecture

Super pixel:

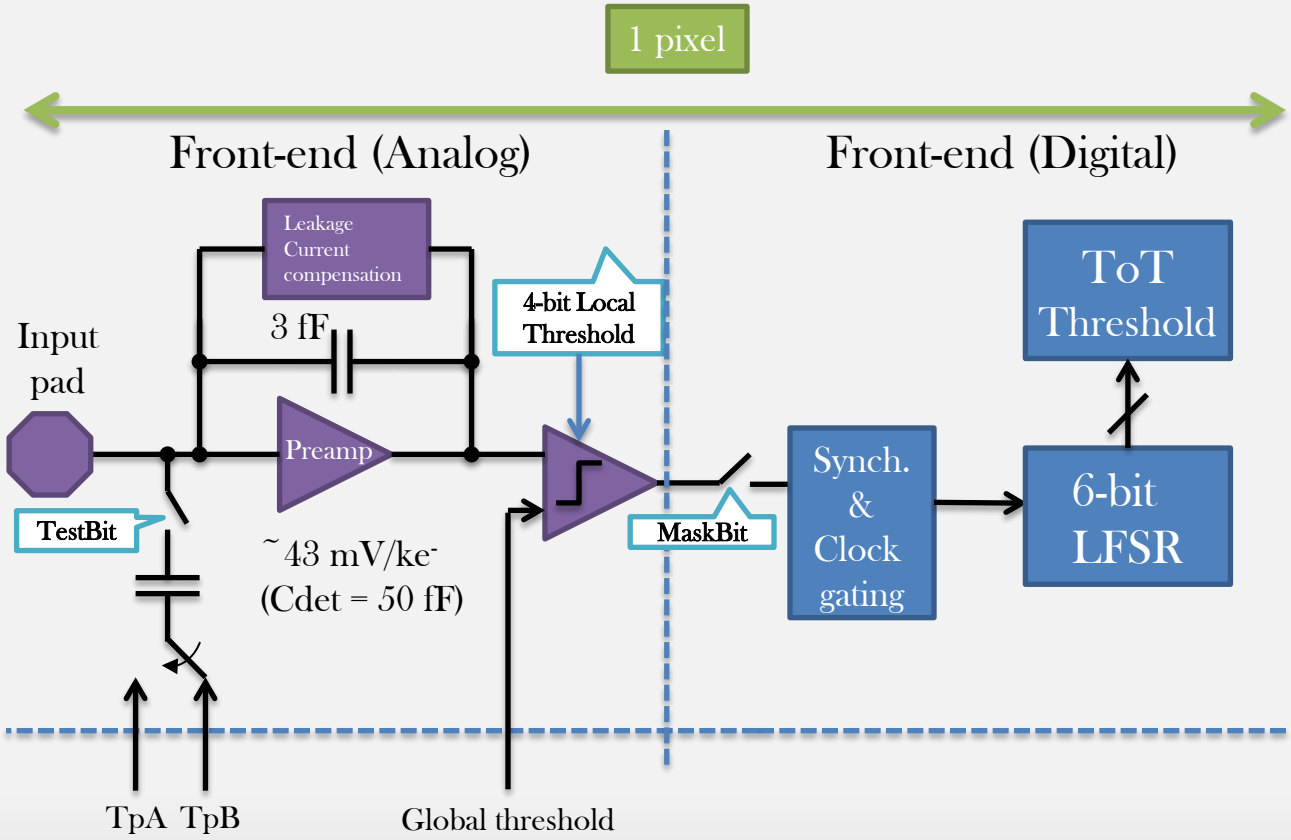
- 2x4 pixels to reduce the data rates
- 30% reduction vs single-pixel



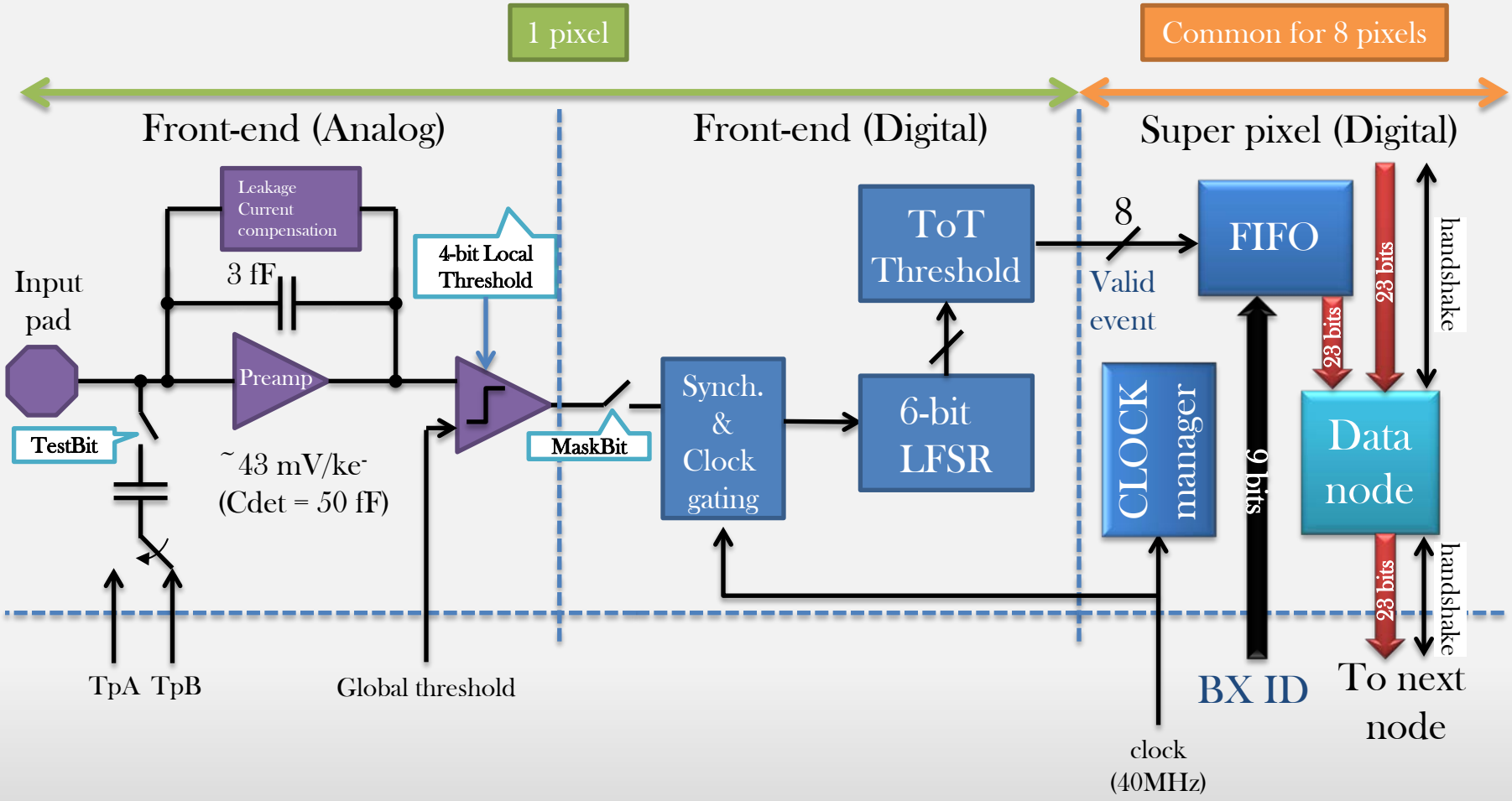
VeloPix Pixel Schematic 1/3



VeloPix Pixel Schematic 2/3

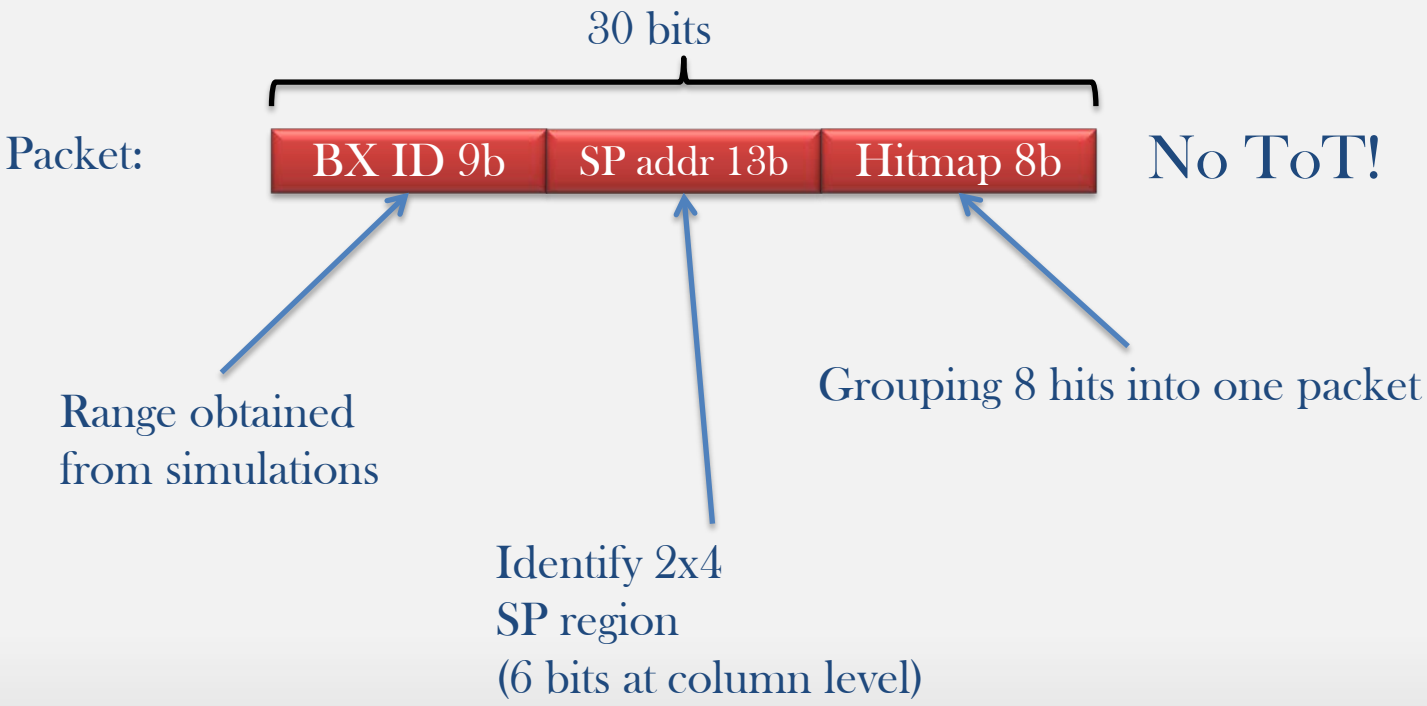


VeloPix Pixel Schematic 3/3



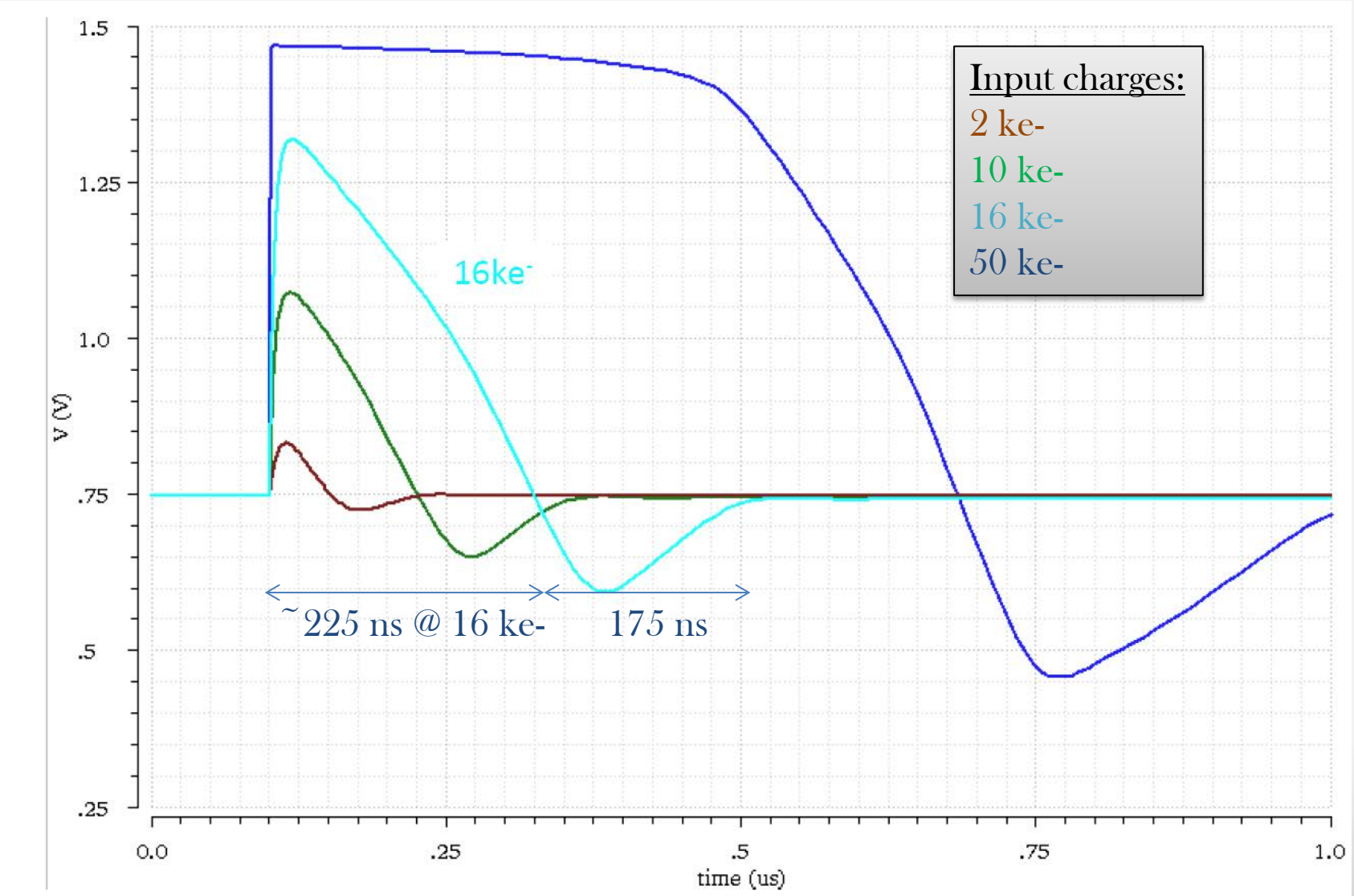
Packet format

30% data reduction from sharing the BX ID and super pixel address among multiple pixels.



BX ID = bunch crossing ID/ time stamp/time-of-arrival

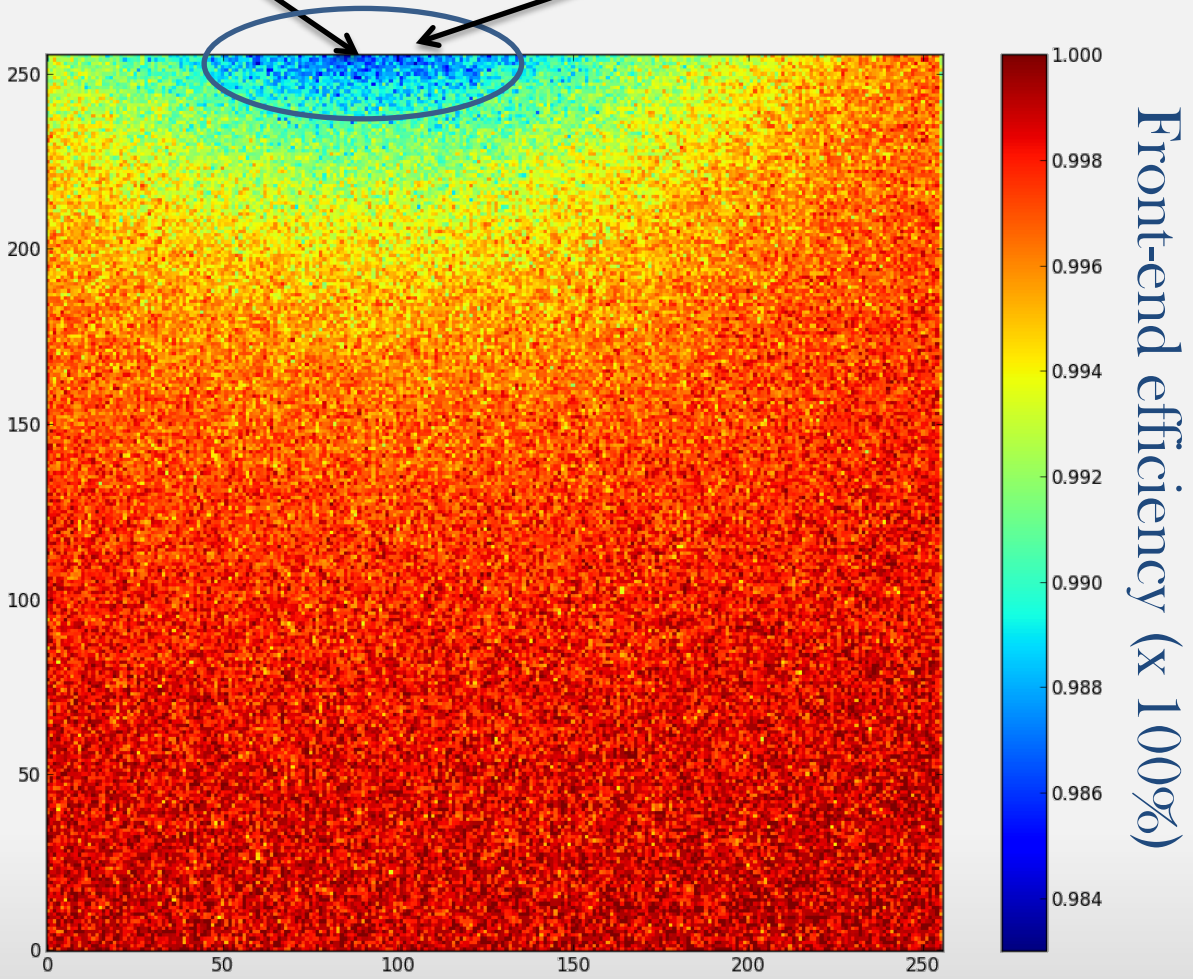
Analog front-end amplifier response



Analog front-end pile-up

Up to 1.6% losses

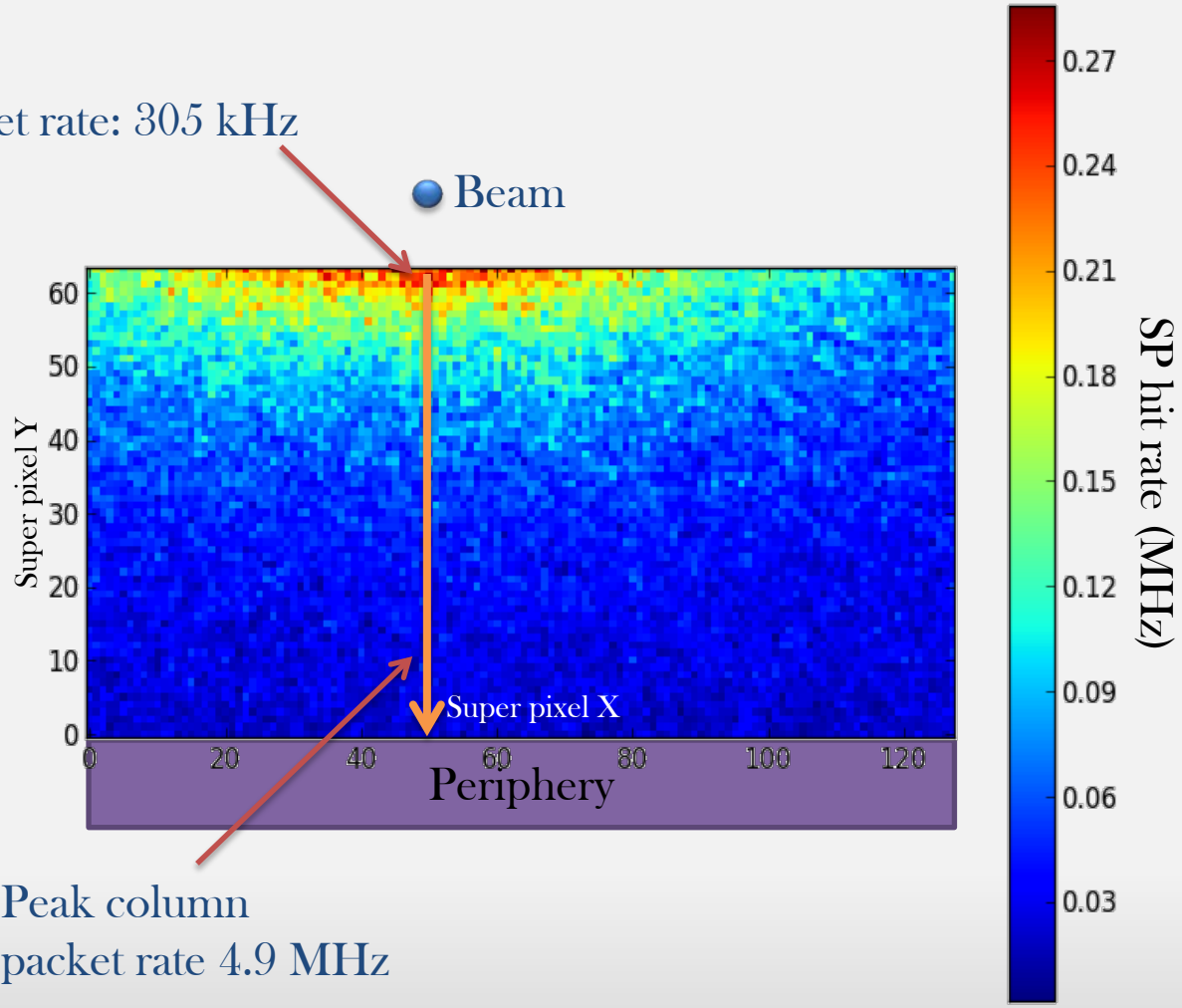
Rates up to 50 kHz per pixel



Packet rates per super pixel

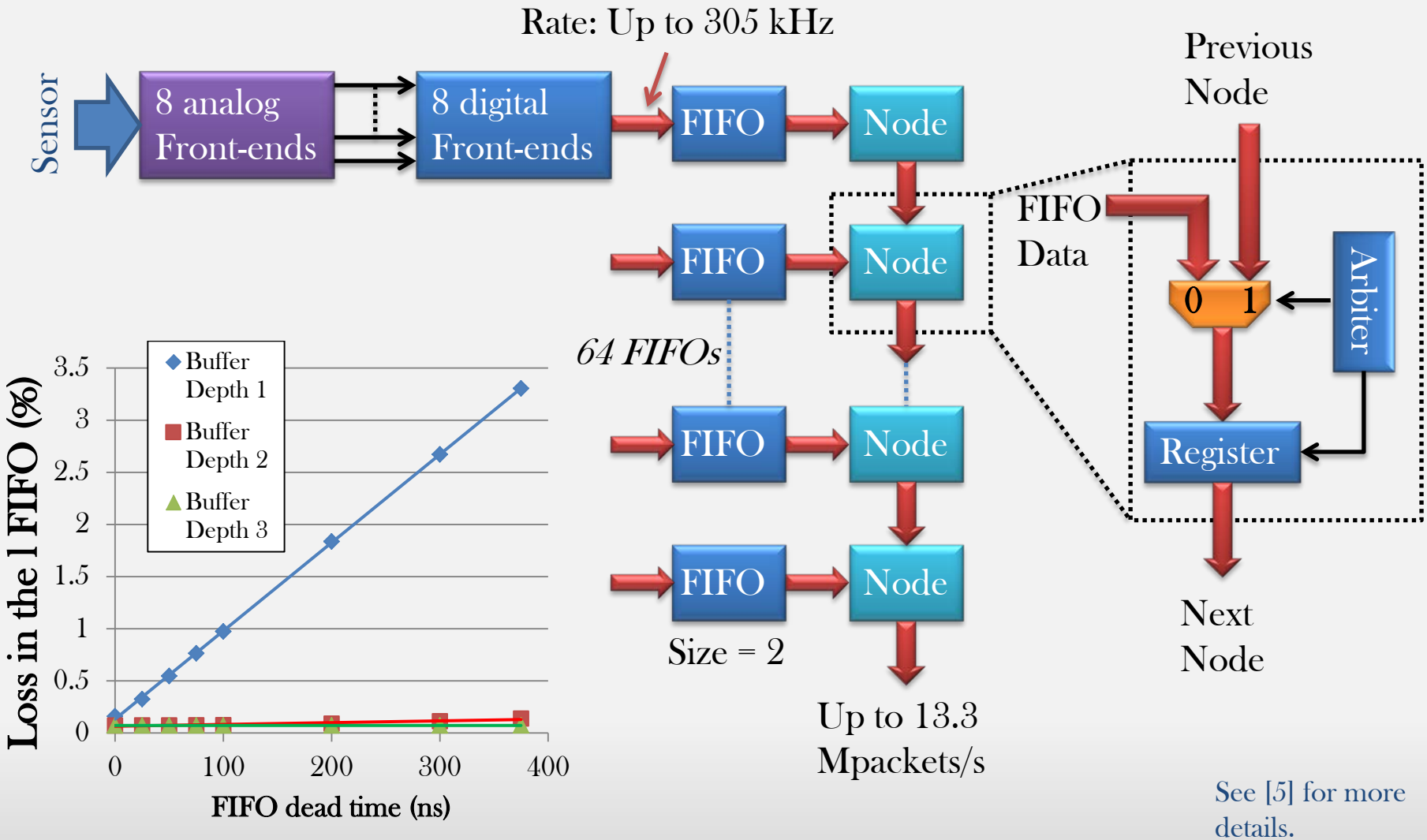
Peak SP packet rate: 305 kHz

Packet rate IS NOT equal to pixel hit rate (1 packet = ~1.66 hits)



Peak column packet rate 4.9 MHz

Double column architecture

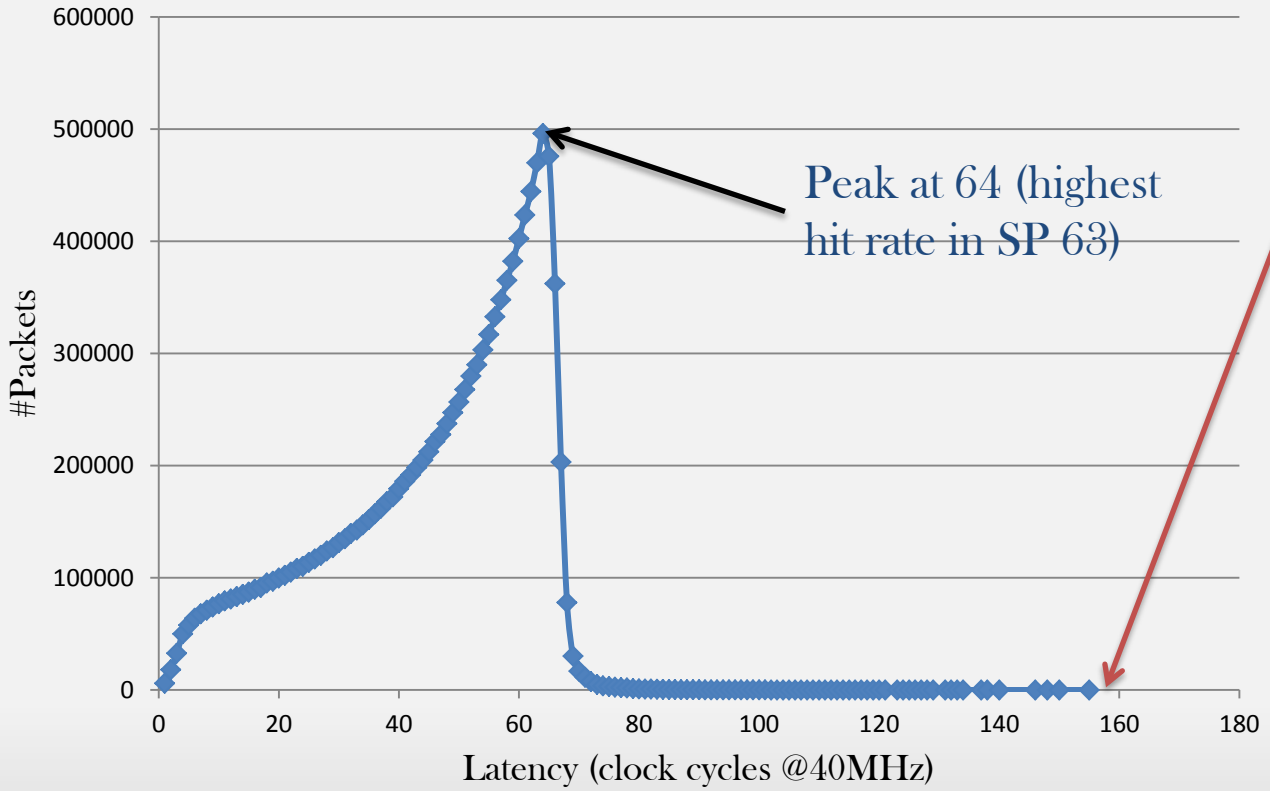


See [5] for more details.

Simulation: Latency & BX ID length

Trigger-less architecture:

Latency must be < BX ID range. Otherwise ambiguities in BX identification.

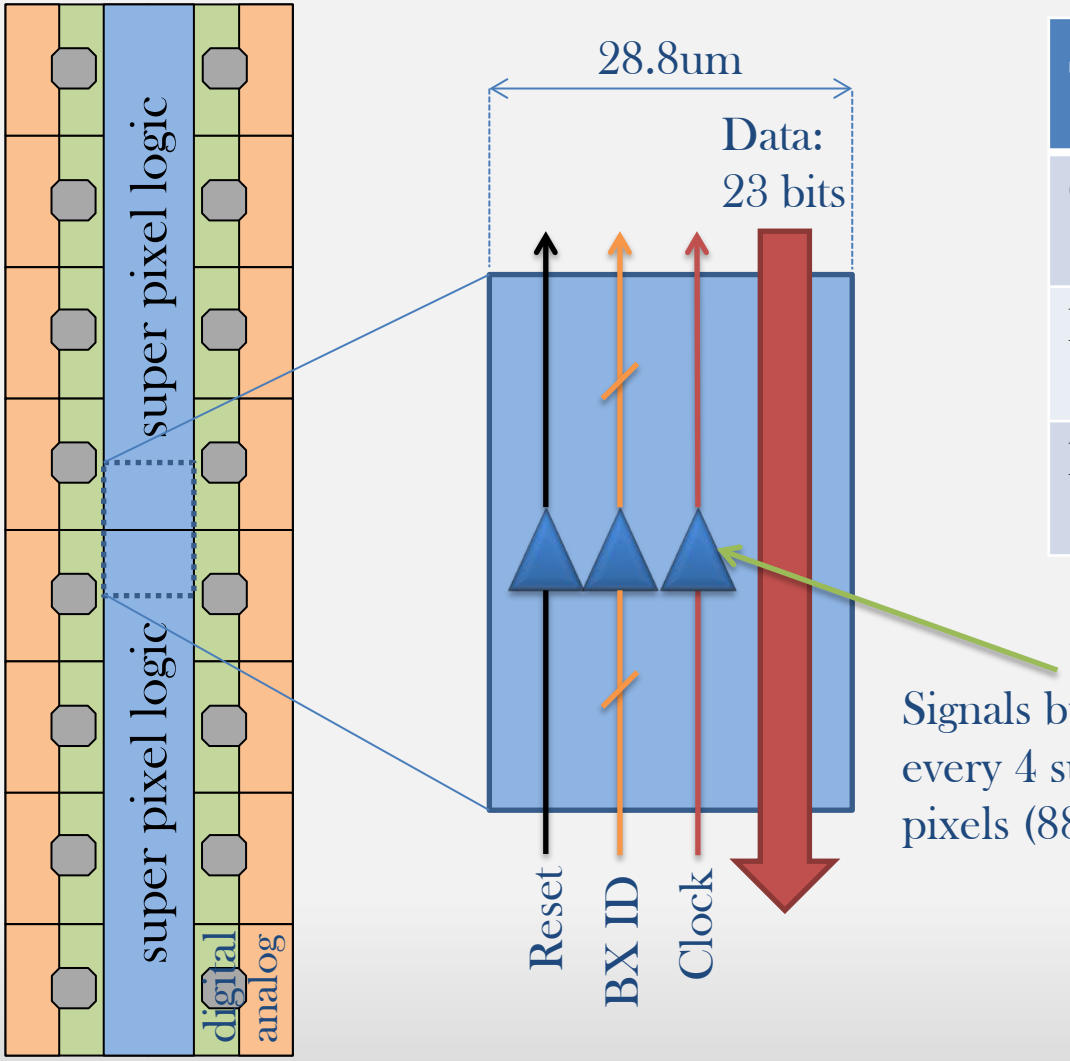


9-bit BX ID (512 clocks) sufficient!

Simulation results:
Efficiency: 99.99%*
Hit rate: 840 Mhits/s
Packet rate: 505 M/s
Data rate: 16.2 Gbps
Hits per packet: 1.66

*No analog pile-up included.

Double column floorplan



Signal	Skew (ps) *	Power (mw) *
Clock	1670 / 1870	0.476
Reset	7130 / 8540	N/A
BX ID (9 bits)	8110 / 9950	0.273

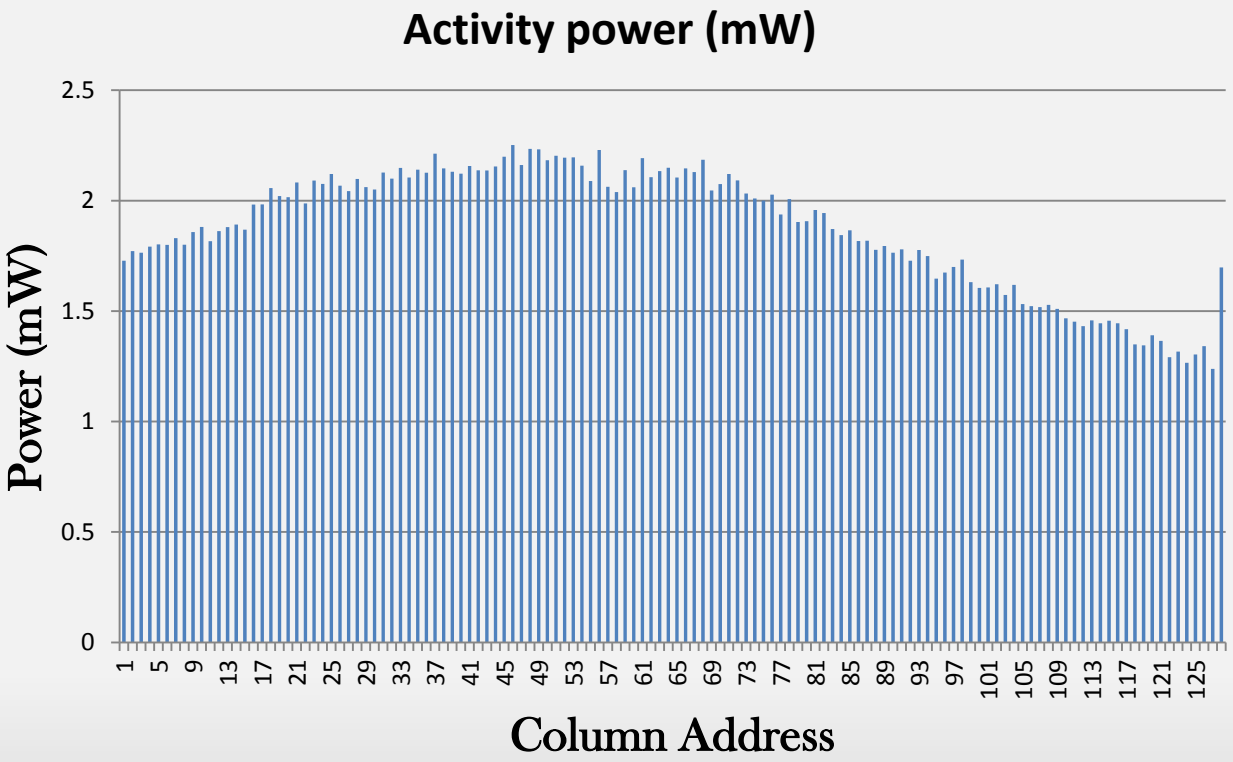
x 128

< 100mW / chip

* slow corner SS/1.4V/125C
* fast corner FF/1.6V/-55C

Digital power (128 columns)

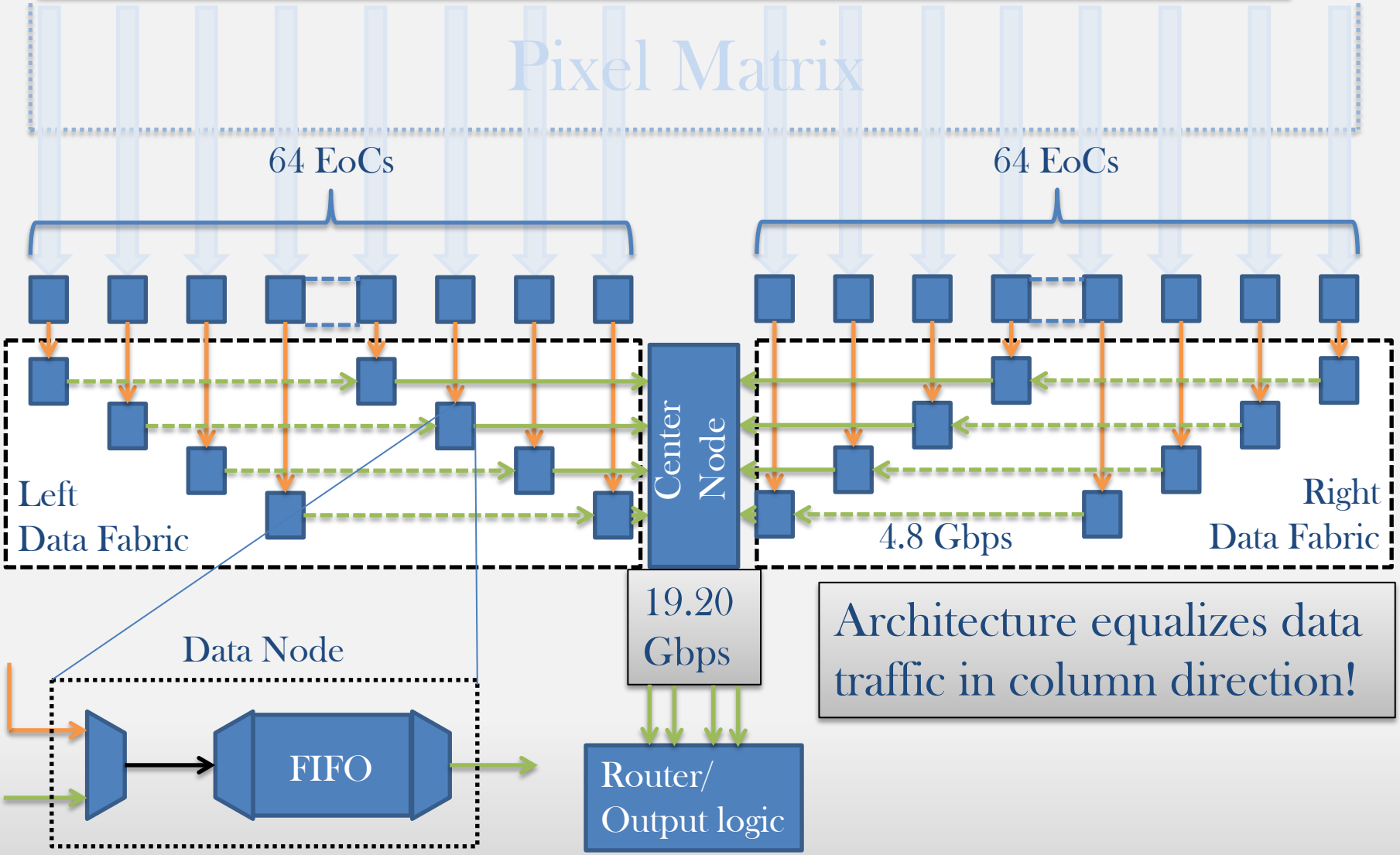
For the hottest column, rate 5 MHz, power 3.3mW (2.25mW active + 1.05 mW standby)
$\Rightarrow$ P(column$_X$) = rate$_X$/5.0MHz * 2.25mW + P(standby$_X$)



Power
Activity: 240 mW
Standby: 120 mW
Clock/BX ID: 100mW
Total: 460 mW*

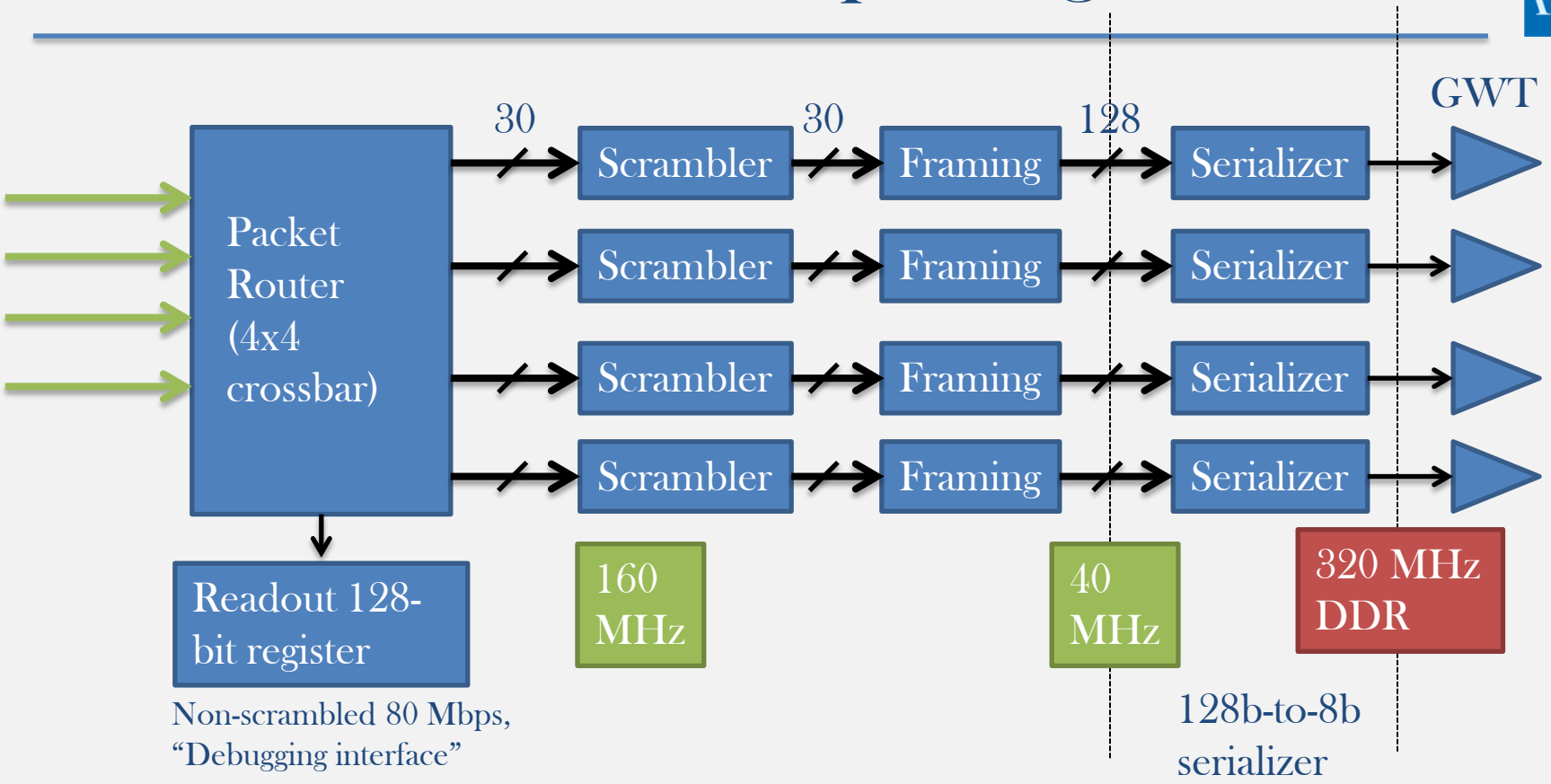
*Not included:
-pixels (analog+digital)
-periphery

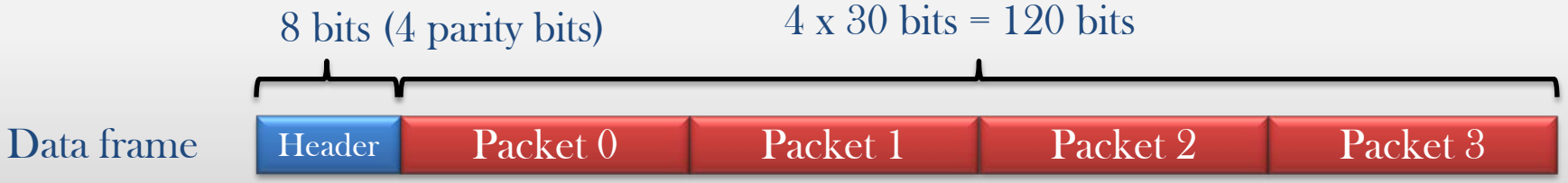
End-of-Column (EoC) data fabric



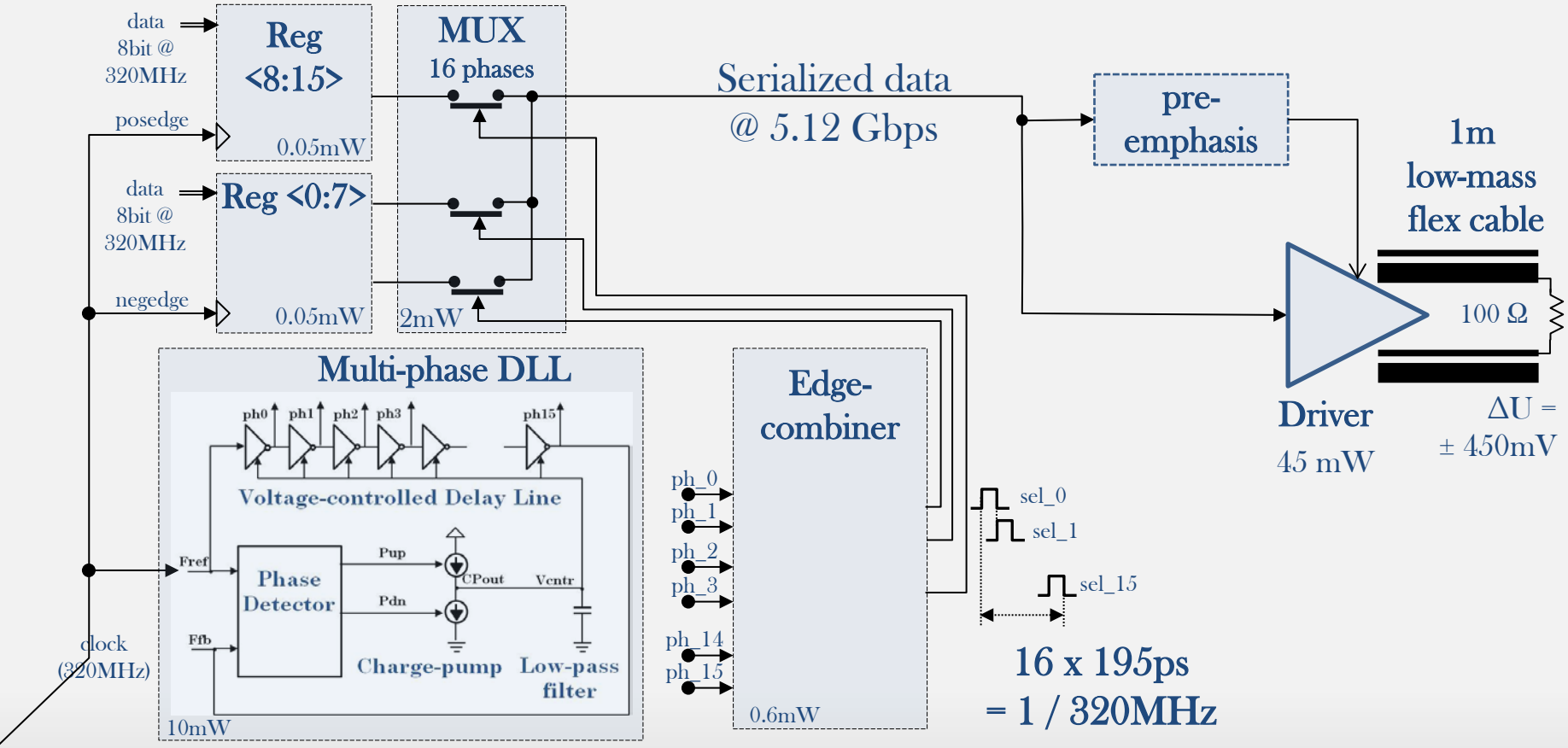
Architecture equalizes data traffic in column direction!

Router/Output logic



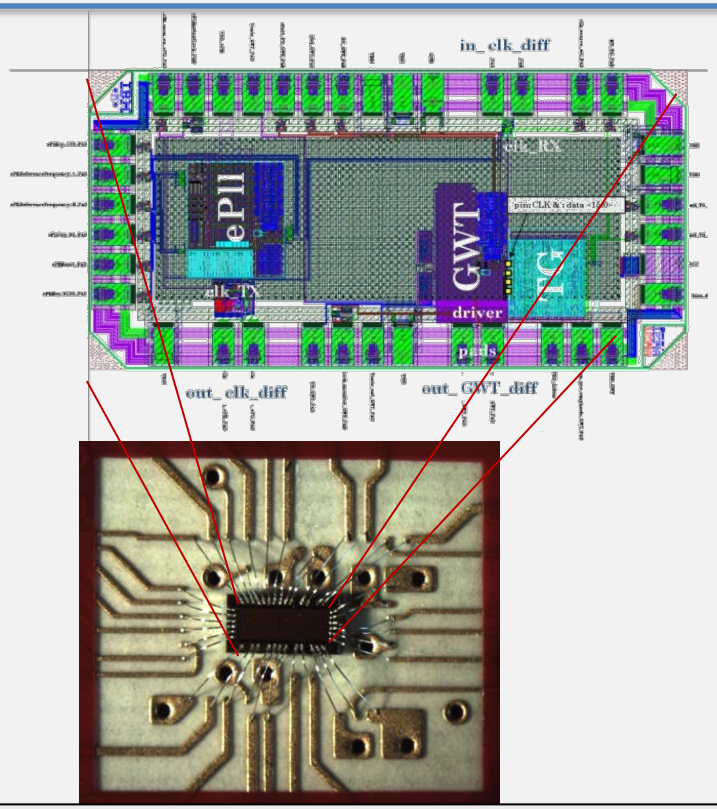


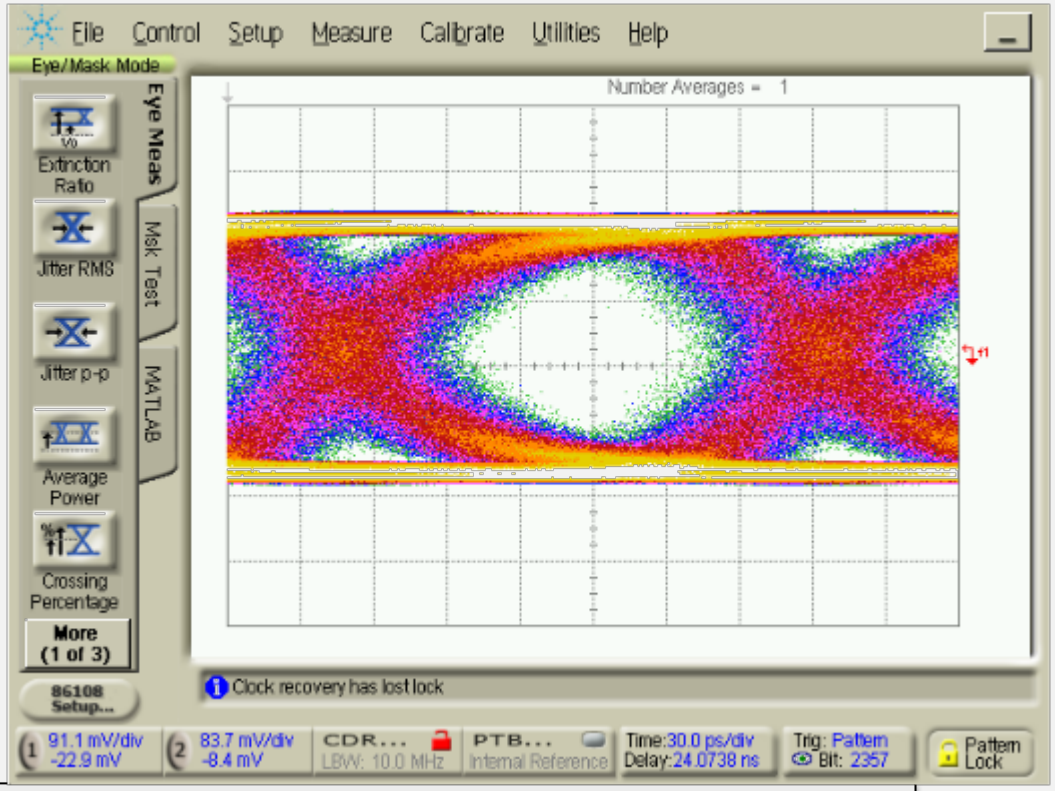
GWT : a 60-mW 5.12 Gbps serializer/transmitter



See a coming talk by Vladimir Gromov: "Development of a lower power 5.12 Gbps Data Serializer and Wireline Transmitter circuit for VeloPix chip" in TWEPP 2014

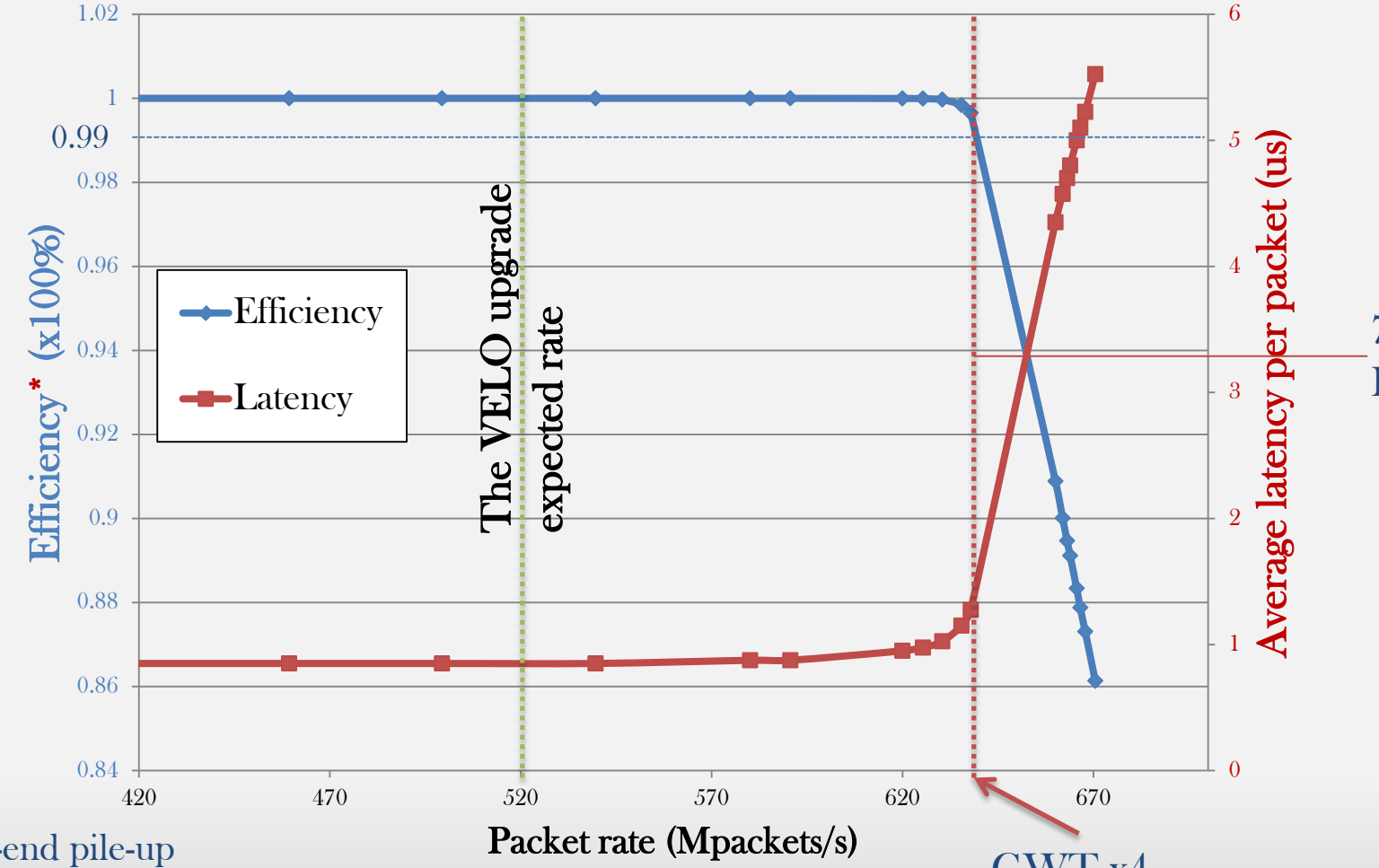
Velo_GWT test chip in 130nm CMOS technology





- 1 mm x 2 mm test chip in 130 nm CMOS technology
- Power : 5.12 Gbps serializer: 15 mW, wireline driver: 45 mW
- Eye diagram: +/- 200 mV is 60 ps (pseudo-random pattern)

Simulation: Data transfer efficiency

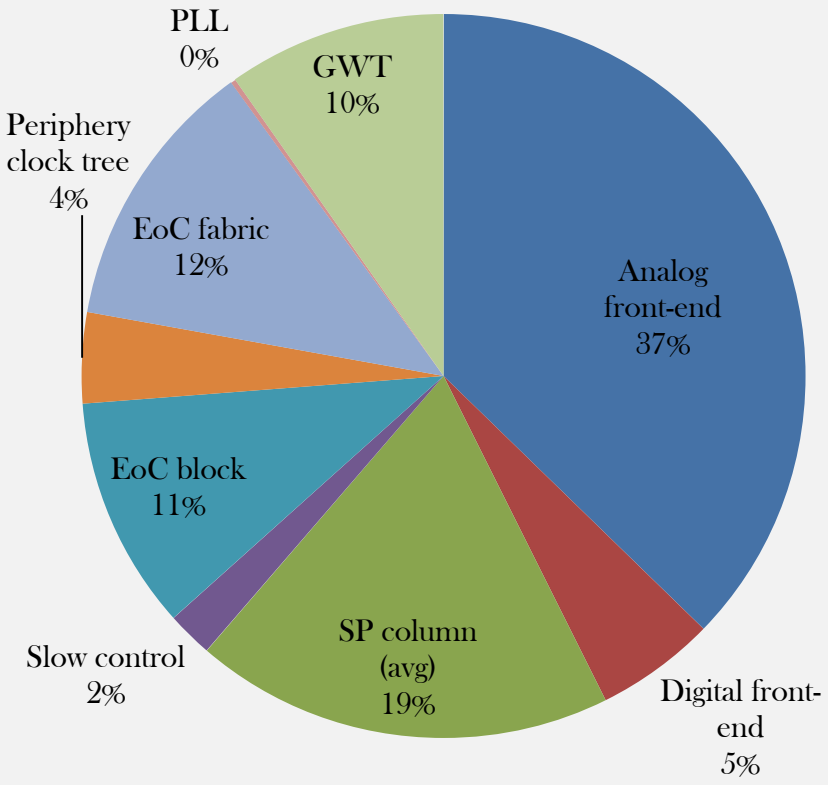


*no front-end pile-up taken into account

Summary: Power

Block	P (mw)	#Blocks	Total power
Analog front-end	0.014	65536	917.5
Digital front-end	0.002	65536	131.1
SP column (avg)	3.6	128	460.8
Slow control	*50*	*1*	*50 **
EoC block	*2*	*128*	*256 **
Periphery clock tree	*100*	*1*	*100 **
EoC fabric	*300*	*1*	*300 **
PLL	*5.5*	*1*	*5.5 **
GWT	60	4	240
		Total (mW):	2460.9
		W/cm^2	1.09

* estimated/budgeted



Summary

- Novel trigger-less HPD readout ASIC architecture was presented
  - Trigger-less, continuous
  - Reads out > 900 Mhits/s/ASIC, consuming < 1.5 W/cm^2
- VeloPix builds on expertise learned during the Timepix3 design
- GWT serializer (5.12Gbps/60mW) already demonstrated working in silicon
- Submission plans: Mid-2015, installation 2018 - 2019

Thank you for your attention!

Questions now?

Or later? Email tuomas.poikela@cern.ch.

Please also see related PIXEL2014 VELO upgrade talks:
1. E. Jans. "The VELO Pixel Upgrade", **Thursday 10:50.**
2. O. Augusto. Evaporative CO2 Microchannel Cooling for the LHCb VELO Pixel Upgrade. **Thursday 14:00.**

References:
[1] LHCb VELO Upgrade TDR. CERN LHCC 2013-021. 2013.
[2] L. Eklund, "The LHCb VELO Upgrade", ICHEP 2014
[3] T. Poikela. "Design and Verification of Digital Architecture of 65K Pixel Readout Chip for High-Energy Physics.", 2010.
[4] T. Poikela et al. "Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout", 2014
[5] T. Poikela et al. "Digital column readout architectures for hybrid pixel detector readout chips", 2014.

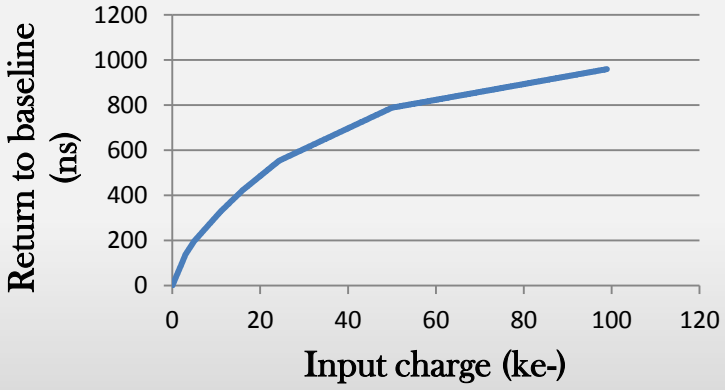
Front-end simulation

From schematic simulation

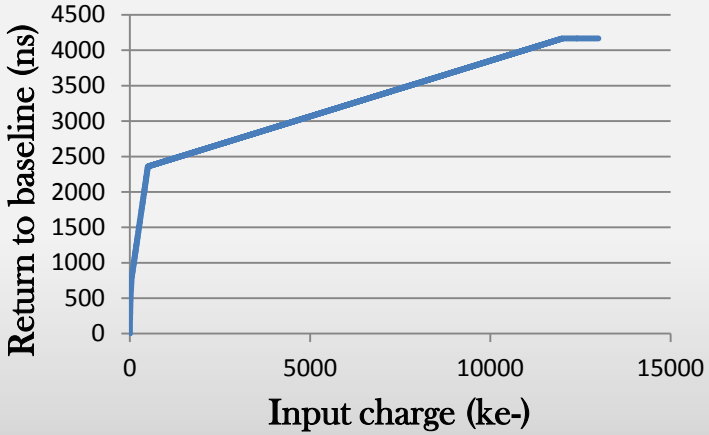
Qin ke-	TOT ns	ToA ns	time-to-baseline Threshold: 1ke-
1.75	49.7	21.1	80
1.8	50.9	20.7	81
3	71.5	16.6	138
4.9	101.4	14.6	198
10.9	200.7	11.3	329
16	282.2	9.8	423
24.3	400.2	8.8	554
50	618	8.2	789
500	1954	9.3	2360
12000	2393	10.1	4167

Perl script to model the front-end:
Qin => Dead time

FE response up to 100ke-



FE response up to 12Me-



Why 2x4 super pixel?

Table: Data rates for different super pixel dimensions:

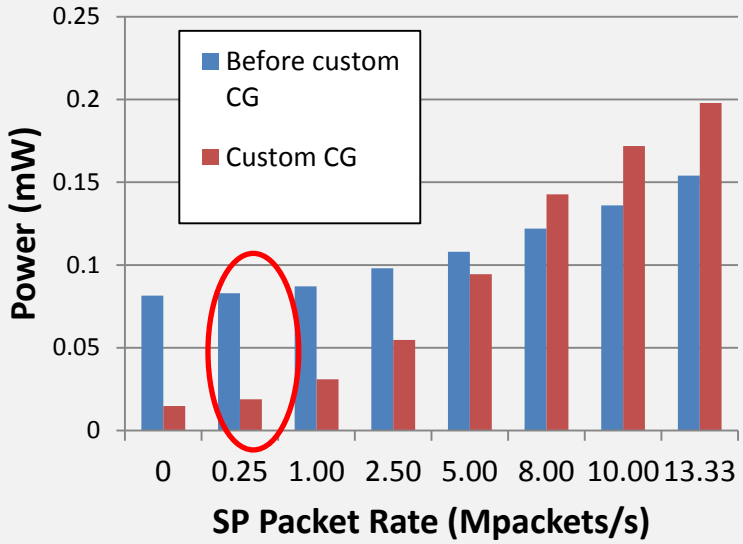
Binary encoded packets (no ToT)			
Super Pixel Geometry	**Data rate (Gbps)**	**Packet size (#bits)**	**Reduction (%)**
256 x 256	14.785	28 + N x 16	38.179
4 x 4	16.477	28 + N x 4	31.105
2 x 4	16.806	28 + N x 3	29.729
2 x 4	16.945	33	29.148
1 x 4	17.758	30	25.748
2 x 2	17.857	30	25.335
1 x 4	18.283	28 + N x 2	23.553
2 x 2	18.373	28 + N x 2	23.177
4 x 4	18.661	40	21.973
1 x 2	19.703	29	17.616
1 x 2	19.878	28 + N x 1	16.884
1, single pixel	23.916	28	0.000

Chosen format

No super pixel grouping

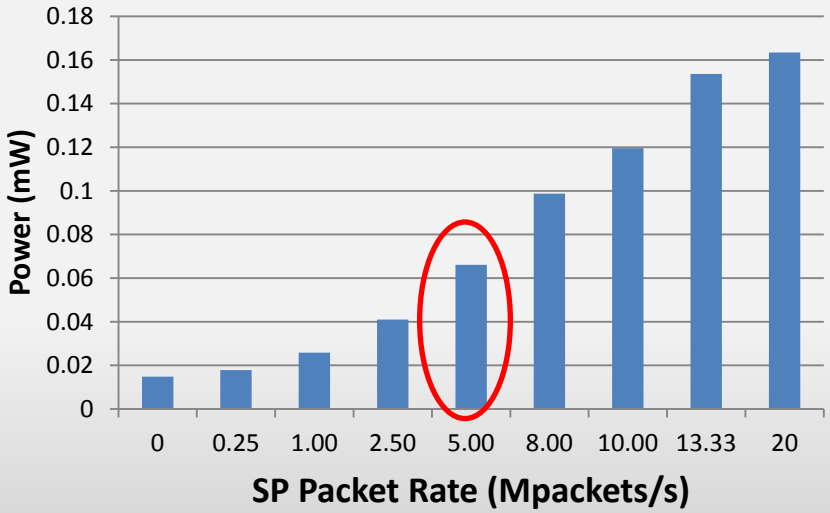
N = number of pixel hits in a packet

Super pixel power estimation



Power for SP hitmap buffers:

- Target rate approx. 300 kHz
- Power approx. 20 uW
- Hand-crafted clock gating (CG) works!



Power for transporting the packets:

- Target rate 5 MHz
- Power 66 uW

128 x 64 = 8192 Super pixels per chip!!