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VeloPix: The Pixel ASIC for the LHCb VELO Upgrade

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The LHCb Vertex Detector (VELO) will be upgraded in 2018 along with the other subsystems of LHCb in order to enable full readout at 40 MHz, with the data fed directly to the software triggering algorithms. The upgraded VELO is a lightweight hybrid pixel detector operating in vacuum in close proximity to the LHC beams.

The readout will be provided by a dedicated front end ASIC, dubbed VeloPix, matched to the LHCb readout requirements and the 55 x 55 um VELO pixel dimensions. The chip is closely related to the Timepix3, from the Medipix family of ASICs. The principal challenge that the chip has to meet is a hit rate of up to 900 Mhits/s, resulting in a required effective bandwidth of more than 16 Gbit/s. The occupancy is also very non uniform, and the radiation levels reach an integrated 400 MRad over the lifetime of the detector.

VeloPix is a binary pixel chip with a data driven readout, designed in 130 nm technology. The pixels are combined into groups of 2x4 super-pixels, enabling a shared logic and a reduction of bandwidth due to combined address and timestamp information. The pixel hits are combined with other simultaneous hits in the same super-pixel, timestamped, and immediately driven off-chip. The analog front end must be sufficiently fast to accurately timestamp the data, with a small enough dead time to minimize data loss in the most occupied regions of the chip. The data is driven off chip with a custom designed high speed serialiser.

The current status of the ASIC design, performance simulations and prototyping will be described, along with recent lab and testbeam results.

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